DESIGN OF LNA ASSEMBLY FOR GPS REPEATERS

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ABSTRACT

LNA ASSEMBLY FOR GPS REPEATERS

Global Positioning System (GPS) is a space-based radio navigation system, consisting of 24 satellites and ground support. GPS provides users with accurate information about their position and velocity, as well as the time, anywhere in the world. There is a little problem with GPS system that it has a poor reception inside the buildings and other covered structures. As GPS is becoming a part of daily life there is a requirement that user should access GPS inside the buildings and covered structures.

The main purpose of a GPS repeater is to pickup signal from the satellite and after amplification the signal is retransmitted inside the building. Our design will be in L2 band of GPS(1.5 GHz) consisting of a receiving antenna, low noise amplifier, power amplifier and a reradiating indoor antenna to make the feeble signals strong for reception by any GPS receiver.

DECLARATION

We declare that this thesis entitled “Design of LNA assembly for GPS Repeaters” is the result of our own work except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

DEDICATION

To our beloved Parents

ACKNOWLEDGEMENTS

We praise Allah Almighty, who gave us strength and perseverance to undertake this project and to complete it successfully.

We wish to express our gratitude to our supervisor; Associate Professor Farooq Ahmed Bhatti, from the Faculty of Electrical Engineering, Military College of Signals (MCS), National University of Sciences and Technology, for his exquisite support and supervision during the course of the project. His persistent guidance and wholehearted dedication was a source of inspiration for us.

Special thanks to Lec Zeeshan Zahid for giving us the guidance and help whenever we needed. The struggle of our parents for our well being and education cannot be overlooked. They have done enormous efforts to make us outshine. We would dedicate our success to them.

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CHAPTER 1

The thesis proposed Design of LNA assembly for GPS Repeaters aims at designing an LNA assembly consisting of receiving antenna, a low noise amplifier, a power amplifier and a transmitting antenna. The design is carried out in Advanced Design Systems (ADS).

1.1 Background

GPS is a radio navigation system used for tracking the position and giving the weather forecast information. In addition, GPS is the backbone for modernizing the global air traffic system.

GPS technology finds its weakness inside the buildings, where the constellation of 4 GPS satellites is not available and the signals are feeble enough to be received by GPS receiver residing inside the building. For this we need to have an amplifying assembly after the receiving antenna, and the reradiate those signals inside the building through the reradiated antenna.

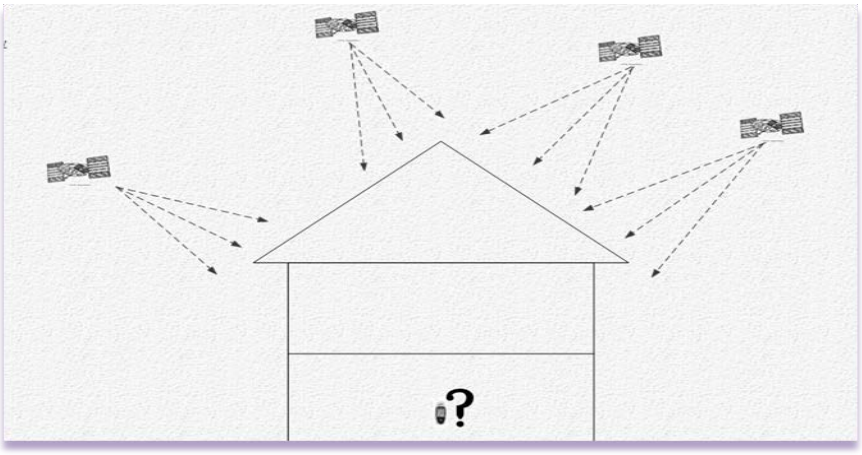


Fig 1. GPS Constellation

1.2 Low Noise Amplifier

Low Noise Amplifiers (LNA's) are used to amplify weak signals received by the antenna. They are one of the important components employed in the wireless systems. Such systems are widely used in communication systems as well as in radars. LNAs find wide applications in commercial electronics, surveillance radars, satellite communication and navigational aids for both civil and military systems. LNA forms an important part of the receiver front end, especially in microwave range. They determine the sensitivity of the receiver to the incoming signals, which are usually low power due to long distance or low transmitted power. If the noise figure (NF) of LNA is less, then the receiver can process lower power signals, thereby increasing the reception range without increasing the transmission power. The design in microwave frequency range is quite different from that in the lower frequency ranges. The main reason for this is change in behavior and impact of active and passive devices on the circuit in this frequency range, this poses a great challenge to the designers of RF/microwave circuits.

Low noise amplifiers are used as front end amplifier of receiver so that receiver sensitivity is improved by low noise Figure and high gain in first stage. Noise from subsequent stages is reduced by the gain of LNA while noise of LNA itself is directly introduced into the received signal.

The given specification demand broad band, high gain and low noise amplifier. A systematic process will be carried out keeping in view the desired specifications, availability of devices, and cost effects. These desired specifications for the LNA are shown in table:

1.3 Design Specifications of LNA

Table1. Specifications of LNA

SPECIFICATON	DESIRED VALUE
Frequency Range	1.2-1.6 GHz
Bandwidth	0.4 GHz
Gain	>10 dB
Noise Figure	<1dB

CHAPTER 2

LITERATURE REVIEW

2.1 Passive Devices

Passive devices are those devices that do not require external energy for their operation. Examples of passive devices are electrical resistors, capacitors, diodes, optical fibers, cables, wires, glass lenses, and filters etc.

Passive components have a property that they do not increase the power of the signal because they have gain always less than one.

2.2 Active Devices

Active devices are those devices that require external power for their operation. Examples of active devices are transistors, amplifiers, silicon control rectifiers (SCRs) etc. The signal is fed into one terminal of the Active device and the amplified version taken from another terminal. The source of power is usually a dc voltage from a battery or power supply.

All active devices control the flow of electrons through them. Some of the active devices available in the industry allow a voltage to control this current while other active devices allow another current to do the job.

2.3 Scattering Parameters

S parameters are useful method of representing circuit as “black box”. External behavior of circuit can be predicted regardless of the content inside the circuit.

A two port network is analogous to Black box that may contain anything resistor, capacitor, transmission line or integrated circuit. Figure 2.1 represents 2 port network. The Ports are terminal pair of lines.

Figure 2.1 Two port network

S parameters are measured by sending mono frequency signal into the network and noting what comes to be the output. For a wave incident on port one some part of it is reflected back on same port while some part exits on other ports.

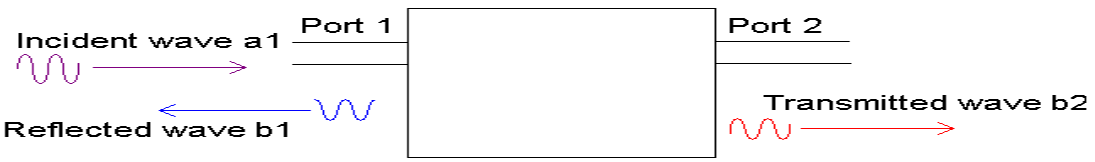


Figure 2.2 Incident, reflected, transmitted wave

S parameters are represented as S11, S22, S21, and S12. S11 refers to signal reflected at port one for signal incident on port 1. S11 is also called input reflection coefficient .S11 is ratio of two waves a1 and b1 .

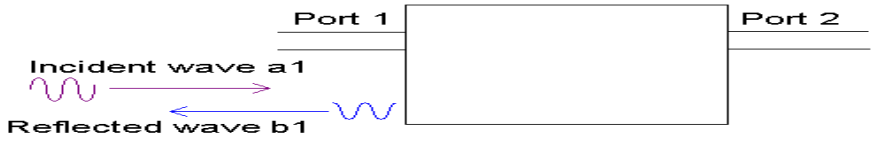


Figure 2.3 Input Reflection Coefficients (S11)

S21 refers to signal exiting at port 2 for input signal at port 1. S21 is also called forward transmission coefficient or gain. S21 is the ratio of two wave's b2 and a1 which is mathematically defined as b2/a1. Two waves forming S21 are represented in Figure 2.4.

Figure 2.4 Forward Transmission Coefficient (S21)

S22 is output signal at port 2 to the input at port 1. S22 is also called output reflection coefficient. S22 is the ratio of two wave's a2 and b2 and is mathematically defined as b2/a2. Two waves representing S21 are described in Figure 2.5.

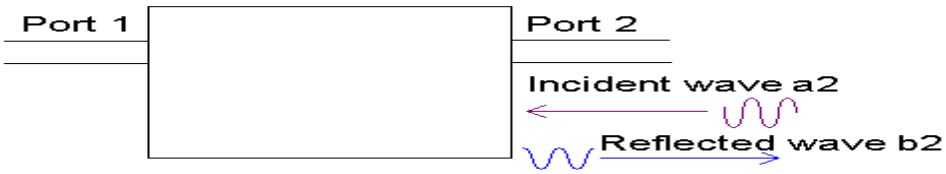


Figure 2.5 Output Reflection Coefficient (S22)

S12 refers to signal exiting at port 1 for signal at port2. S12 also refers to reverse transmission coefficient. S12 is the ratio of two wave's a2 and b1 and is mathematically given as b1/a2. Two waves representing S12 are described in Figure 2.6.

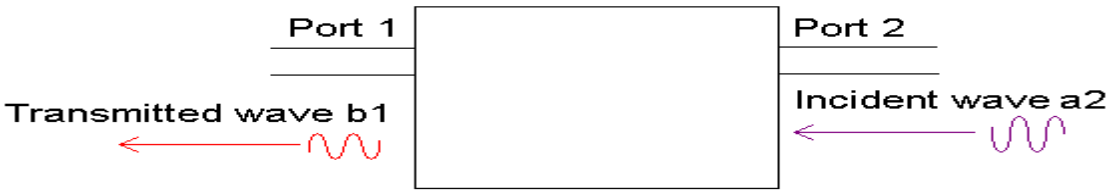


Figure 2.6 Reverse Transmission Coefficients (S12)

S parameters rely upon network, characteristic impedances of source and load and desired frequency. Matrix algebraically representing two port networks is shown with the help of Equation 2.1

$$\begin{pmatrix} b1 \\ b2 \end{pmatrix} = \begin{pmatrix} S11 & S12 \\ S21 & S22 \end{pmatrix} * \begin{pmatrix} a1 \\ a2 \end{pmatrix} \quad \text{.....} \quad \textbf{Equation 2.1}$$

Some matrices are symmetrical. In case of symmetrical two port network it means S21=S12 i.e. changing input and output port does not change transmission properties. Transmission line is an example of two port symmetrical network.

S-matrix for n port network contains n^2 coefficient. No of rows and columns in s parameter matrix is equal to no of ports. For the S-parameter subscripts "i j", "j" is the port that is excited (the input port) and "i" is the output port.

2.4 FR-4 Substrate

FR-4 substrate is a fundamental and bears an importance in RF applications, finds its applications in Relays, Bus Bars, Washers, Arc Shields, Test Boards, Transformers, Printed Circuit Boards, Panels, Sockets, Coils, Fuses, Motors, Generators, Condensers, Antennas, Wave Solder Pallets, Knife Handles Carriers, and more.

Figure 2.7 FR-4 Sheets available in Prototyping Facility

The properties of FR-4 that is available in prototyping facility are shown in table 2.1.

PARAMETERS	SYMBOL	VALUES
THICKNESS	H	1.6mm
DISSIPATION FACTOR (LOSS TANGENT)		0.02
DIELECTRIC CONSTANT (PERMITTIVITY	Er	4.3
CONDUCTOR THICKNESS	T	17um
CONDUCTIVITY	K	5.813E+7

Table 2.1 Properties of available FR-4

Layout of Printed circuit board on FR-4.

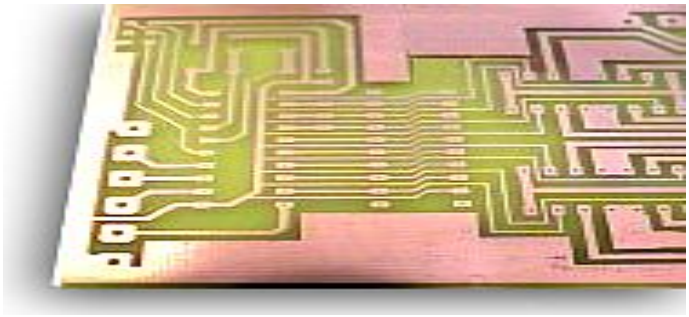


Figure 2.8 PCB Layout on FR-4 substrate

2.5 AMPLIFIER TOPOLOGIES

Amplifier can be classified according to any of the three topologies. They are discussed below.

2.5.1 Common Source

(a). Common source (CS) configuration is widely used in almost all amplifier circuit.. it is used catering for the gain and whether single stage or cascade. Figure 2.9 shows common source amplifier.

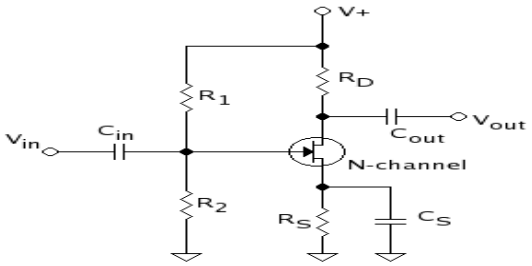


Figure 2.9 Common Source Amplifier

2.5.2 Common Drain

(b). Common drain is commonly known as source follower and is made by making signal ground at drain. Its gain is nearly equal to unity. It is mostly used as buffer. It has a very low output resistance and is potent to drive low impedance circuit. Figure 2.10 shows common drain amplifier.

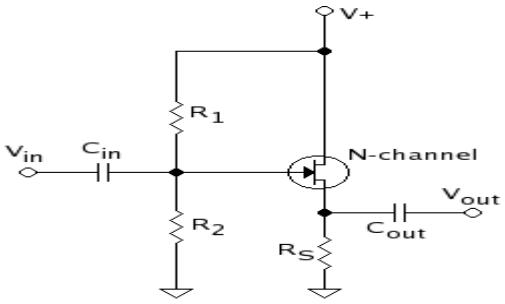


Figure 2.10 Common Drain Amplifier

2.5.3 Common Gate

(c). Common gate configuration is established by establishing signal ground on gate terminal. Input resistance of common gate is low. It is mostly used as a current buffer. Figure 2.11 shows common gate amplifier.

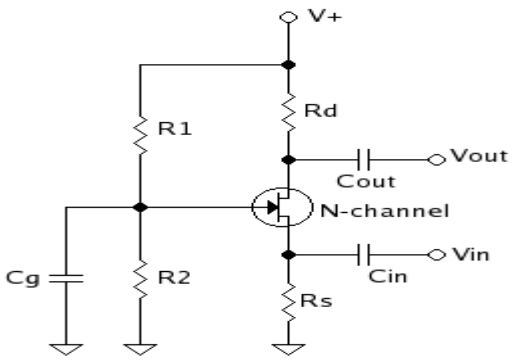


Figure 2.11 Common Gate Amplifier

2.6 Biasing Networks

Biasing networks are used for obtaining predetermined voltages and/or currents at various points of a circuit to set an operating point. In electronics a bias point also known as quiescent point or Q-point is a DC voltage which when applied to device causes it to operate in required fashion. Different biasing are chosen in order to control voltage and current. Following topologies were studied.

2.6.1 Current Mirror

(a). It is the typical type of active biasing. In Active biasing transistors are utilized for controlling the current and voltage. In special case of identical transistors the current simply replicates the reference current in output terminal.

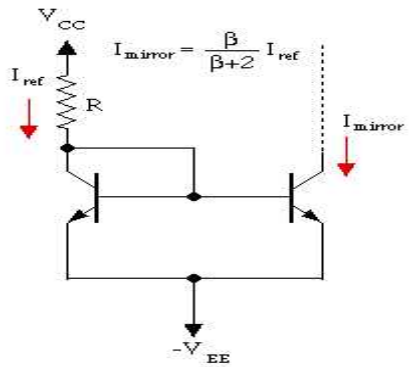


Figure 2.12 Current Mirror

2.6.2 Resistive Biasing

(b). It is passive biasing. In passive biasing only lumped components are used. Resistive biasing has been employed in the amplifier design schematic considering its simple structure.

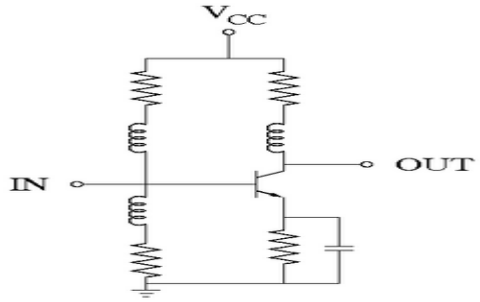


Figure 2.13 Resistive Biasing

2.6.3 Matching Network

Matching in RF networks means to match the input and output pair for maximum power transfer. In transmission lines problems matching means simply terminating the line in its characteristic impedance.

Block diagram of input and output matching networks are shown in Figure.

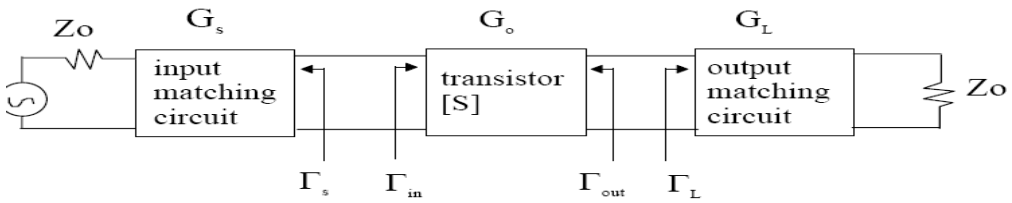


Figure 2.14 General input/output Matching Networks

There are many ways in which matching networks can be designed. Two fundamental techniques that were utilized in amplifier design schematic are discussed below.

2.6.4 Lumped Components

This uses two reactive elements to match arbitrary load impedance to transmission line. The main advantage is that it saves a lot of space.

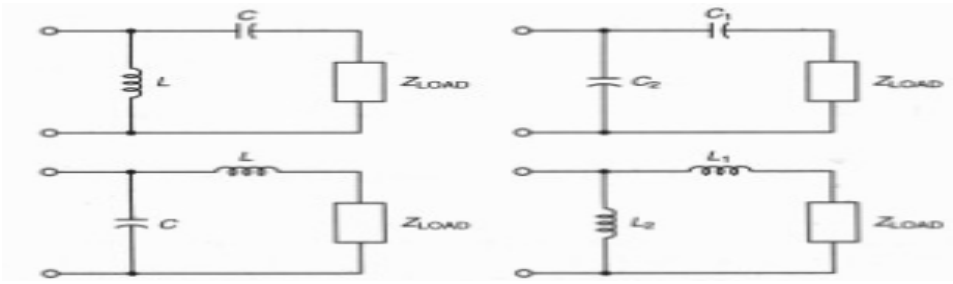


Figure 2.15 Lumped Components Matching Networks

2.6.5 Transmission Line

Transmission line is a medium or structure that is used for directing the transmission of energy. Figure below shows matching using transmission lines

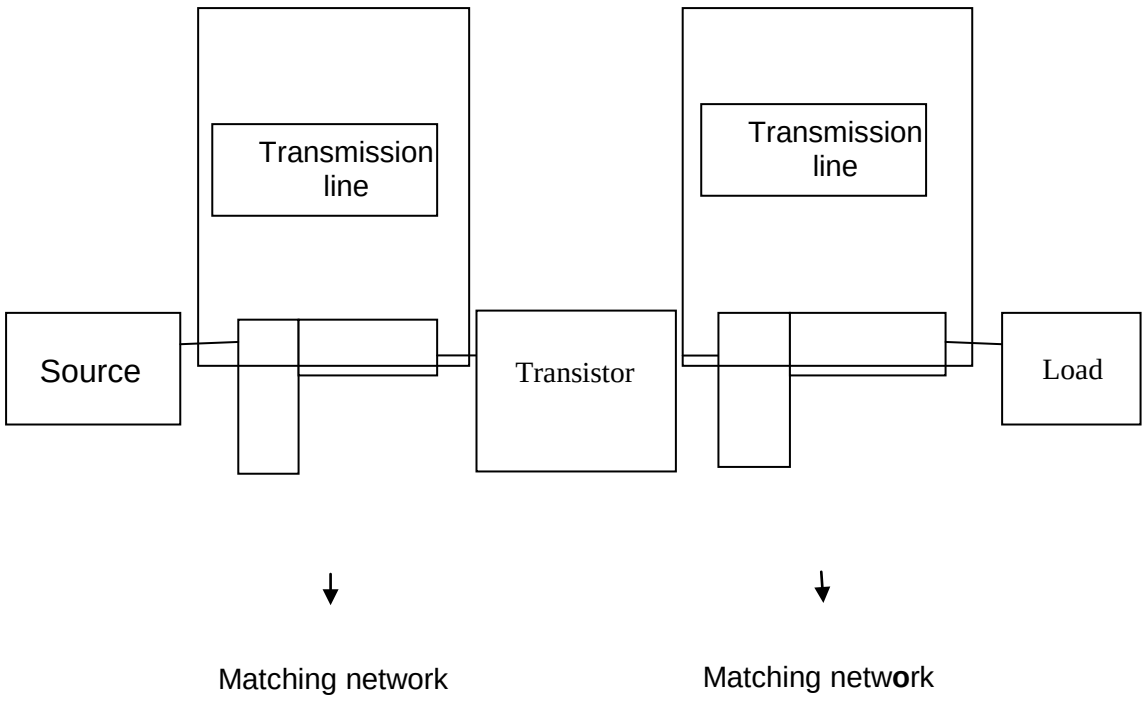


Figure 2.16 Matching Network using Transmission Lines

CHAPTER 3

THE LNA DESIGN PHILOSOPHY

The design of the LNA is carried out in ADS which is an industry grade RF simulator. This project implements the design of a low noise amplifier (LNA) for the GPS repeaters. LNA is an integral part in the receiver front end in the microwaves communication systems. We will be designing LNA at 1.2GHz to 1.6GHz. The design will be implemented using Gallium Arsenide (Gas) pseudomorphic High Electron Mobility Transistors (pHEMT's) on FR-4 substrate. Gas pHEMT's have been selected for LNA design because of their low noise figure and stable response at the frequency band of interest. Gas can achieve high efficiency and linearity, as well as provide high output.

3.1 Advanced Design System (ADS)

ADS provides an integrated environment to designers of RF electronic products such as amplifiers, oscillators, mixers, wireless satellite communications, radar systems, and high-speed data links.

3.2 Low Noise Amplifier Design

The design of low noise amplifier was carried out in Advanced Design Systems (ADS) which is an industry grade software.

3.2.1 Analytical Design

First of all Device Selection was carried out. Then block diagram for LNA was drawn for analysis. After this the Stability analysis was done. Matching networks Layout is carried out as the final step.

3.2.2 Device Selection:

In order to design a low noise amplifier, the transistor must be DC biased at a desired operating point. These depends mostly on the application (low noise, high gain, high power), and the type of the transistor. A transistor which will have gain of more than 10 dB and noise figure of less than 1 dB is desired. For this purpose ATF54143 (pHEMT) is a suitable choice. The details of ATF 54143 are given in appendix.

3.2.3 Block diagram for LNA:

The block diagram of the initial design of LNA is shown via a block diagram. Firstly , designing the matching networks which is of utmost importance.

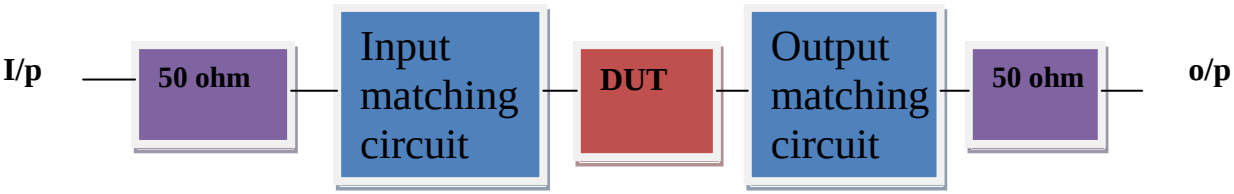


Figure 3.1 The Block Diagram with matching networks

3.2.4 Stability Analysis

Two-port network may be unconditionally stable or potentially unstable. It is very important that the amplifier does not oscillate in the product environment, since such behavior leads to product malfunctioning. Oscillations occur due to unstable. Certain source or load terminations that produce the oscillations provide the conditions necessary for the unstable behavior. This type of

design is called a **conditionally stable design**.. It becomes very difficult to know the real cause. If the **conditionally stable** design method is utilized, extreme care must be observed to guarantee that a source or load termination that produces an oscillation is never presented to the amplifier. This applies to all frequencies in-band and out-of-band. This can be a difficult task at best in most applications.

Two-port stability is analyzed using stability circles or equations.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \quad \text{..... (1)}$$

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| \quad \text{..... (2)}$$

$$B_1 = 1+|S_{11}|^2-|S_{22}|^2-|\Delta|^2 \quad \text{..... (3)}$$

$$B_2 = 1+|S_{22}|^2-|S_{11}|^2-|\Delta|^2 \quad \text{..... (4)}$$

3.2.5 Analytical Analysis

The design begins with the analytical design in which the S parameters of the device are analyzed and consequently the stability circles etc are drawn on Smith Chart. The complete analytical design proceeds as:

S- parameters @ 1.5 GHz ATF- 54143

From equation (1) we have

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}$$ …….. (5)

In rectangular coordinates

S_{11}= -0.55-0.32j…….(6)

S_{22}= -0.055-0.20j……(7)

S_{12}= 0.04+0.03j……..(8)

S_{21}= 0.64+9.31j…….(9)

Δ= S_{11} S_{22}- S_{21} S_{12}…….(10)

Δ = (-0.55-0.32j) (-0.055-0.20j) – (0.04+0.03j) (0.64+ 9.31j)……..(11)

Δ= 0.33 ……..(12)

Putting the values of S- parameters and Δ in equation 1, we get

K= 0.7

sm= 0.3 ∠150

3.2.6 Design of input matching network

The input and output matching networks are designed analytically on Smith Chart using the equations. Either lumped or distributed components can be used.

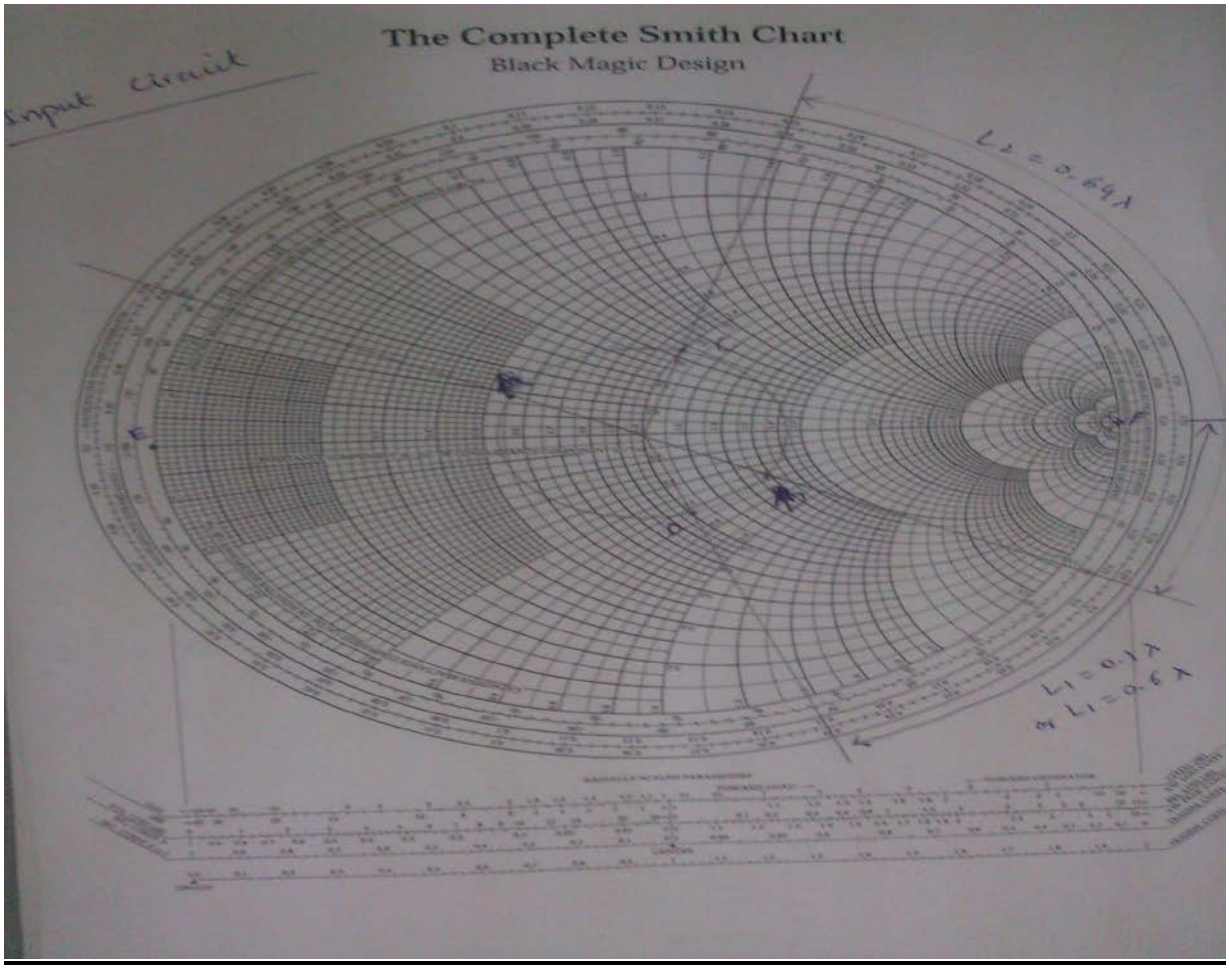


Figure 3.2 Input Matching on Smith Chart

Using smith chart we draw the input matching network circuit as shown in figure 1.

Hence

$\lambda = 720$, BC $= 0.14\lambda$, $L_2 = 0.14\lambda$ And $L_2 = 0.14\lambda + \lambda/2 = 0.64\lambda$

$L_1 = 0.6 \times 210\text{mm} = 126\text{mm}$, $L_2 = 0.14 \times 210\text{m} = 29.4\text{mm}$

3.2.7 Output matching circuit

Output matching circuit is designed using the same method as the input matching circuit. Here lumped components (lumped capacitor and inductor) were used.

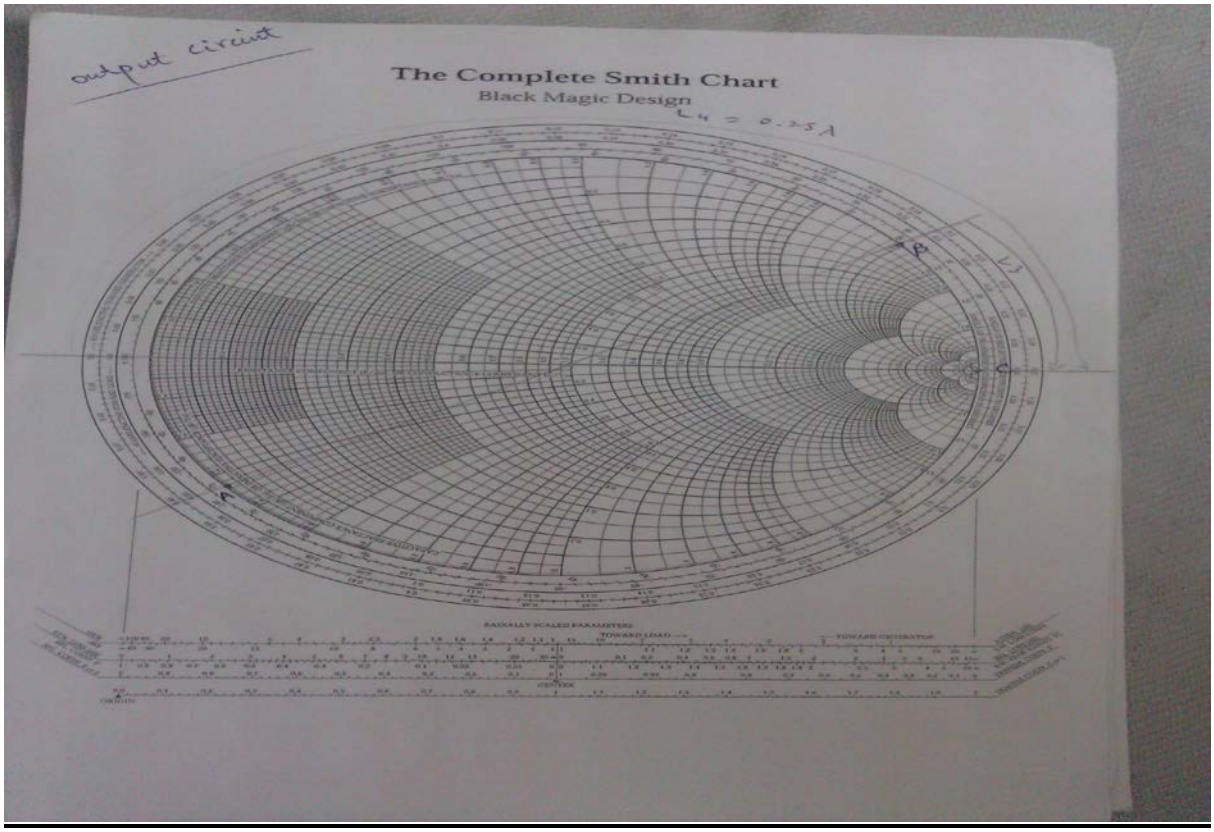


Figure 3.3 Output Matching on smith Chart

repeating the same procedure

$L_3 = 0.053\lambda = 11.08mm$

$L_4 = 0.25\lambda$ (open circuited stub)

$L_4 = 52.5mm$

3.2.8 Stability curves

The stability circles were also drawn on Smith Chart and also in ADS using Smith Chart utility. The region on Smith Chart outside the circle is stable region so the emphasis was laid to make the transistor unconditionally stable.

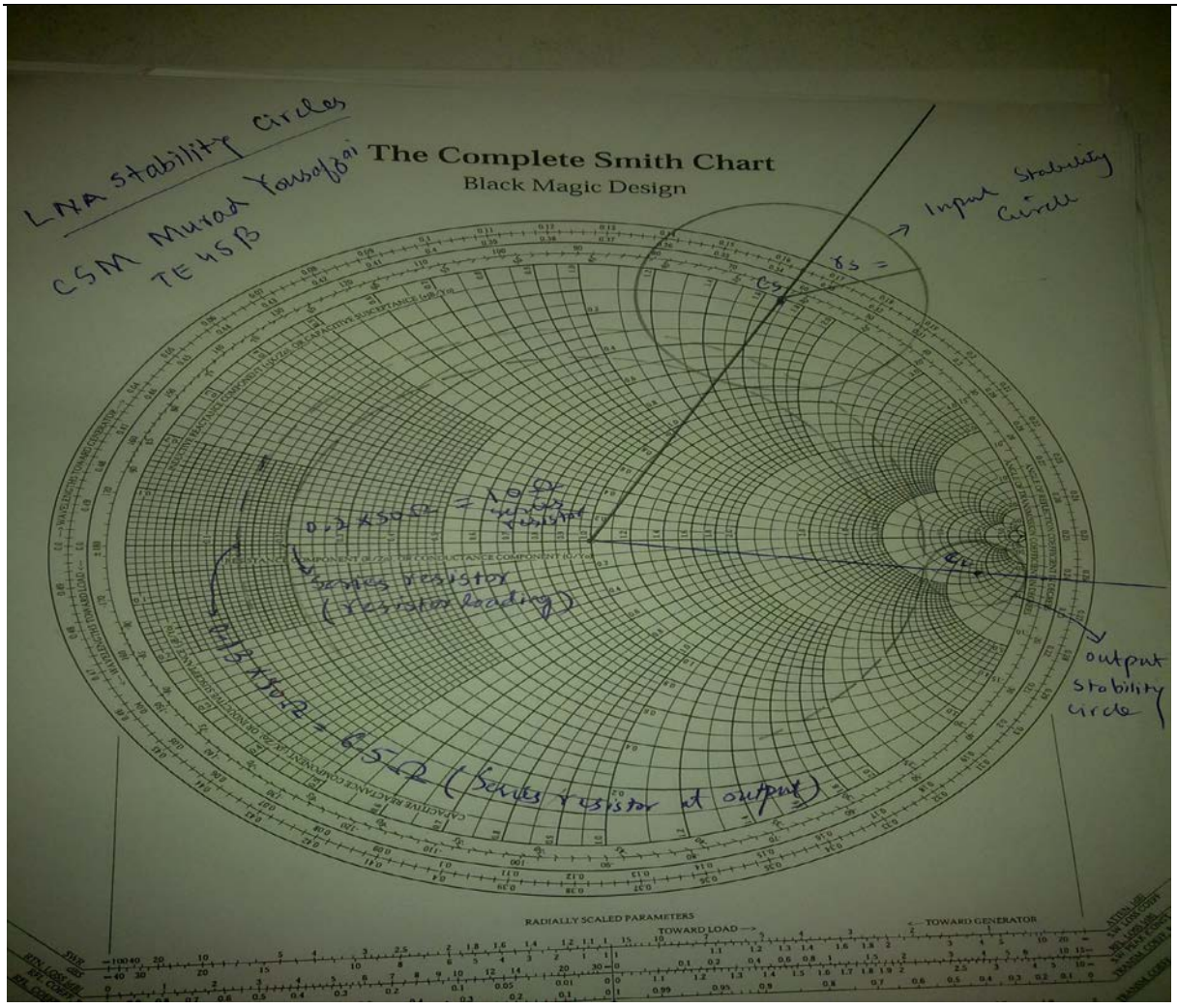


Figure 3.4. Stability Circles

3.3 Design on ADS

After carefully designing the circuit analytically the next step was to design it on ADS. The same lengths of the transmission lines were used as calculated and Linecalc utility in ADS was utilized in this regard.

3.3.1 Initial Schematic Design in ADS

initial schematic design is as shown.

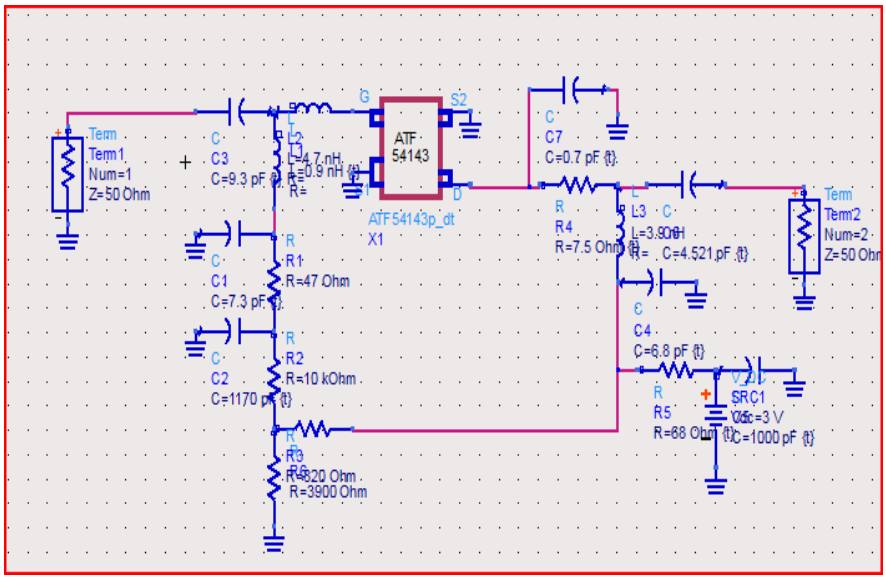


Figure 3.4 Schematic Design

3.3.2 Microstrip Design

After designing the MLIN circuit, it was then modified to microstrip elements so that its layout can be generated.

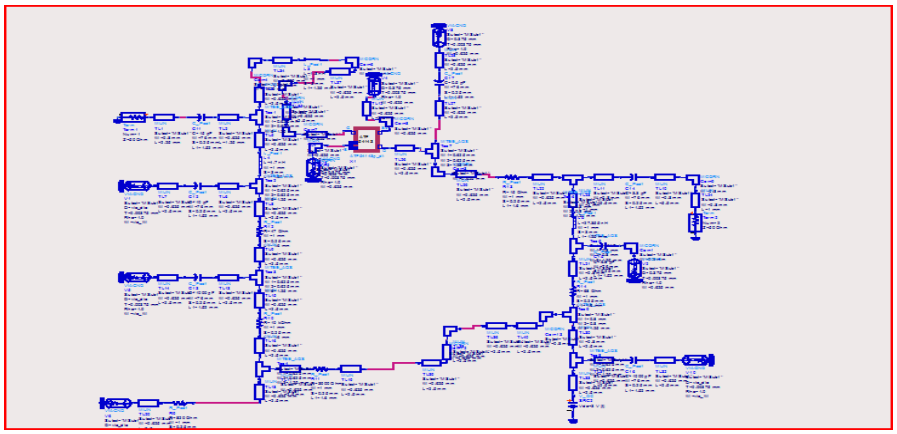


Figure 3.5 Microstrip Design

3.3.3 The Layout in ADS

The design in schematic window was then exported to generate the layout for fabrication.

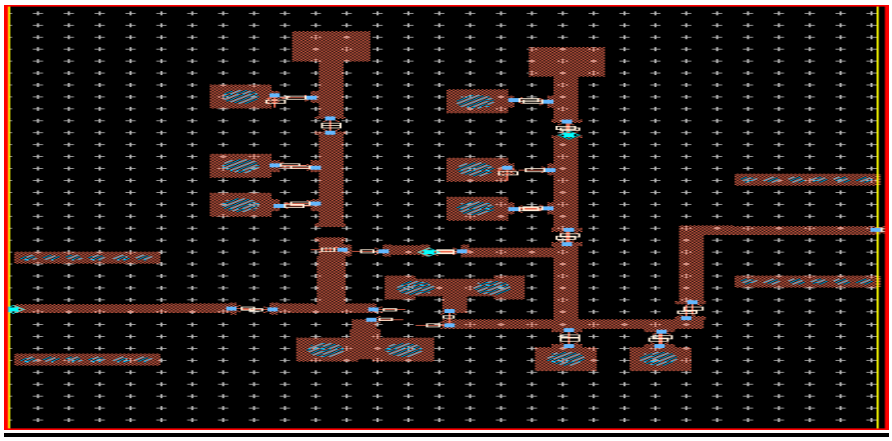


Figure 3.6 The Layout

3.3.4 The Co-simulation/ EM Simulation

The last very important step is to do the co-simulation which is done in order to cater for all the parasitic effects in the layout. The results obtained after co-simulation match closely with the practical results.

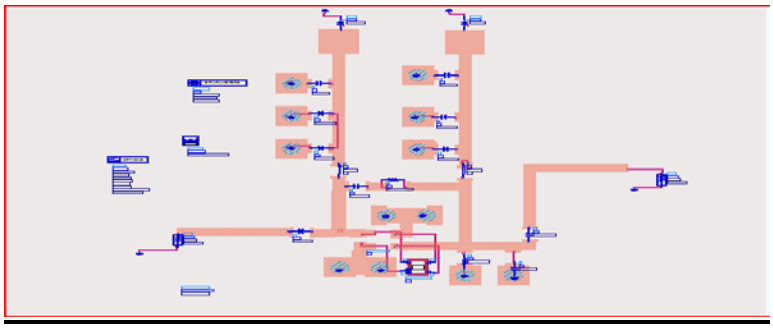


Fig 3.7 The Cosimulation

3.3.5 Simulation results (the S parameters)

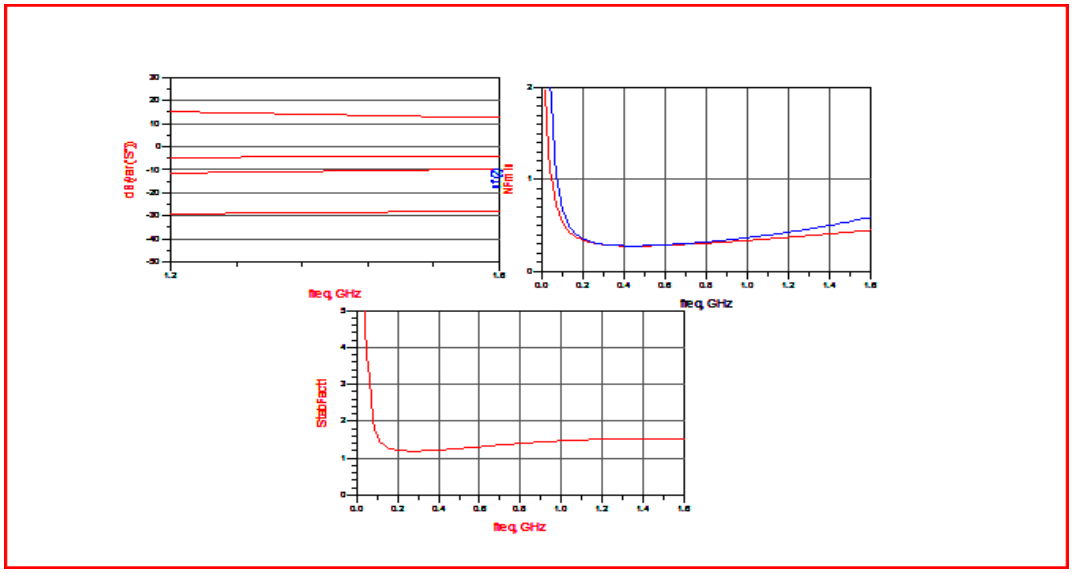


Fig 3.8 Cosimulation Results

CHAPTER 4

THE ANTENNA DESIGN

The two critical steps in designing the patch antenna were the definition of the patch dimensions and the feeding configuration. The dimensions have an influence on the operating frequency and on the antenna gain. The difficulty to predict accurately the patch dimensions is related to the fringing fields together with the small size of the ground plane used.

The feeding provides correct impedance at the coupling point. At high-signal frequencies it is necessary to design a feeding line with specific characteristic impedance. The patch antenna was fed with a micro strip line connected to a point inside the patch where the input impedance is 50 Ω.

4.1Concept of Radiation in Patch Antenna:

To understand working of this antenna, it is important to have the concept of radiation in single patch antenna.

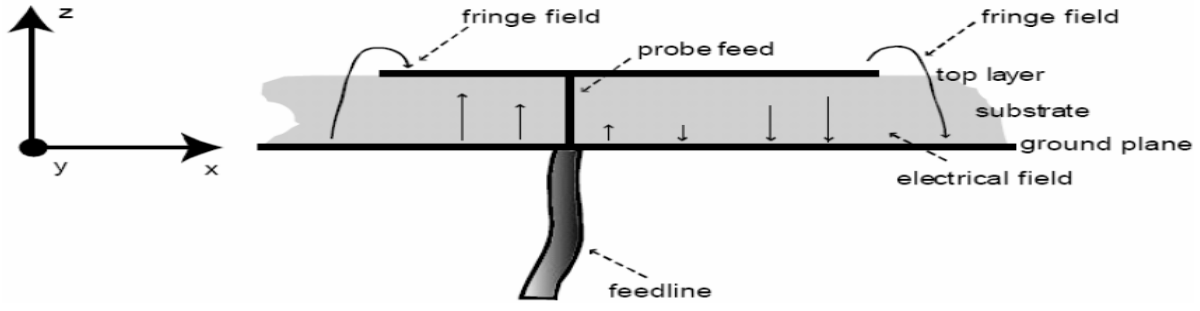


Figure 4.1. Basic Microstrip Patch radiation

The substrate is clad with two conductive layers. The resonant frequency is based on dimensions and substrate properties. The feed probe couples Electromagnetic Energy into the antenna structure. Lowest order mode is TE_{10}.

4.2 Feeding Methods:

There are many configurations that can be used to feed micro strip antennas. The most popular are micro strip line, coaxial probe and aperture coupling. Aperture coupling is the most complicated of all. It consists of two substrates separated by ground plane. It has the advantage of providing good matching but provides very narrow bandwidth.

4.3 Substrate Properties

There are many substrates that can be used for the design of micro strip antennas, and their dielectric constants are usually in the range of $2.2 \leq \varepsilon_r \leq 12$. Desirable for good antenna performance are thick substrates whose dielectric constant is in the lower end of the range because they provide better efficiency, loosely bound fields for radiation into space, but at the expense of larger element size.

The substrate selected for this project was the Rogers RO-4350B because its dielectric constant ε_r=3.66 which is desirable for good performance as it is in the lower end of the range. Also the height of the substrate h= 20 mils, which is low and hence good for microwave circuitry of this project.

4.4 Antenna design:

Three of the parameters were known before other calculations which were the dielectric constant of the substrate **(ε_r),** the resonant frequency (f_r) and the height (h) of the substrate. The substrate used is Rogers RO-4350B with dielectric constant ε_r=3.66 and height h= 20 mils (0.02 inch). The resonant frequency **f_r = 1.575 GHz.**

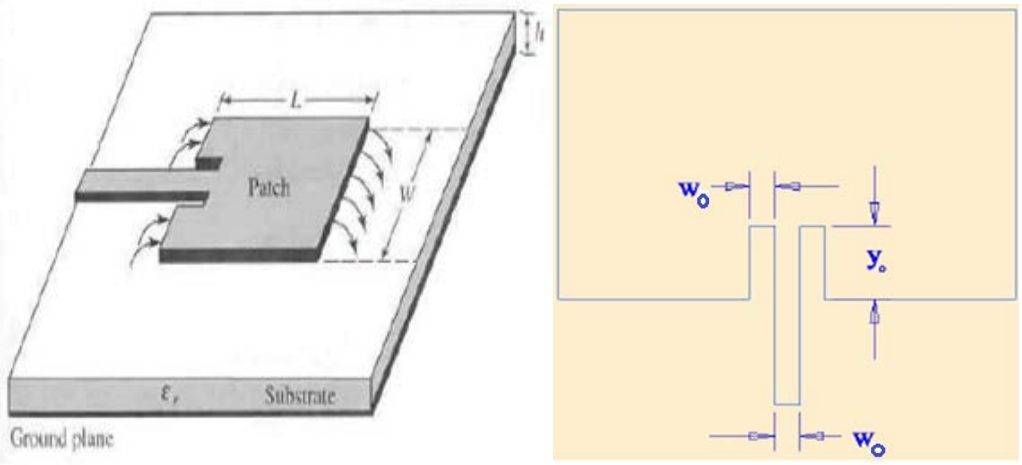


Figure 4.2 Denotation of Dimensions of Rectangular patch [3]

$$W = \frac{1}{2f_r\sqrt{\mu_0\varepsilon_0}}\sqrt{\frac{2}{\varepsilon_r+1}} = \frac{v_0}{2f_r}\sqrt{\frac{2}{\varepsilon_r+1}} \qquad 3.1$$

For W/h > 1 calculated by :

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left[1+12\frac{h}{W}\right]^{-1/2} \qquad 3.2$$

$$\frac{\Delta L}{h} = 0.412\frac{(\varepsilon_{eff}+0.3)\left(\frac{W}{h}+0.264\right)}{(\varepsilon_{eff}-0.258)\left(\frac{W}{h}+0.8\right)} \qquad 3.3$$

1. The actual length (L) of the patch is then found by:

$$L = \frac{1}{2f_r\sqrt{\varepsilon_{eff}}\sqrt{\mu_0\varepsilon_0}} - 2\Delta L \qquad 3.4$$

$$Z_C = \frac{120\pi}{\sqrt{\varepsilon_{reff}}\left[\frac{W_o}{h}+1.393+0.667\ln\left(\frac{W_o}{h}+1.444\right)\right]} \;;\; \frac{W_o}{h} > 1 \qquad 3.5$$

2. The inset feed point (y_o) was then calculated by the formula:

$$y_o = 10^{-4}\left\{\begin{matrix}0.001699\varepsilon^7{}_r + 0.13761\varepsilon^6{}_r - 6.1783\varepsilon^5{}_r + 93.187\varepsilon^4{}_r - 682.69\varepsilon^3{}_r + \\ 2561.9\varepsilon^2{}_r - 4043\varepsilon_r + 6697\end{matrix}\right\}\left\{\frac{L}{2}\right\} \quad (2 \le \varepsilon_r \le 10) \qquad 3.6$$

3. The length of the feed line was kept equal to $\lambda_o/3$ and the width of the notches was also kept same as the width (W_o) of the feedline.

The results obtained are as follows:

- Width (W) = 62.36 mm
- Effective dielectric constant (ε_{eff}) = 3.5
- Extended Incremental length (ΔL) = 0.24 mm
- Length (L) = 46.1 mm
- Width of feed line (W_o) = 1.1066 mm

Inset Feed Point Distance (y_o)= 13.24 mm

4.5 Antenna Model Simulation

The patch antenna model using the above calculations was designed in ADS and the dimensions were adjusted to achieve the resonant frequency.

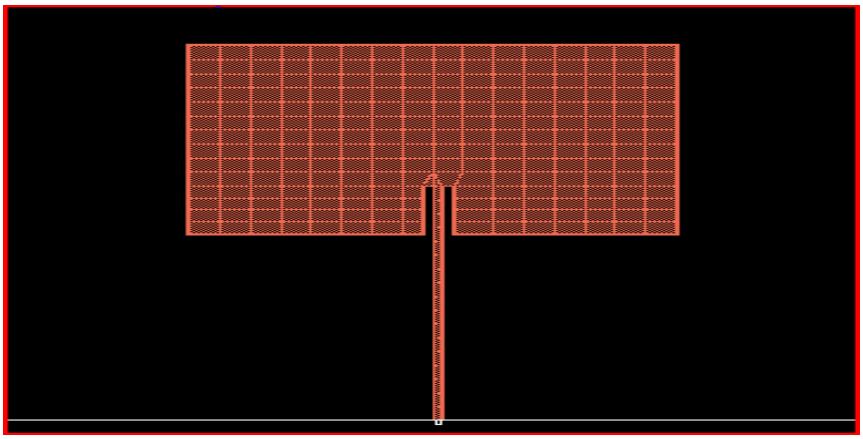


Fig 4.3. Antenna Model

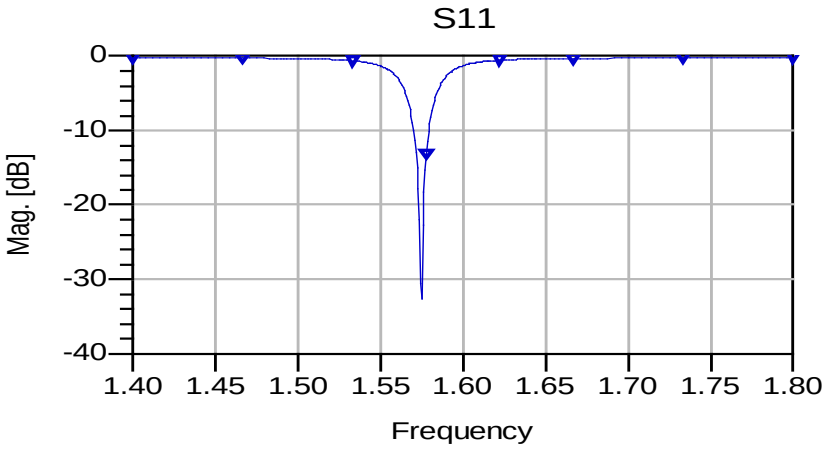


Figure 4.4 The Reflection Coefficient

using the 3D analysis the radiation plots were drawn in ADS.

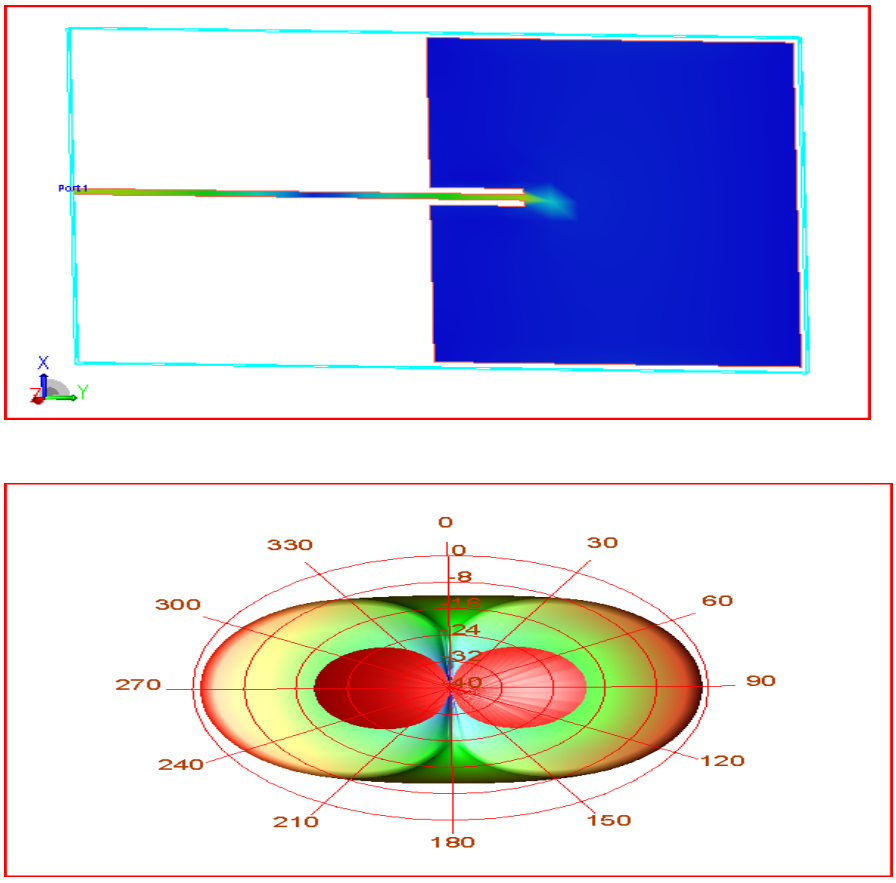


Figure 4.5 The Radiation Plot

CHAPTER 5

POWER AMPLIFIER

The second important module of repeater assembly is the design of power amplifier which acts as a signal compensator as well as provides enough gain to the signal so that it can be fed to the reradiating antenna.

5.1 POWER AMPLIFIERS

A variety of applications use Power Amplifiers such as Radar, RF heating and Wireless Communication. The techniques for RF power amplification can use classes as A, B, C, D, E, and F, for frequencies ranging from VLF (Very Low Frequency) through Microwave Frequencies.

5.2 Power Classes Definition

Power amplifiers are divided into class A,B,C,D,E etc. The choice of selecting one of them depends upon linearity and the desired

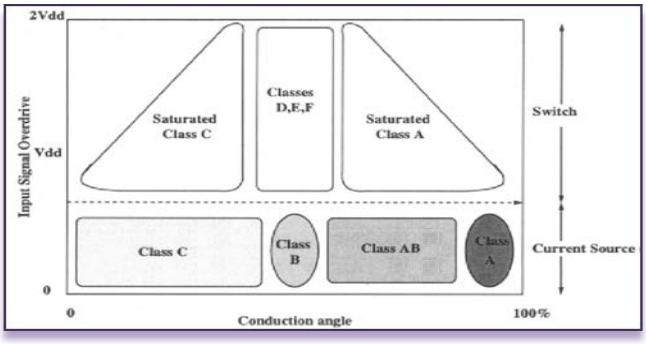


Figure 5.1 power classes

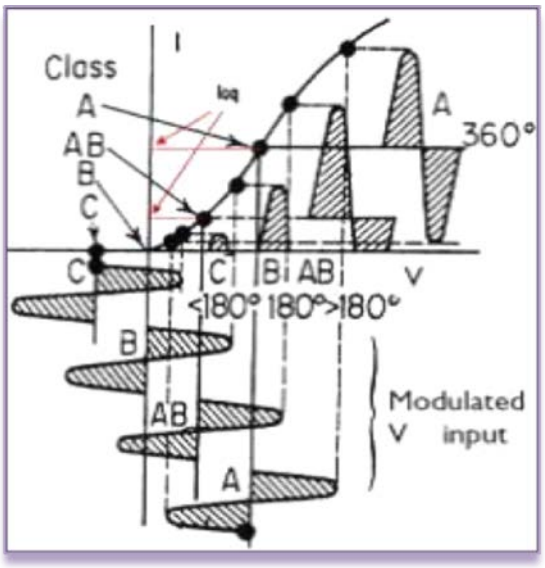


Figure 5.2 power classes

5.3 Power Amplifier Linearity

Inter modulation products result when two or more signals are fed to a single stage.

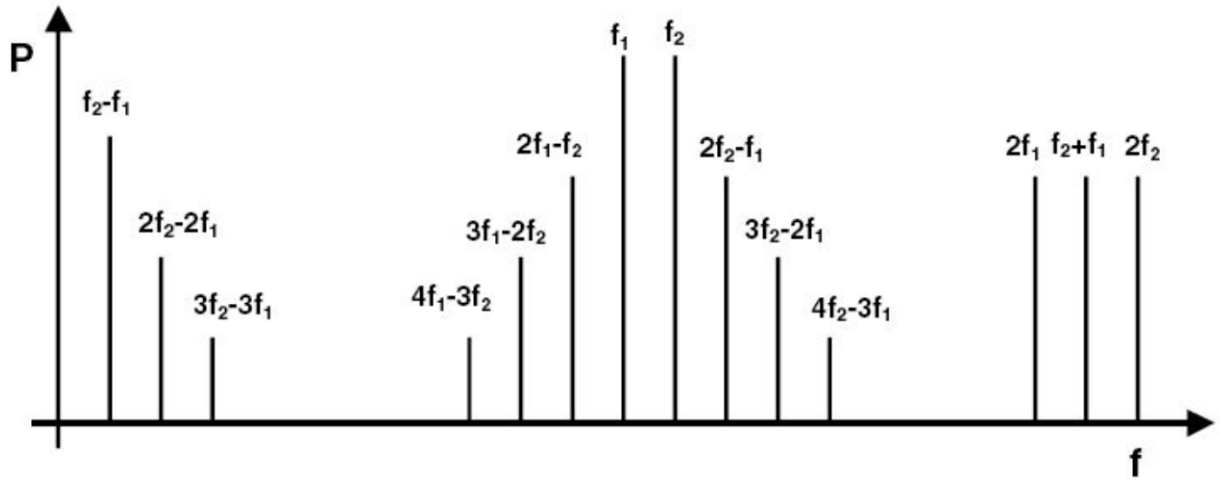


Figure 5.3 Harmonics

In all the Power Amplifiers, the output level is a “compressive” or saturating function of the input level.

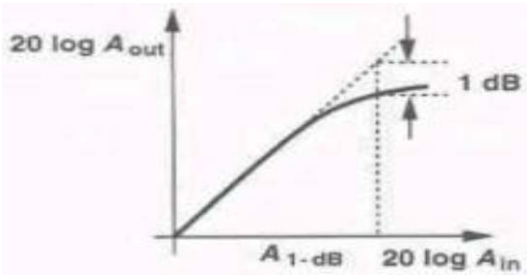


Figure 5.4 1 dB Compression Point

5.4 Input/Output Matching and Load Line

The input matching, including the bias circuit, has an important effect on the operation of the RF Power Amplifiers. The input match will show different optima for maximum gain.

e.g. - if the source impedance is $Zs=R+jX$, then its complex conjugate would be $Zs^*=R-jX$

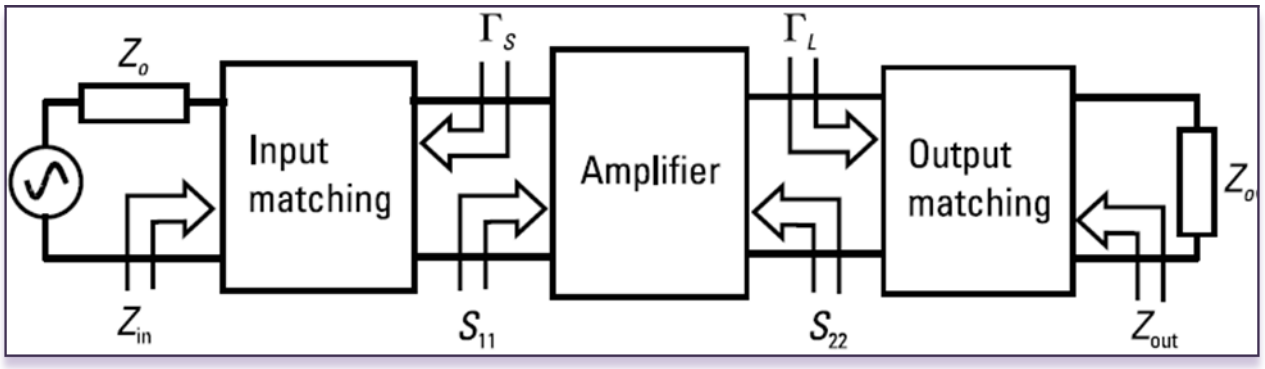


Figure 5.5 Amplifier Topology

If matched: Zin = Zo, Γs = S11*, and Zout = Zo, ΓL = S22*

Matching for maximum Power transfer occurs when Optimum Load impedance (RL) is equal to Source impedance (R gen). Power amplifier is never conjugate matched rather the Rl is varied so that correct voltage and current is fed to the load.

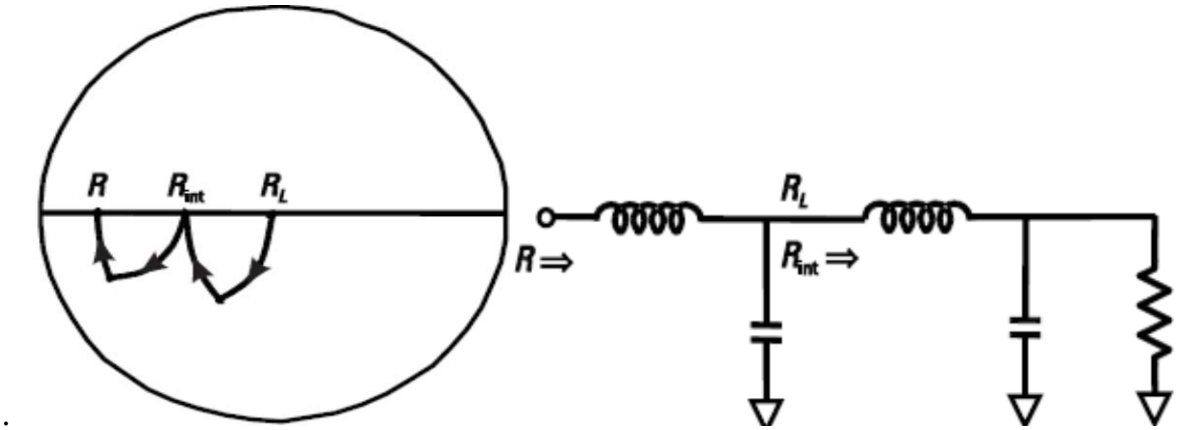


Figure 5.6 Smith chart realization of matching circuits

5.5 Optimum Load Resistance

In the absence of collector output resistance information on the datasheet, it becomes necessary to make a simple calculation to determine the optimum load resistance for the transistor.

5.6 Power FET transistor biasing:

The gate biasing circuit has many functions. Its credibility to maintain constant gate-to-source voltage, Vgs. Ability to provide bias current Igs.

5.7 Design of Power Amplifier for GPS Repeater Assembly

5.7.1 Aim of Power Amplifier

Our design of Power Amplifier was motivated by the fact that in order to provide sufficient gain to the signal, to overcome the various losses that may occur in the cables as well as to provide reasonable input power to the transmitting antenna, we will be required to design a single stage class A amplifier that provides gain, linearity as well as power to the transmitting antenna.

5.7.2 Criteria to be Met

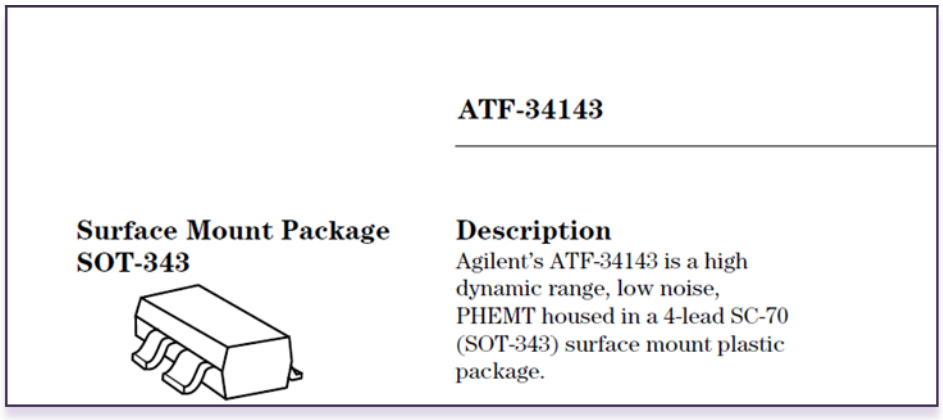
The power amplifier should meet the following criteria

Table 5.1 Characteristics of PA

Frequency	1.573-1.577 GHz
Gain	More than 15 d B
Output Power	More than -120 d Bm
Noise	Less than 2 dB
Stability	Greater than 1
Input vswr Output vswr	Less than -10 Less than -10

5.8 Selection of Device :

Selecting the appropriate device that serves the purpose is very important. For this purpose we downloaded various datasheets and selected the one that best matched our interest. The device selected is ATF-34143, because of its 18d B gain, very low noise figure at the desired frequency. Also , in the datasheet power parameters are provided which suited our requirements just fine at the frequency of operation.



ATF-34143

Surface Mount Package
SOT-343

Description
Agilent's ATF-34143 is a high dynamic range, low noise, PHEMT housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

Figure 5.7 Data Sheet of ATF 34143

ATF-34143 Power Parameters tuned for Power, V_{DS} = 4 V, I_{DSQ} = 60 mA

Freq (GHz)	P_{1dB} (dBm)	I_d (mA)	G_{1dB} (dB)	PAE_{1dB} (%)	P_{3dBm} (dBm)	I_d (mA)	PAE_{3dB} (%)	Gamma Out_mag (Mag)	Gamma Out_ang (Degrees)
0.9	18.2	75	27.5	22	20.5	78	36	0.48	102
1.5	18.7	58	24.5	32	20.8	59	51	0.45	117
1.8	18.8	57	23.0	33	21.1	71	45	0.42	126
2	18.8	59	22.2	32	21.9	81	47	0.40	131
4	20.2	66	13.9	38	22.0	77	48	0.25	-162
6	21.2	79	9.9	37	23.5	102	46	0.18	-77

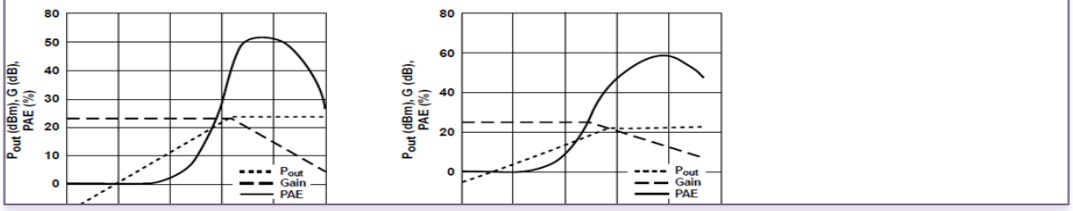


Figure 5.8 Power Parameters

5.9 Design of Bias Circuit

The next important step in the design of PA is the selection of bias point and the design of appropriate bias circuit. The bias point that we selected had following specifications;

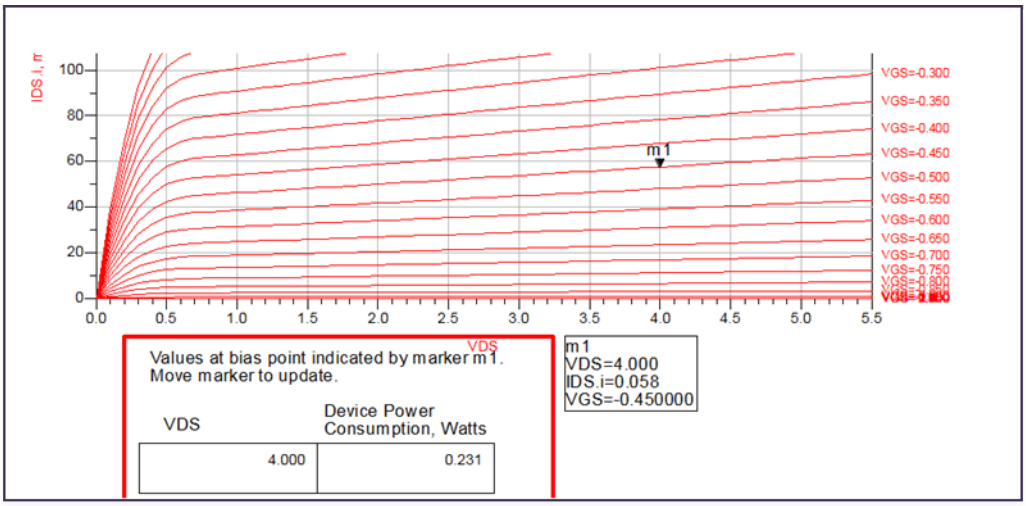


Figure 5.9 DC Curves

Vdd = 5.5V, Vgg = -0.6V
Voltage at drain = 4V
Voltage at gate = -0.4V
Current in drain terminal = 60 m A.

Table 5.2 Bias Point

The selection of bias point is made by analyzing the DC curves, and selecting the point that gives max power while maintain the condition of linearity. The next step is to design an efficient bias circuit that not only provides bias conditions but also to maintain or fix the bias point in case it varies due to external temperature or other such factors. Also, the design of bias circuit incorporates the important concept of load line. As shown in the figure the slope of load line and its starting and ending points determines the range of power input signals that for which transistor will operate to deliver the desired output power. The line here is drawn by adjusting the slope to remain in linear region.

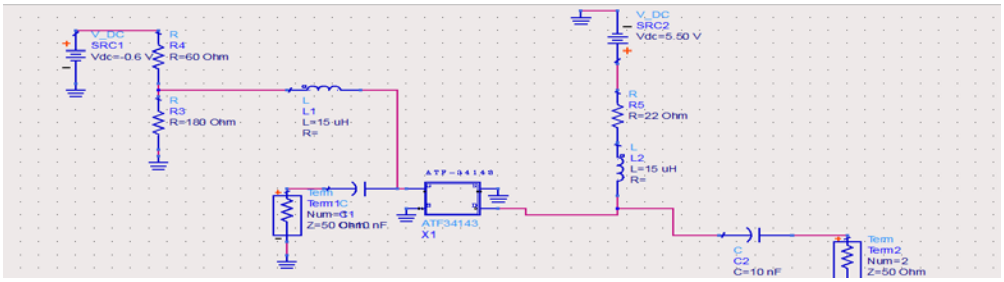
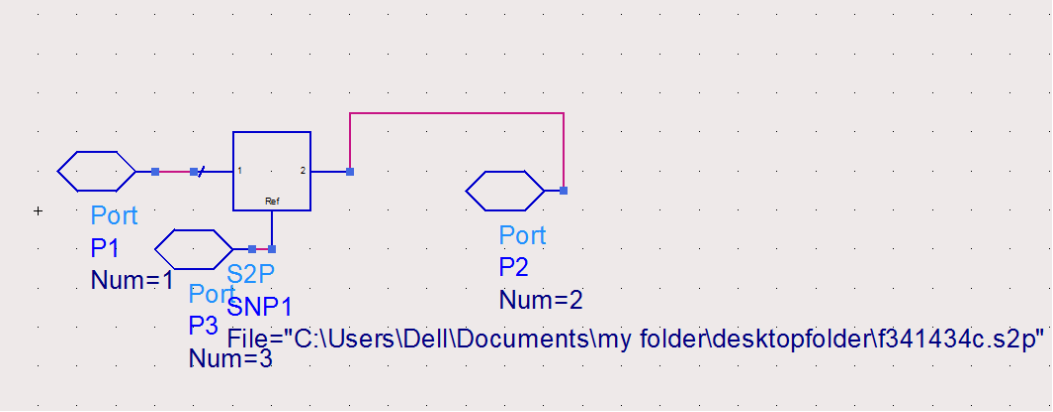


Figure 5.10 Bias Circuit

5.10 Bias circuit equivalent of S2P

The s2p file of a transistor consists of s-parameters of transistor at a particular bias point which are measured with particular bias configuration. We designed an mlin equivalent bias circuit that gave same results as that of s2p file so that instead of using s2p file for designing further circuit we use this bias circuit directly. This step was taken so that nonlinear analysis can be performed which otherwise cannot be performed with s2p file.



5.11 Design of circuit:

We then proceed towards designing of an amplifier circuit that provides the gain of our requirement and at the same time satisfies the condition of stability. The design procedure was

carried out by keeping in mind that we are not only aiming to provide stability at our desired frequency our bandwidth rather unconditional stability is achieved at all the frequencies at which transistor can operate to ensure that no unwanted oscillations are produced that would otherwise cause malfunctioning of the device.

The circuit is optimized to provide stability while the “Max Gain” parameter shows the maximum amount of gain that can be achieved with this transistor topology after adding matching circuits so this value is optimized.

5.12 Design of Mlin circuit:

The circuit shown below consists of Mlin schematic that consists of components’ pads as well. The circuit was designed to cater for all the paristics that are involved in the practical circuit. The value of components was again optimized to meet the required conditions. This schematic along with matching circuits will be used for power/nonlinear analysis of circuit.

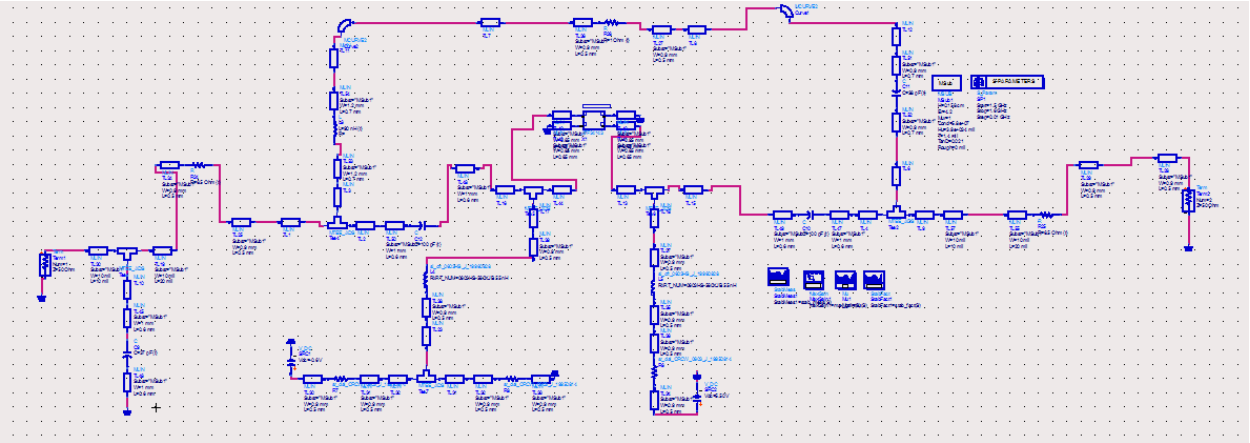


Figure 5.12 Schematic Design

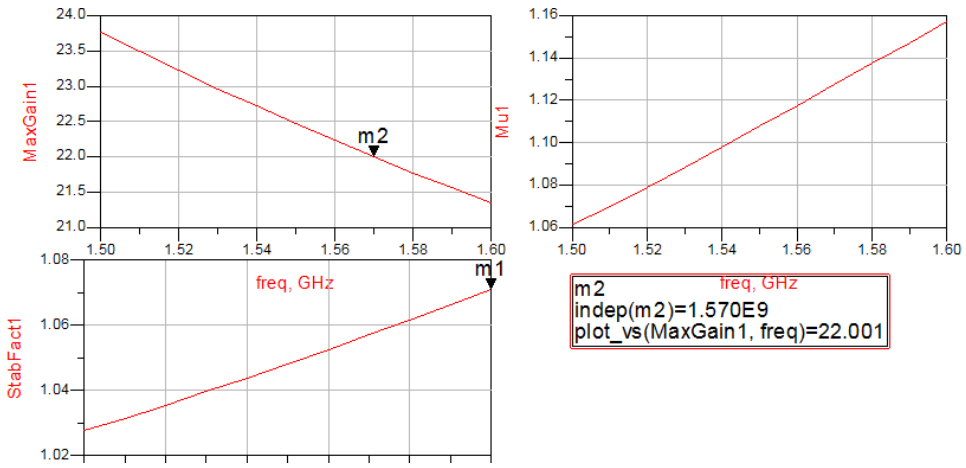


Figure 5.13 The initial schematic results

5.13 Design of matching circuits

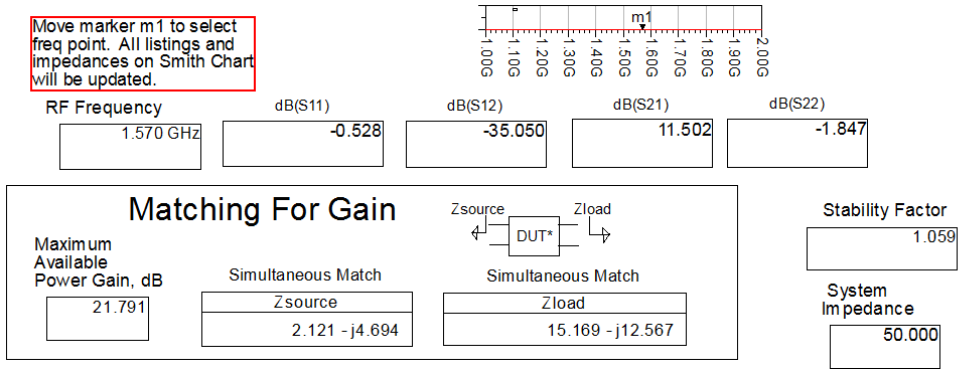


Figure 5.14 Designing matching circuits

Usually for matching circuits we employ the concept of conjugate matching, however in order to obtain max power from the amplifier circuit, a technique called “Load Pull Analysis” is performed. The purpose of this technique facilitates in designing an output matching circuit that provides more power than the conjugate matching. While for the design of input design circuit either matching to 50ohm can be done or Source Pull Analysis is done.

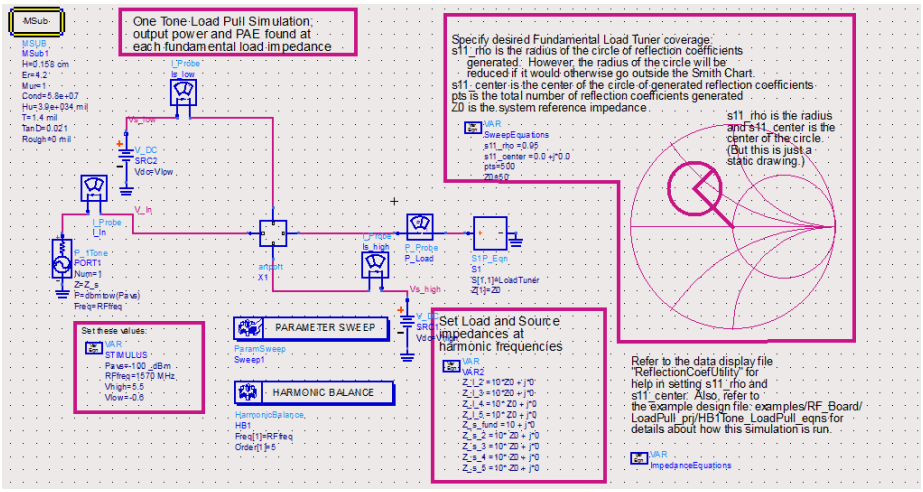


Figure 5.15 Load Pull utility

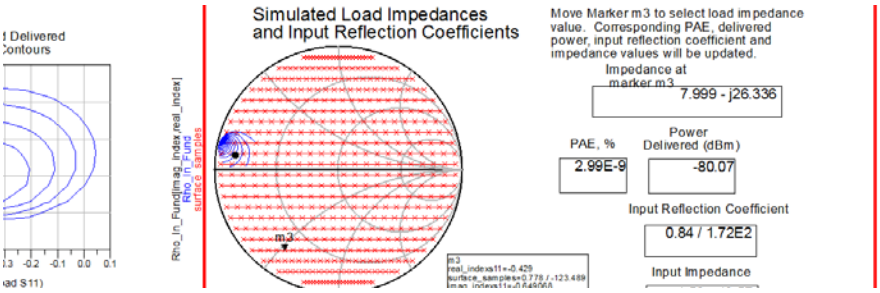


Figure 5.16 Finding the exact matching point

The actual designing of matching circuits is facilitated by an ADS utility Smith Chart and transforming the design into circuit form is facilitated by “LineCalc” utility.

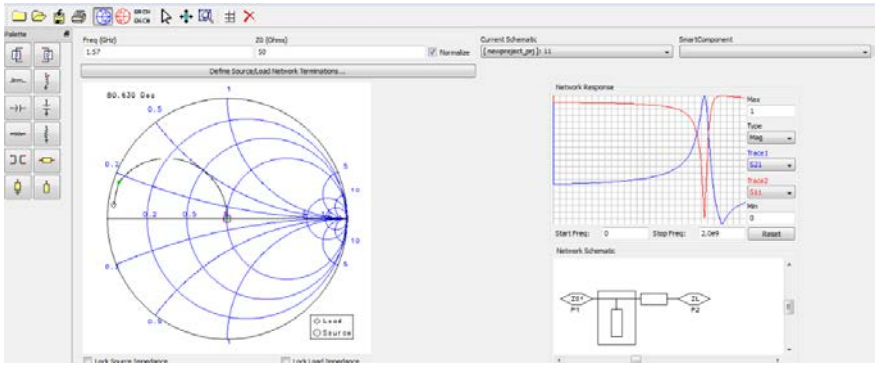


Figure 5.17 Smith Chart Utility

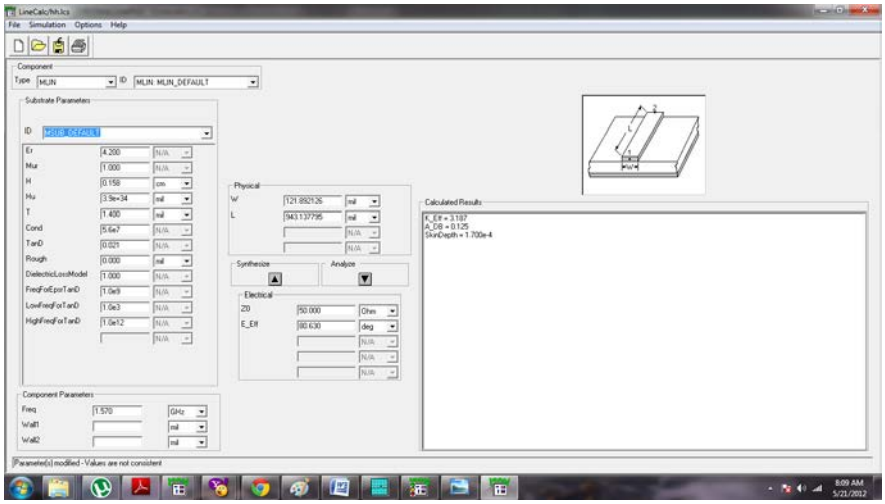


Figure 5.18 Linecalc

5.14 Results after the implementation of matching circuits:

After matching circuits were designed the circuit was finally simulated to see for the results.

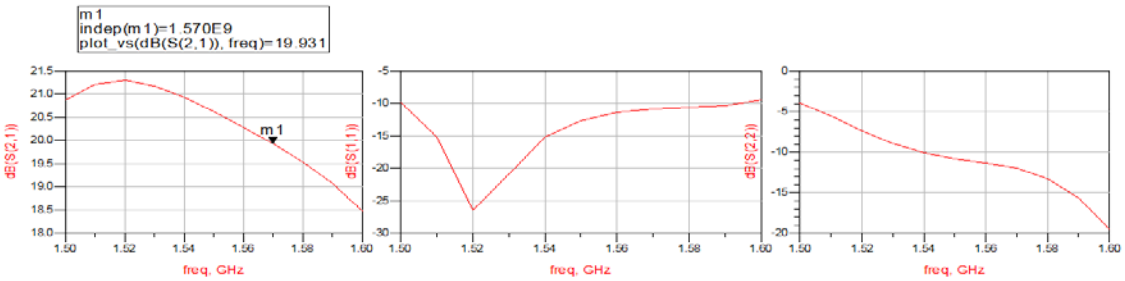


Figure 5.19 Results after matching circuits

5.15 Nonlinear Analysis:

After a complete topology of transistor with matching circuits is obtained, the next step is to carry out nonlinear analysis that includes the data about gain compression point, 1d B and 3d B compression point and the power of the intermodulation products.

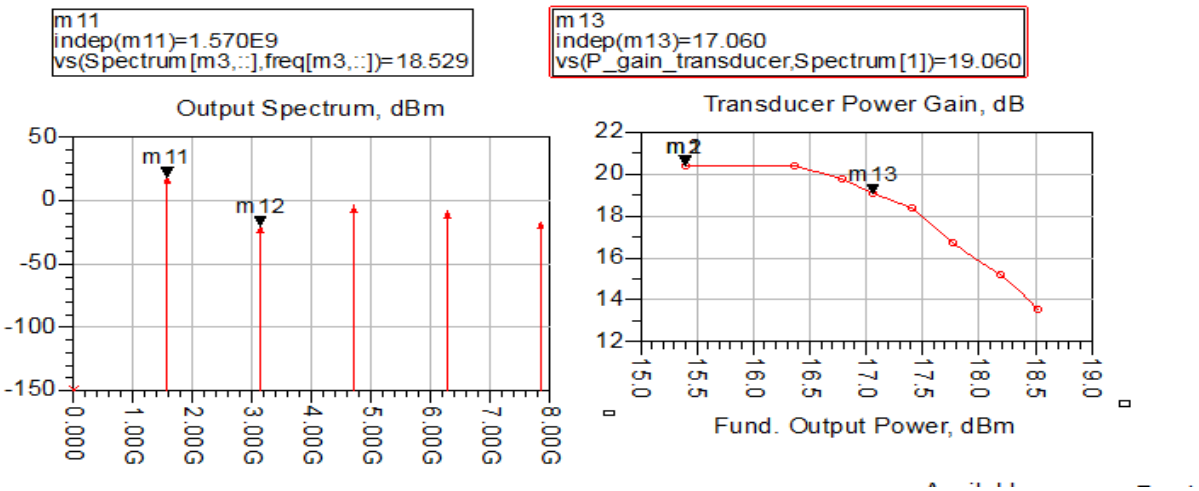


Figure 5.20 Non linear analyses

5.16 Co-Simulation:

In order to carry out the EM analysis of the circuit one has to go through the process of co-simulation , in which the whole circuit is tested in EM environment in order to have accurate insight of how the circuit is going to perform once it is fabricated. For this schematic, the co-simulation process was carried out by defining an equivalent symbol for each and every node, the process of optimization was again carried out.

As can be seen in the results, the max gain that is achievable with co-simulated circuit is 3d B lower than the result achieved from the schematic.

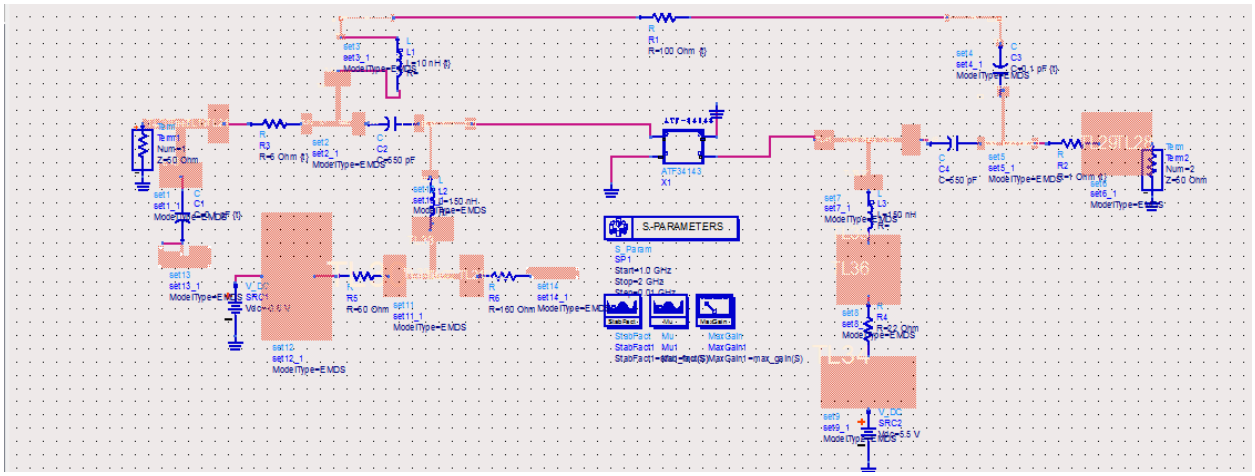


Figure 5.21 Co-simulation

5.16.1 Designing of Matching Circuits for co simulated circuit:

Again the process of load pull analysis is carried out for determining the optimum load impedance and the built-in utilities employed to design the matching circuits.

The final results of Matched co simulated circuit are as follows:

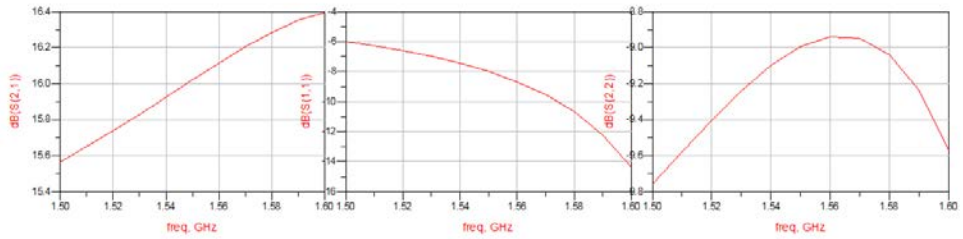


Figure 5.22 Co-Simulation results

5.17 Layout

The final layout of power amplifier in ADS is carried out after seeing and analyzing the co-simulation results.

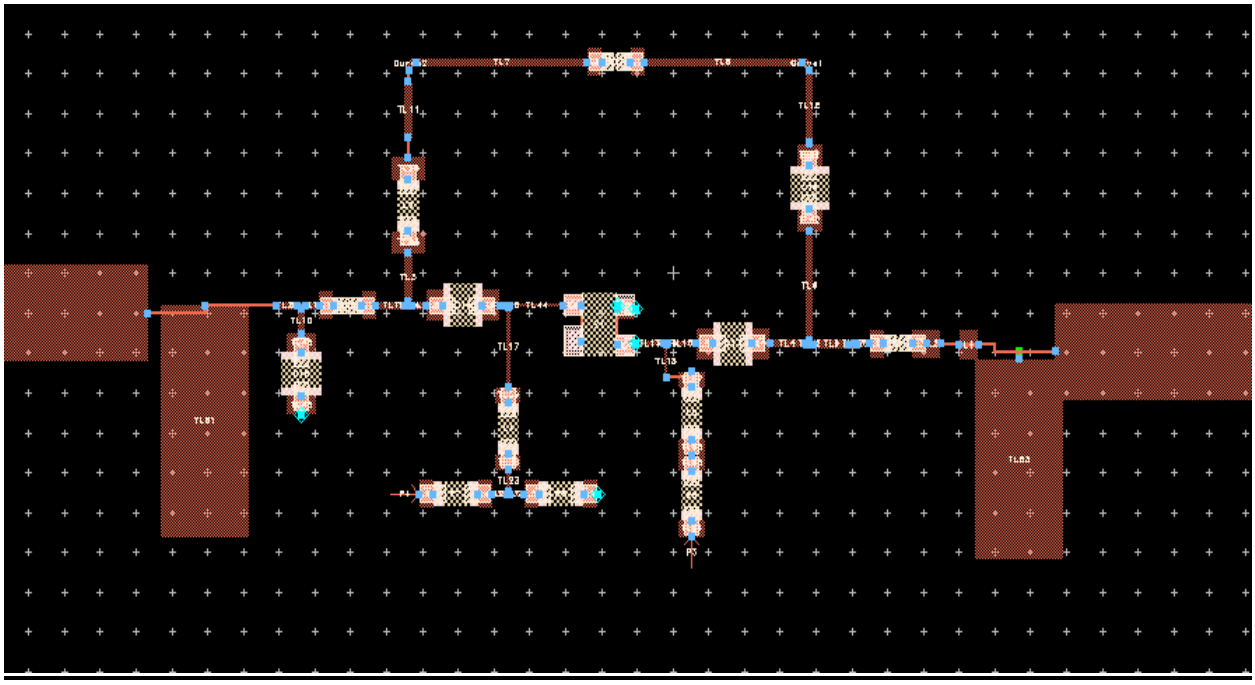
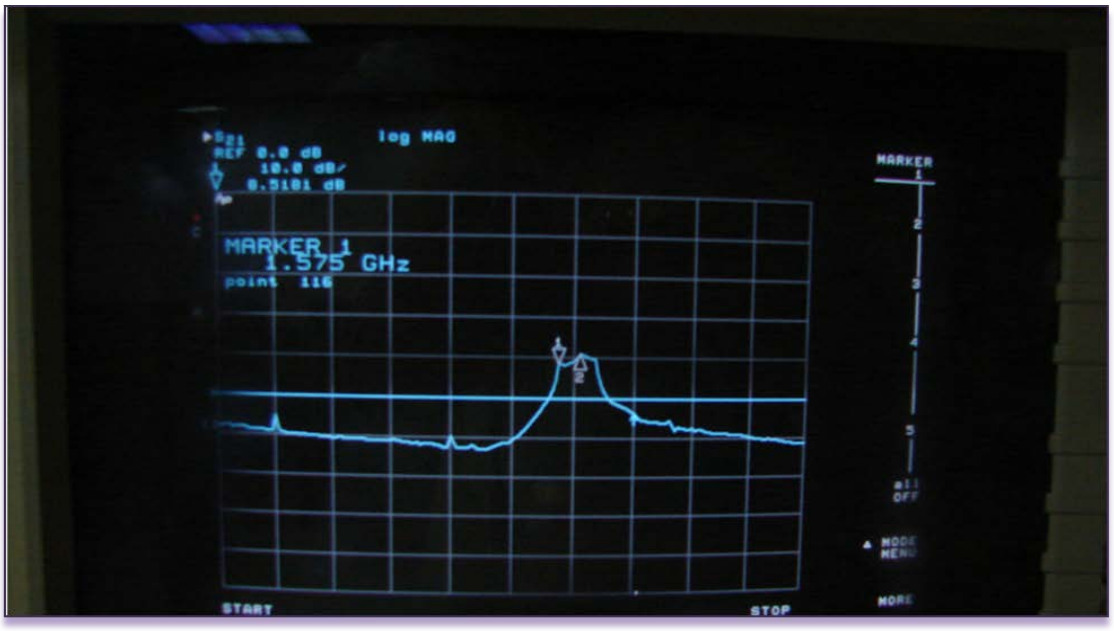


Figure 5.23 The Layout of final PA

5.18 Measurement

The actual practical measurement for the testing purpose of amplifier is carried out by using 50 Ohm SMA connectors as the amplifier circuit was matched to 50 ohm input and 50 ohm output. The attenuators have to be connected for testing the amplifier to avoid it from getting damaged.



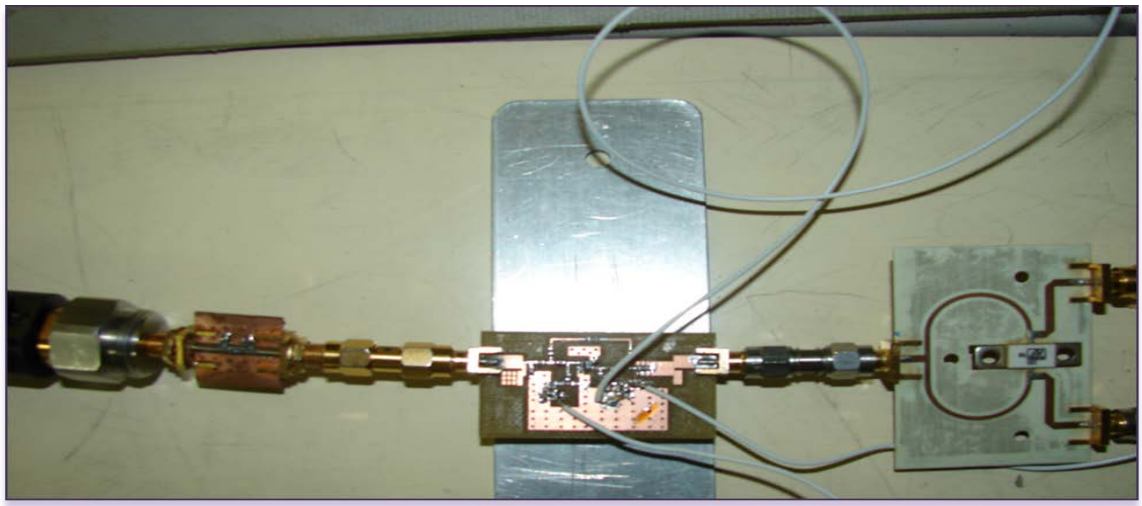


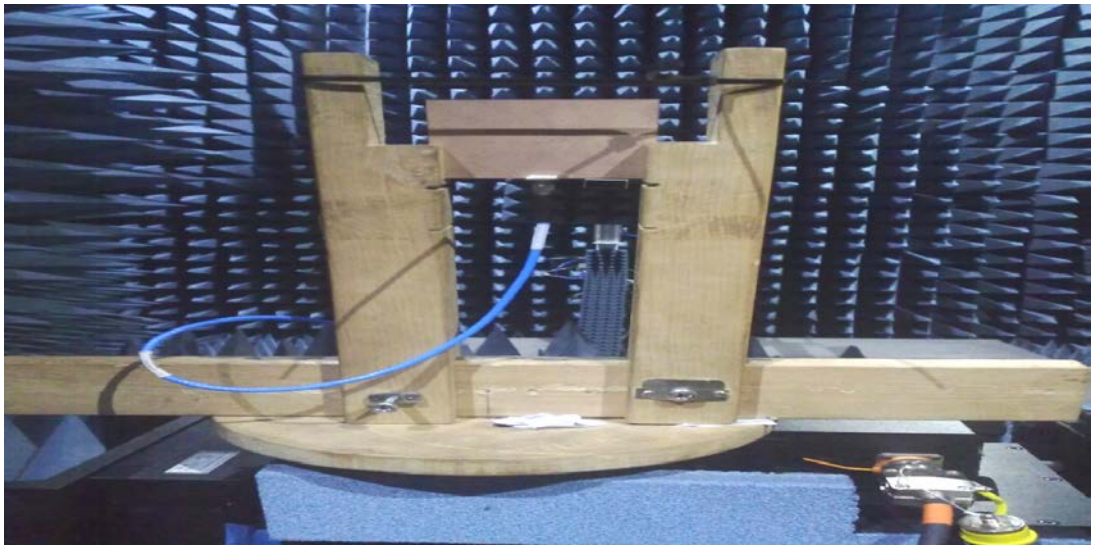
Figure 5.24Measurement

CHAPTER 6

MEASUREMENTS

6.1 Antenna Radiation patterns

The antenna 3D radiation patterns were measured in anechoic chamber at RIMMS institute at NUST H-12 sector.



The antenna results measured in the anechoic chamber are measured practically and they match closely to the simulated results proving the accuracy of the design. The azimuth radiation pattern is practically manifested. The Tx antenna and Rx antenna are in fact the replica of each other.

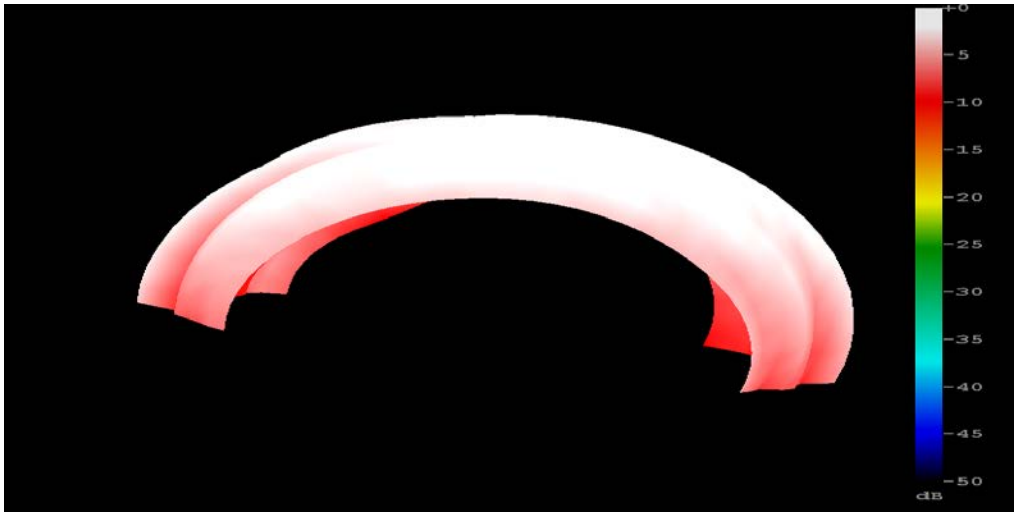


Figure 6.1. antenna results in anechoic chamber (Tx antenna)

6.2 Rx Antenna Radiation pattern

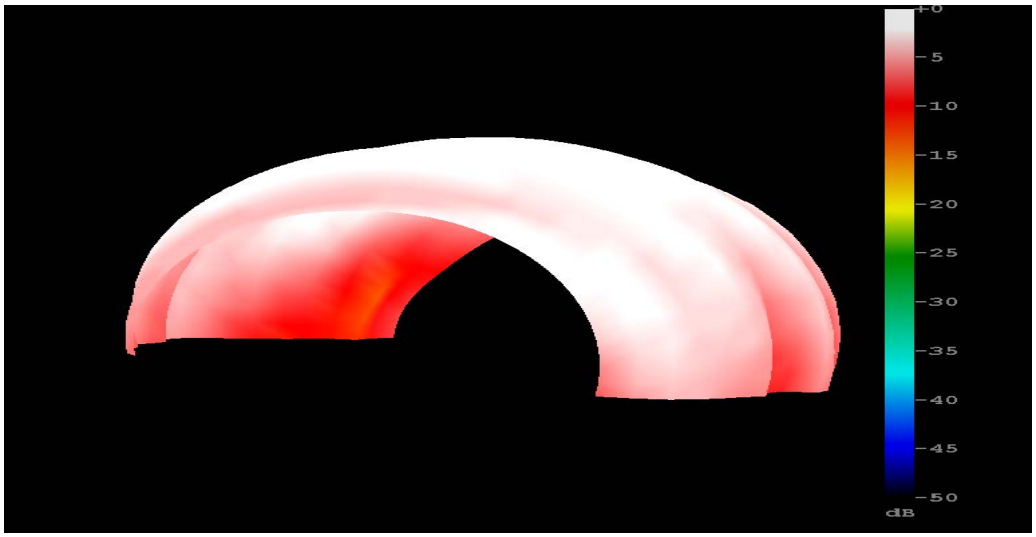


Fig 6.2 Rx antenna

6.3.LNA

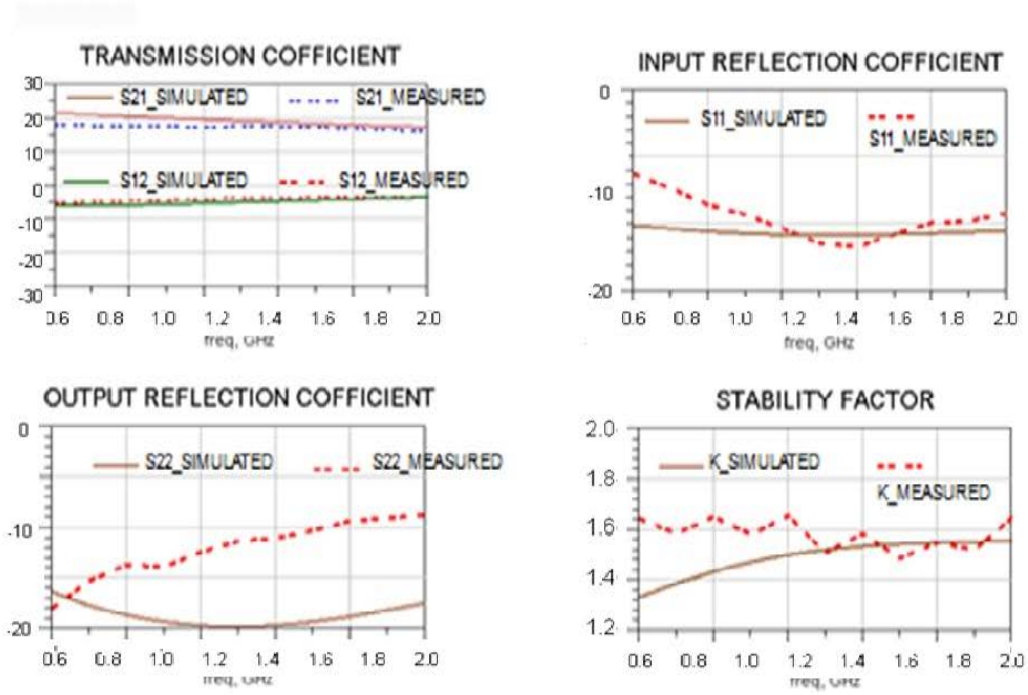
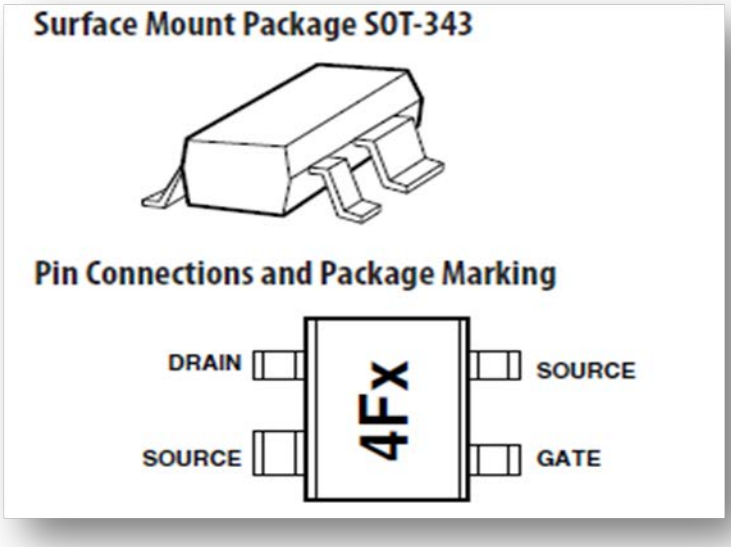


Fig 6.3 LNA Results

APPENDIX

ATF 54143

High gain, linearity, very low noise figure makes it suitable for MMDS and the frequency range from 650 MHz to 4 GHz.



Features

It has high linearity performance. It provides Enhancement Mode Technology. It has a very Low noise figure. It provides with excellent uniformity in all the product specifications and comes with low cost surface mount (SMT) small plastic package SOT-343 (4 lead SC-70). Lead-free option is also available.

Specifications

2 GHz; 3V, 60 mA (Typ.). 36.2 dBm output 3rd order intercept. 20.4 dBm output power at 1 dB gain compression. 0.5 dB noise figure.16.6 dB associated gain

Applications

LNAs for cellular/PCS base stations. It is used for Wireless local loop (WLL).Discrete E-PHEMT for other ultra low noise applications.

Data sheet:

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain - Source Voltage[2]	V	5
V_{GS}	Gate - Source Voltage[2]	V	-5 to 1
V_{GD}	Gate Drain Voltage[2]	V	-5 to 1
I_{DS}	Drain Current[2]	mA	120
P_{diss}	Total Power Dissipation[3]	mW	725
$P_{in\ max.}$ (ON mode)	RF Input Power (Vds=3V, Ids=60mA)	dBm	20 [5]
$P_{in\ max.}$ (OFF mode)	RF Input Power (Vd=0, Ids=0A)	dBm	20
I_{GS}	Gate Source Current	mA	2[5]
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{jc}	Thermal Resistance[4]	°C/W	162

Operation of this device in excess of any one of these parameters may cause permanent damage. Assumes DC quiescent conditions. Source lead temperature is 25°C.Derate 6.2mW/°C for TL > 33°C.Thermal resistance measured using 150°C Liquid Crystal Measurement method. The

device can handle +20 dBm RF Input Power provided IGS is limited to 2mA. IGS at P1dB drive level is bias circuit dependent.

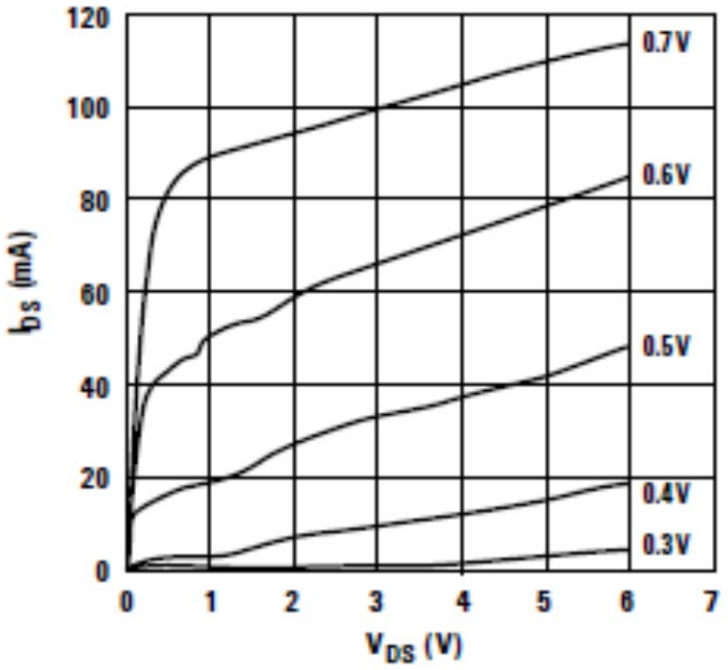


Figure .Typical I-V Curves. (VGS = 0.1 V per step)

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