HIGH POWER AMPLIFIER FOR S-BAND RADAR APPLICATIONS

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THESIS

Submitted to:

Department of Electronic and Power Engineering

Pakistan Navy Engineering College Karachi

National University of Science and Technology, Islamabad Pakistan

In fulfillment of requirement for the award of the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

With Specialization in Communication Engineering


بسم الله الرحمن الرحيم

Acknowledgement

I am very much grateful to Almighty ALLAH, the most merciful and beneficent, whose ample blessings enable us to recognize and pursue knowledge in life. My sincere gratitude to my supervisor Dr. Faisal Amir PN, Assistant Professor, Department of Electronic and Power Engineering at PN Engineering College, NUST. I consider myself very lucky and honored to have him as my supervisor. I thank him for his unprecedented attention and patience throughout the thesis work. I admire him as a teacher and as a person.

In addition to above, I am also thankful to the guidance committee comprising of following faculty members who led me to achieve my target:

- Dr. Tariq MairajRasool Khan
- Dr. Sameer Qazi
- Dr. SajidSaleem

I want to take this opportunity to thank my parents, and sisters. Thank you for your prayers, love, encouragement, patience… Thank you for everything.

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Abstract

Amplifiers are the most common component used in electronics. The use of amplifiers is varied according to requirements of amplification. Amplifiers are available in large number of form factors ranging from miniscale ICs to the largest high power transmitter amplifiers [1].

This thesis presents a SSPA (Solid State power amplifier deign) based on two stages a driver amplifier followed by an isolator and a power amplifier. The RFIC is used for a driver amplifier and GaAs based FET is used for power amplifierin class AB configuration. It forms an efficient design for 10 watt S-band amplifier in the range of 2-2.3GHz. The performance parameters are 52% efficiency with 43dbm gain and 60dbc 2^{nd} harmonic rejection in frequency range of 2-2.3Ghz. The proposed HPA designed and developed product can be used for both S-band radar and LTE applications [1, 2].

Study in microwave device development has enabled Solid State Power Amplifier (SSPA) for use in wireless communication and radar systems.SSPA are replacing magnetrons and travelling-wave tube-based amplifiers (TWTA) for base stations of cellular network using L- and S-band for satellite communication and terrestrial communication base stations of C to Ku band.SSPA's are being in demand in radar systems to increase the detectable range, improve detection of smaller targets and comply with the electronic countermeasure (ECM) requirements [2]. Size and cost is also influencing the use of SSPA's in communication and radar systems as they are improving mobility and portability and are easily installed and mounted. To provide high power output and efficiency for precision radar systems as well as civilian radars for weather observation and air traffic control [2, 3].Power amplifier stage uses a cost effective, linear, high power, reasonable gain FET transistor from Eudyna working in the desired frequency range which makes it a most optimum choice for selection. Also the power amplifier stage has an efficiency of 62% which is better than other power amplifier designs working in this frequency range[3, 4].GaAs technology is employed in high efficiency microwave and millimeter wave radar systems as driver and final stage amplifiers. They are high efficiency but low power so can be used in cascade modes where space limitation is not a requirement [7, 8].Furthermore nonlinearmodeling is performed in the end on similar GaN transistor in the same frequency range which reinforces the design methodology.

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CHAPTER 1

INTRODUCTION

1. Introduction

Power amplifiers are **devices that serve** to increase **the** current**, voltage** or Power of the signal that we want to process. Either it can be used for increasing the level of signal received via receiver or to enhance the signal so that it would be satisfactorily transferred through the transmitter. **So in both cases p**ower amplifiers serves as back bone to strengthen the signals **for better communication** [1, 2].As the power amplifier devices not generates **the** power**,** it **actually** work on the principle of power transfer i.e. it transfers the power from the supply to the signal. **Thus to transfer power with high efficiency is much needed. High efficiency of amplifiers can be attained only if less harmonic distortion is propagated through by the device during amplification. For less harmonic distortion the amplifier needs to be linear. In the current design all these parameters were keep in consideration in order to have an efficient power amplifier design** [2]**.**

1.1 Background

Power amplifier design is a challenging task for designer as it involved trade off the most important parameters like power gain, efficiency and linearity. The designer also decides the general configuration of class of operation and structure of PA which includes cost, size, and thermal limitations. Linearity and efficiency are the most important parameters in PA design and a lot of research is being done to optimize these parameters [1].

In today's third and fourth generation networks, the main issue with any base station is of relatively high power consumption. One reason for this is the complexity of base station due to extensive signal processing. However, the major source which consumes a lot of power in any base station is the power amplifier (PA). Power consumption in PA is due to the low mean

efficiency where the majority of the input power is dissipated as heat. Therefore high efficiency is the primary concern in any RF PA. Thus PA plays a very important role to build efficient transmitter architecture in modern wireless communication systems [1, 2].

Cut of frequency of Si devices is less than the GaAs devices. GaAs has higher breakdown voltages than Si devices. PNPs and FETs are most technological advantage of Si devices over GaAs which are not available in GaAs. Due to this functionality as PNPs and FETs of Si devices, they are used mostly in Power amplification processes. Si devices have efficient thermal conductivity than GaAs which will aid in their ruggedness i.e. in Power amplification processes their mismatch will not causes a lot while GaAs devices will fails due to mismatch phase angles which draws high current then leads to failure because of the poor thermal conductivity of the GaAs substrate [2,3]. Si devices will have one disadvantage that it experiences quasi saturation at higher current densities which will cause bad linearity. GaAs devices have voltage offsets that lead to poor Power added efficiency. Si Devices have lower Noise figure than GaAs devices whereas GaAs devices have lower RxBN than Si devices. Si devices will fails only due to low breakdown voltages. Therefore if we compare both founds that Si devices are more likely to bear realistic austerely performance due to their exceptional thermal properties are exploited by considerable thinning the die [3].

1.2 Motivation

The areas of application related to this research include S-band radars for airborne and space borne platforms, satellite up/down link applications, wireless communication [4].

The topic has been selected to enable the users to avail the benefits of SSPA's for use in both communication and radar applications, with further two tone testing; S-band amplifiers can also be used for LTE communication products. With the trend of multi carrier modulation and high data capacity digital communication High power amplifiers are in strong need for lower distortion communication systems [3]. As compared to tube based amplifiers which have less life, less ability to reduce spurious and unwanted harmonics and greater size and weight solid state power amplifiers are current trend of market and are replacing travelling wave tube amplifiers (TWTA's) in communication systems [4, 5].

1.3 Aim and Scope

All communication-system RF parts include at least one transmitter and one receiver, sometimes called a transceiver. A generic RF transceiver system is shown in Figure 1-1. In the receiver (Rx) path, a receiver signal from the antenna first passes through a band-pass filter (BPF). The BPF attenuates out-of-band signals. The receiver signal then goes through a low-noise amplifier (LNA), which must provide enough gain and at the same time generate a minimum of noise. After the LNA, the signal goes to a down-converter circuit, which shifts the frequency from RF to the baseband. After the baseband amplifier, the signal is fed to the analog-to-digital converter (ADC) [3] [4]. Finally the digital signal is processed by a powerful Digital Signal Processor (DSP). In the transmitter (Tx) path, a digital signal is first fed to a digital-to-analog converter. It then passes through a pulse-shaping block, which can alleviate Inter-Symbol Interference (ISI) due to narrow channel filters. Then an up converter modulates the baseband signal and shifts the frequency from baseband to the RF range [5].

The PA amplifies the RF signal and sends it to the antenna. A good RF designer, therefore, must be familiar with analog circuits and know some digital design as well. General architecture in which a power amplifier works is shown in figure1.1.

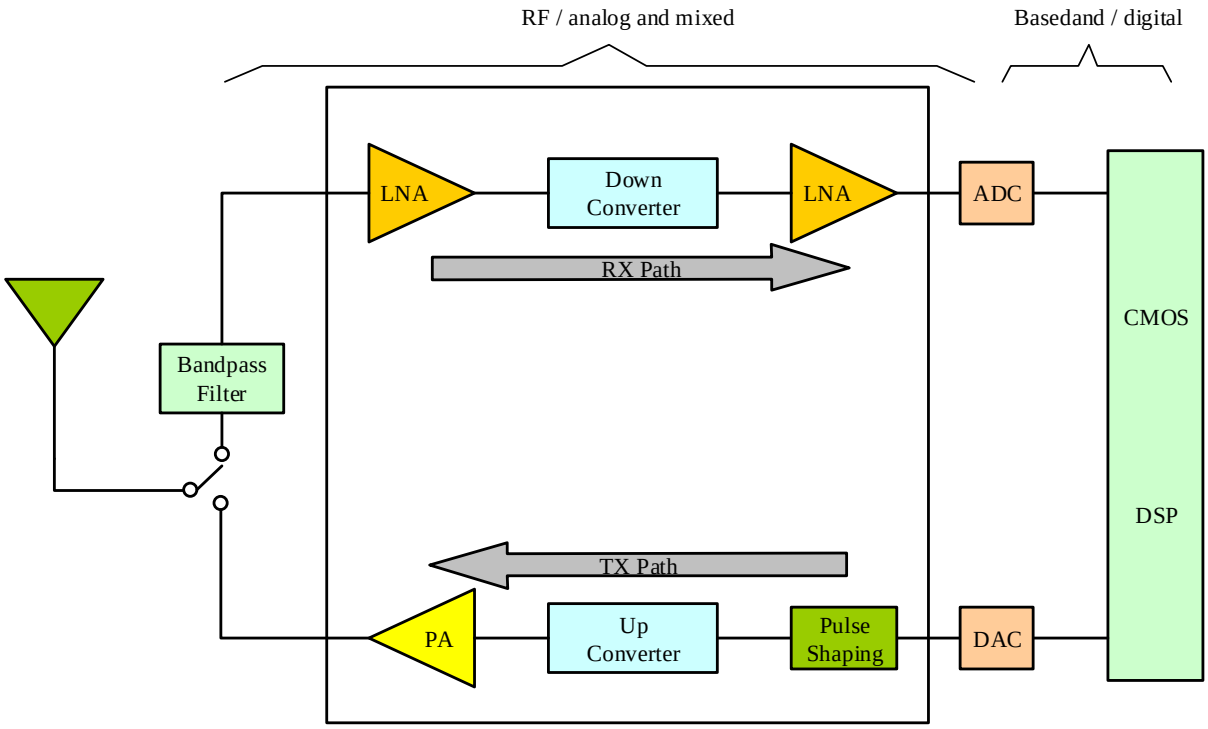

Figure 1-1 Typical Transceiver System showing RF signal transmission (TX) and reception (RX)

Note: the bold box indicates the integrated RF front end

The major commercial RF components still use Si BJT or BiCMOS technology, which provides both BJT and CMOS devices on a single chip. For applications whose working frequencies are greater than 3 GHz, SiGe technology gives better performance. GaAs hetero-junction bipolar transistor (HBT) technology, which provides higher linearity and lower power-consumption characteristics, dominates the PA section. That is by far the hardest part to integrate onto a single chip [6, 7]. A general description of technology used in RF front end is presented in figure 1.2.

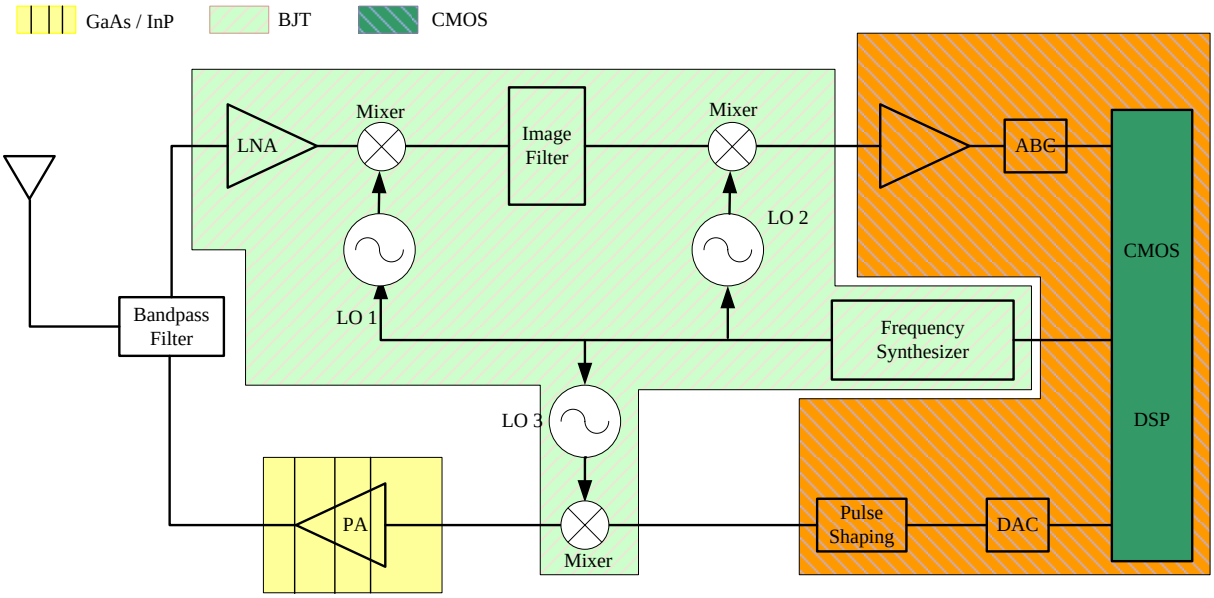

Figure 1-2 Different building blocks in RF front end showing PA, LNA and processing unit

1.4 Thesis Outline

The main objective is to first design the amplifier in Advanced Design System 2011. Stability, S-parameters are calculated in ADS, based on these results amplifier hardware will be designed and tested. For further improvement of results post fabrication tuning will be done through passive tuners or load pull setup if available. The goal is to achieve 52% efficiency with 43dbm gain and 50dbc 2^{nd} harmonic rejection in frequency range of 2-2.3Ghz. As mentioned gain and linearity are the two important factors in HPA's, therefore these two parameters will be tested at different biasing and input power levels. The amplifier is also unique as it will be used for both S-band radar and for LTE applications.

2 Literature Review

2.1 PA design systems and latest technology

The topic has been selected to use previous research on Power amplifiers and pave the way for future development in the field of SSPA's (Solid State Power Amplifiers). To properly analyze the potential of GaAs based FET's for S-band applications. The GaAs FET as a single discrete transistor has been widely used in hybrid microwave integrated circuit (MIC) amplifiers for

broadband, medium-power, high-power, and high-efficiency applications. This wide utilization of GaAs FETs can be attributed to their high frequency of operation and versatility [8, 9].

GaAs amplifiers are used as pre-drivers, drivers, and final stage amplifiers for radar systems that require high efficiency while operating in microwave and millimeter frequencies. GaAs amplifiers operate in the 5V to 28V range. They are high efficiency but low power so can be used in cascade modes where space limitation is not a requirement [8].

The S band range of 2-2.3Ghz also has applications in LTE (Long term Evolution) of UMTS (Universal mobile telecommunication system). Utilizing the gain of S-band amplifier which is 43dbm it can be used in LTE applications. Testing for amplifier for downlink of LTE data can be done by using OFDMA (Orthogonal frequency domain multiple accesses). LTE is a standard and its power amplifiers have certain specifications, by using our amplifier in balanced configuration its bandwidth can be increased and made available for complete LTE frequency band. Rigorous two tone testing is also required to be done for our amplifier to be applicable for LTE applications [5, 9].

The GaAs FET as a single discrete transistor has been widely used in hybrid microwave integrated circuit (MIC) amplifiers for broadband, medium-power, high-power, and high-efficiency applications. This wide utilization of GaAs FETs can be attributed to their high frequency of operation and versatility [7].

S-band (2-2.3GHz) has wavelength in the range of 8-15cm which is not easily attenuated by rain and oxygen molecules. Previous work has suggested that in S-band rain attenuation is negligible but heavy rains can offer up to 0.22dB/km of attenuation. This negligible attenuation in average weather conditions makes S-band an ideal choice for weather observation [8, 9].

2.2 GaAs Power Devices

All the power amplifier designs discussed in this dissertation is done using GaAs power FET devices; therefore, in this sub-section, the fundamental concepts in a GaAspower device are reviewed. GaAs FET has higher flexibility with lower NF, and is a very mature technology. Two figures of merit that are commonly used to describe microwave transistor performance [10, 11]:

1. Maximum cutoff frequency (f_t): It is the frequency where the short circuit gain approximates unity; ft is a measure of certain internal transistor parameters that affect high-frequency performance. A transistor with higher f_t can achieve good high frequency noise performance.

2. Maximum available gain frequency (f_{max}): It is the maximum frequency of oscillation. It is the frequency where the maximum available power gain of the transistor is equal to 1. As in the case of f_t, f_{max} is calculated from the equivalent circuit of the device. Equivalent circuit that used to derive f_{max} include parasitic elements, thus f_{max} is a much better parameter to describe the performance capability of a FET.Today, the state-of-the-art GaAs FET has f_t and f_{max} are around 22 GHz and 110 GHz, respectively.

2.3 Designs in Literature

Designs described in different literature are described below:

2.3.1 An 8 W GaAs Class-AB Amplifier for Operation in Envelope Tracking Systems [31]

In this paper an 8 W GaAs HEMT power amplifier for operation in envelope tracking systems is presented. The application targeted is UMTS downlink operation with a peakto-average ratio of about 7 dB. By varying the drain bias voltage between 5 V and 12 V the compression point can be 52 % in the area of average output power of a UMTS signal. Gain can be kept above 14 dB in this operation mode with a variation of 3 dB.

2.3.2 LTE Power Amplifier Module Design: Challenges and Trends [32]

Long Term Evolution (LTE) provides a high data rate, high quality and low cost solution for the cellular industry facing an overwhelming increase in mobile data traffic. Beginning with an overview of LTE UE transmitter requirements, authors examine the key challenges for the Power Amplifier Module (PAM) from the perspective of designers, and review current development activities. Then, trends are predicted in architecture design as wells device and technology development.

2.3.3 Broadband S-band Class E HPA [33]

A broadband class E High Power Amplifier (HPA) is presented. This HPA is designed to operate at S-band (2.75 to3.75 GHz). A power added efficiency of 50% is obtained for the two stage amplifier with an output power of 35.5 dBm on a chip area of 5.25 x 2.8 mm^2.

2.3.4 Novelty of the current proposed research work

The research included in this thesis presents state of art GaAs transistor used for designing a high efficiency power amplifier for a frequency range of 2-2.5GHz. High gain was also targeted and numerous iterations were performed to achieve 62% efficient and gain of 10dB. Furthermore amplifier is tested for third order intercept point which is also found to be 10dB greater than then the maximum power output. Hence the research work provides a high gain, high efficiency, linear gain power amplifier for S-band radar as well as LTE applications.

2.4 Thesis Organization

Chapter 2: Gives the brief overview to the relevant literature that helped me in depth understanding and achievement of the goals in this thesis.

Chapter 3: In this chapter we have discussed the High power amplifier design characteristics

Chapter 4: HPA Model development and simulations in ADS are shown and discussed

Chapter 5: Design of power amplifier is presented in ADS 2011 and its optimization is shown

Chapter 6: Two Tone Testing measurements are performed and TOI intercept point is presented.

Chapter 7: Conclusion is presented in last to present overall approach presented in this thesis and future work proposed

CHAPTER 2

BACKGROUND THEORY OF POWER AMPLIFIERS

3 Power Amplifiers

3.1 Efficiency Analysis

The Figure of merit of a PA design is output power, gain, linearity and efficiency. However efficiency can be characterized into different metrics which are the output efficiency, power-added efficiency and overall efficiency of the amplifier. The output efficiency of power amplifier is referred to as the drain/collector efficiency. It can also be defined mathematically by the ratio of the output RF power and the power drawn from the DC supply [3, 4].

$$\eta = \left(\frac{\mathbf{Pout}}{\mathbf{Pdc}}\right) \qquad \textbf{3-1}$$

Where,

$\mathbf{P_{out}}$ is the RF power delivered to the load (refer to fundamental frequency) and

$\mathbf{P_{dc}}$ is the total dc power drawn from the DC power supply.

Power Added efficiency (PAE) is the real efficiency performance of the power amplifier. PAE is defined as:

$$\mathbf{PAE} = \frac{(\mathbf{Pout} - \mathbf{Pin})}{\mathbf{Pdc}} \qquad \textbf{3-2}$$

Where:

$\boldsymbol{P_{in}}$ is the input (drive) power

$\boldsymbol{P_{out}}$ is the output power (referred to fundamental frequency)

Pdis the total power drawn from DC supply.

From (2.1), substitute ***Pdc***on (2.2) and can be expressed as shown in (2.3).

$$\mathbf{PAE} = \frac{\mathbf{Pout-Pin}}{\mathbf{Pdc}} = \frac{\mathbf{Pout}}{\mathbf{Pdc}}\left(\mathbf{1} - \frac{\mathbf{Pin}}{\mathbf{Pout}}\right) = \boldsymbol{\eta}\left(\mathbf{1} - \frac{\mathbf{1}}{\mathbf{Gp}}\right) \qquad \textbf{3-3}$$

Where: equation2-3 is the output efficiency of the PA,

Gpis the power gain, given by G_P = Pout/Pin.

Another Efficiency measurement is the overall efficiency. It is the overall efficiency performance of power amplifier and is defined as the ratio of the output power(refer to fundamental) over the total power fed into the PA.

$$\boldsymbol{\eta_{Overall}} = \frac{\boldsymbol{Pout}}{(\boldsymbol{Pdc+Pin})} \qquad \textbf{3-4}$$

From equation 2.1 and 2.2, it can be seen that when the amplifier gain is high, such as in the case of multistage amplifier, PAE is almost the same as the drain efficiency.

In general, PAE is a better efficiency measurement parameter. Unlike drain efficiency, PAE doesn't discriminate against low-gain amplifier in which a significant fraction of the output power comes from the RF input power [5].

3.2 Classes of Amplifier

Power amplifiers are classified according to conduction angle which defines the working of a amplifier. Common classes of amplifiers are A,B and C class which depends on the conduction angle of the drain current. A PA working as dependent current source can be shown by the its drain current waveform in figure 2.1[2, 3].

The DC Q point of an amplfier is an important factor of an amplifier design which determines the class in which the amplifier will operate. Various classes at microwave frequencies are defined as A,B, AB, C,D,E and F. The selection of class a solely depends on the application for which the amplifier has to be used, biasing network is used to set the quiscent Q-point for active

devices, and it maintains the constatnt setting irrepectivbe of change of transistor paramters varaiations and temperature fluctuations [4]. Current waveforms for different classes of amplifier are shown in figure 2.1

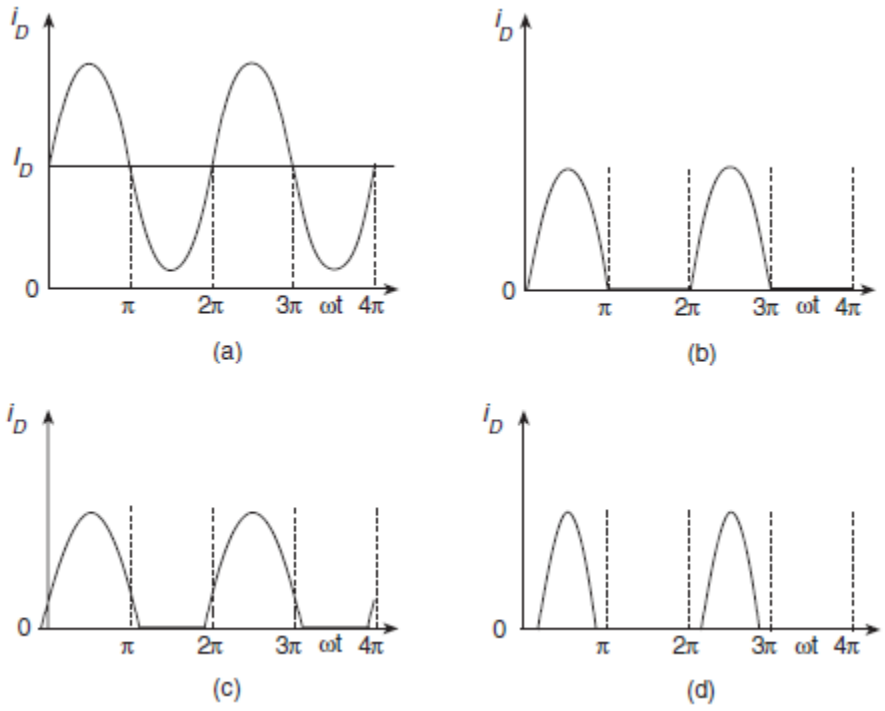

Figure 3-1 Waveform of current Id in various classes of PA(a)Class A(b)Class B(c)Class AB(d)Class C [3]

These classes of Amplifiers are discussed further in following section:

3.2.1 Class A Amplifiers

For the input signal in class A the transistor operates in active region at all times and works as a current source controlled by the input signal. Class A amplifier has a conduction angle of 360^o. It conducts for the complete cycle and has a maximum efficiency of 50%.

3.2.2 Class B Amplifiers

For the class B, transistor is biased at the edge of cut-off. Unlike class A the power dissipation in the absence of signal is zero. The transistor works for the half of input cycle making a conduction angle of 180^o. Maximum efficiency in class B amplifier is 78.5%.

3.2.3 Class AB Amplifiers

In Class AB, the transistor is biased slightly above cut-off. In this case, the conduction angle 2θ is between 180° and 360°, and the term Class AB is used for the amplifier.

3.2.4 Class C Amplifiers

In Class C, the transistor is biased in the cut-off region and for only a portion of input signal, which is less than 180°, acts as a current source. Assuming a sine-wave input, the output current is tips of a sine-wave.

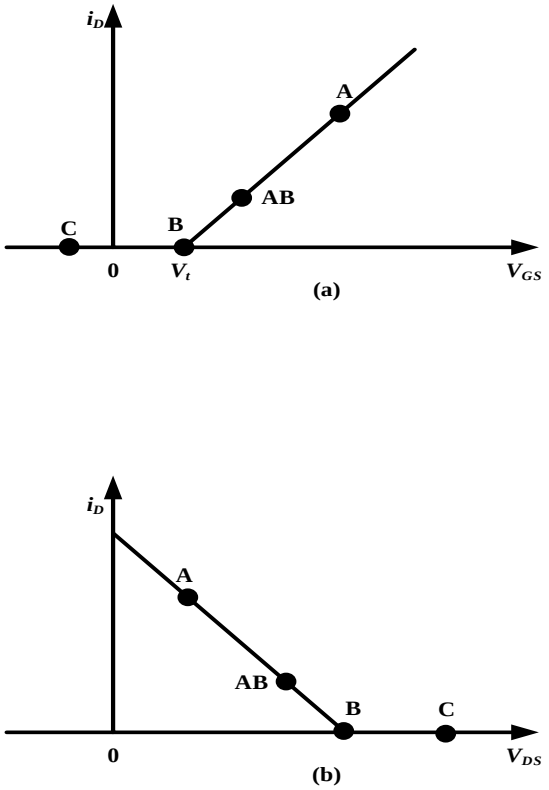

Figure 3-2Operating points for various Classes of PA [3]

A brief summary of all power amplifier classes is described in Table 2.6-1

Table 3.2-1 PA Classification

Class	Mode	Conduction	Output	Maximum	Gain	Linearity

		Angle ϕ	**Power**	**Efficiency**		
A	Current Source	100%	Fair	50%	Large	Good
AB		B<ϕ<A	Fair	A<η<B	Large	Fair
B		50%	Fair	78.5%	Fare	Fair
C		<50%	small	100%	small	Poor
D	Switch	50%	large	100%	small	Poor
E		50%	large	100%	small	Poor
F		50%	large	100%	small	Poor

The operating point for various classes of operation is shown in Fig. 2.2

4 HPA Design characteristics

4.1 RF Amplifier Design Procedure

The selected device is checked for stability and maximum gain. Apart from specialized Power Amplifiers the general design methodology for HPA is quite common. The first and foremost step is to evaluate Rollet's Stability factor to define the frequencies at which the device is stable and to check the stability of device at required frequency [5]. Biasing conditions are different for different classes of Amplifier so it is required to find the ideal bias conditions. Stability circles should be realized on Smith chart reflecting the source match and load match calculated. Strict consideration should be taken in account for the position of source match in relation to stability circles [6].

Analysis of factors affecting RF PA design is discussed in the following section.

4.1.1 Condition for maximum efficiency

The average drain efficiency of PA as described in equation (1.1) can also be written as:

$$\eta = \frac{P_{\text{out,RF}}}{P_{\text{in,DC}}} = \frac{P_{\text{DS}}}{P_{\text{in,DC}}} = 1 - \frac{P_{\text{D}}}{P_{\text{in,DC}}} \quad \text{4-1}$$

The condition for achieving 100% average efficiency is:

$$P_{\text{D}} = \frac{1}{T}\int_0^T i_D V_{DS} dt = 0 \quad \text{4-2}$$

or

$$i_D V_{DS} = 0 \quad \text{4-3}$$

Thus the waveform for i_D and V_{DS}should be non-overlapping for achieving an efficiency of 100%, at-least in theory.

Such non-overlapping waveforms are possible in switching amplifiers classified as D and E. In these Classes, the transistor acts as a switch and not a current source. Since an ideal switch has either zero voltage across it or zero current though it, the switch dissipates no power. Therefore, switching classes of amplification have an efficiency of 100% in the ideal case [5, 6].

The Class D amplifier is similar to an inverter gate with a series tuned circuit connecting its output to the load. The input signal toggles the output of the gate and generates a square waveform which is filtered by the tuned circuit, and a sinusoidal waveform appears across the load. The on-resistance of the transistors reduces the efficiency from its ideal 100%.

Class E amplifiers have a single switching transistor connected to a passive load network. Because Class E uses capacitance shunting across the switch to shape the voltage and current waveforms, it avoids the power loss due to charging and discharging the capacitance, thus, achieving a better efficiency than Class D at high frequency. Class E is also less sensitive to the transition time of the switch than Class D [5, 6].

The efficiency is defined as a ratio of the generated RF power and the drawn DC power.

$$\boldsymbol{\eta = \frac{P_{out,RF}}{P_{in,DC}}} \quad \textbf{4-4}$$

Where, $P_{\mathrm{out,RF}}$is the output RF power

$P_{\mathrm{in,DC}}$is the applied DC power and η represents the efficiency.

Another figure of metric (FOM) is the power added efficiency (PAE) which is also used to measure the performance of PA and is defined as the ratio of the difference between the output power P_{out} and the input power P_{in} to the dc supply powerP_{dc}.

$$\mathbf{PAE} = \boldsymbol{\frac{P_{out}-P_{in}}{P_{dc}}} \quad \textbf{4-5}$$

High efficiency is required for low energy consumption, a longer battery lifetime and thermal management. The efficiency of conventional linear RF PAs varies with the signal amplitude (envelope), resulting in relatively low average efficiencies, especially when the peak-to-average ratio (PAR), which is defined as the ratio of the peak power to the time-averaged power of the signal, is high.

$$\boldsymbol{C = \frac{P_{peak}}{P_{avg}}} \quad \textbf{4-6}$$

where $P_{\mathrm{peak}}$is the peak power, P_{avg} is the time-averaged power of the signal and C is the peak to average ratio. For example, for a Rayleigh-envelope signal with a 10-dB peak-to-average ratio, the average efficiencies of ideal class-A and –B PAs are only 5 and 28 percent, respectively.

Another very important property which defines the performance of any PA is the linearity. Linearity is required for achieving less distortion in amplified output signals and also to minimize interference and spectral re-growth. Many modern applications that use shaped-pulse data modulation or simultaneously transmit multiple carriers require linear RF power amplification. Linear class A or class AB PAs are used to achieve high linearity, which, contrary, yields low average efficiency [5].

Therefore, the design of linear and efficient radio frequency PAs presents one of the most challenging design problems in modern telecommunication systems when using spectral efficient modulation schemes such as WCDMA, OFDM and new standards such as LTE.

The efficiency and linearity of PAs can be increased in many ways. The architecture of PA can be classified into two categories. The linear mode amplifiers and switch mode amplifiers.

Linear amplifiers can be combined in many ways. Recently various techniques for high-efficiency linear amplification (e.g. Chireix and Doherty) have been developed, but all are subject to limitations in bandwidth or the dynamic range over which the efficiency is improved. In Doherty two or more amplifiers are connected in a parallel like configuration with a main and peak amplifier. By the proper combining of the amplifier branches the impedance seen by each amplifier for different power levels is beneficial to efficiency, compared to a single transistor amplifier [6].

Alternatively, the DC supply voltage of PA can be changed to keep the transistor working closer to saturation for different output levels. The technique used in Envelope Tracking (ET) is based on this principle. In ET, the DC supply voltage follows the envelope of the signal.

In order to reach very high efficiency figures, switch mode amplifiers can be used such as envelope elimination and restoration (EER). In EER, the maximum output power is changed by adjusting the drain DC voltage, while the transistor still kept working in saturation. But, EER has several short comings such as phase distortion introduced by non-linear transistors and by limiters [3, 4].

4.1.2 Unilateral Condition

A transistor is unilateral if S_{12} is zero or very near zero when compared to the other S-parameters of its scattering matrix. From the S matrix that we determined for the Free-scale transistor, the S_{12} term is very small and can be set to 0 to simplify our amplifier calculations. With this assumption, there will be no internal feedback [4, 5]. This means the input resistance will be independent of the load resistance, and the output resistance will be independent of the source resistance [3, 4]. This will make designing the source and load matching networks easier. For example, the output matching network would see R_{ds} looking into the output of the transistor and

if the manufacturer of the transistor would make R_{ds} = 50 ohms, then a matching network would be minimal.

4.1.3 Stability

A successful amplifier design requires a number of characteristics to be met including voltage gain, power gain and linearity, but perhaps the most critical aspect of any amplifier is stability. Even if a design produces excellent gain and linearity, if it is unstable it is essentially unusable. For this reason it was vital for us to consider stability through every step of the design process. Stability of an amplifier is its immunity to causing spurious oscillations. In the case of high-frequency amplifiers, there are two types of stability defined: conditional stability and unconditional stability [5, 6]. If an amplifier is conditionally stable, it is shown to be stable with both ports properly terminated (that is, with the intended source and load impedances). A much better result is unconditional stability, which shows that an amplifier is stable regardless of input and output impedances. In our analysis we sought to determine unconditional stability for this amplifier design. If the transistor is not unilateral the following conditions must be met to determine unconditional stability:

$$|\boldsymbol{\Gamma_{in}}| = \boldsymbol{S_{11}} + \frac{\boldsymbol{S_{12}S_{21}\Gamma_L}}{\boldsymbol{1-S_{22}\Gamma_L}} \qquad \textbf{4-7}$$

And,

$$|\boldsymbol{\Gamma_{out}}| = \boldsymbol{S_{22}} + \frac{\boldsymbol{S_{12}S_{21}\Gamma_s}}{\boldsymbol{1-S_{11}\Gamma_s}} \qquad \textbf{4-8}$$

To facilitate the determination of this key factor, we needed to first establish that our circuit was unilateral; that is, signal flows only in the forward direction or, equivalently, S_{12} (transmission from port 2 to port 1) equals zero. If the unilateral condition is met, calculations required for unconditional stability determination simplify greatly, requiring only two conditions. These are:

$$|\boldsymbol{S_{11}}| < 1 \qquad \text{and} \qquad |\boldsymbol{S_{22}}| < 1$$

To determine the stability of the circuit we needed to examine the magnitude of input and output reflection coefficients as various parameters of the circuit were varied to find if any condition

existed which would cause either of these magnitudes to exceed unity [3] [4]. For Rollet stability criteria stability factor (k) must be greater than 1 and stability measure (b) must be greater than 0.

Where K and b are:

$$\boldsymbol{K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}||S_{12}|}} \qquad \textbf{4-9}$$

$$\boldsymbol{b = 1 + |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2} \qquad \textbf{4-10}$$

If the stability analysis of k and b shows that the device is potentially unstable then the unstable regions for matching on the smith chart need to be identified and avoided in design. To do this the unstable regions for the source and load reflection coefficients, o_s and r_L need to be identified. So two reflection coefficient planes need to be considered, corresponding to the input and the output.

Firstly considering the input reflection coefficient, r_L the boundary between the stable and unstable regions is defined by the locus of i_L for $|r_L| = 1$. For these conditions C_L and radius R_L where,

$$C_L = \frac{S_{22}^* - \Delta^* S_{11}}{|S_{22}|^2 - |\Delta|^2}$$

$$R_L = \frac{S_{12}\, S_{21}}{|S_{22}|^2 - |\Delta|^2}$$

Similarly the boundary between the stable and unstable regions for r_s, Corresponding to $|r_{OUT}| = 1$ is again a circle on the smith chart with center $C_s$and radius $R_S$where

$$C_s = \frac{S_{11}^* - \Delta^* S_{22}}{|S_{11}|^2 - |\Delta|^2}$$

$$R_L = \frac{S_{12}\, S_{21}}{\left| S_{11} \right|^2 - \left| \Delta \right|^2}$$

And again, $\Delta = S_{11}S_{22} - S_{12}\, S_{21}$

Unconditionally stability is achieved if the reflection coefficients for $r_{OUT}$and n_{IN} for all passive loads ($|r_L| < 1$) and all passive sources ($|r_s| < 1$) lie within the stable region, i.e. on the smith chart. This is achieved if the following conditions are met:

A. $|S_{11}| < 1$ and $|S_{22}| < 1$,
B. $|C_s| - R_s > 1$ and,
C. $|C_L| - R_L > 1$

4.1.4 Linearity

Many phenomena contribute to the distortion of a signal as it goes through an amplifier. Even the simplest case of an RF signal with constant envelope, some distortion is still caused by the variation of the group delay within the band. The problem becomes much more complex if the envelope is not constant, either because it consists of multiple RF carriers, or because it is, in fact, amplitude modulated. This is inevitably the case in modern communication systems: as the channel information efficiency is increased, the modulation becomes progressively more sophisticated [5, 6]. In fact, an efficient coding generally includes both amplitude and phase modulation, and the most efficient coding result in signals that closely resemble band-limited white noise. Such signals typically exhibit high peak-to-average power ratios. The problem is further aggravated when multiple signals are amplified within a single RF channel, because the beat between carriers generates amplitude modulation. This is, in fact, the mode of operation that is typical of base stations. In order to maintain signal integrity, even at the high peaks, the amplifier is operated at reduced output power, in what is called a back off mode. This inevitably reduces the operating efficiency, which becomes the most critical parameter. Thus optimizing the efficiency at a specified value of linearity is typically the main objective in the design of a linear power amplifier [6].

The amplifier must reproduce with low distortion both the amplitude and the phase of the signal. Yet, for the sake of simplicity, phase linearity is often neglected, and the entire industry of microwave solid-state amplifiers has been built around the concept of P1dB, which is only a measure of amplitude distortion, at best [3, 4].

For an amplifier or mixer the degree of non-linearity is measured by performing two tone tests or by determining the third order intercept (TOI) point. Input, Output impedances, frequency and input power levels affects the characteristic of inter-modulation distortion (IM).

In the measuring setup some errors in the input signals may increase error and it is difficult then to understand if the error is due to device or test setup. Impedance mismatching and proper isolation is required between input test signals. Error in setup is reflected at spectrum analyzer and accuracy of device under test (DUT) is compromised. For the third harmonics of DUT it is necessary to test the equipment first without DUT and ensure that the level of third harmonic is at desired level than the fundamental harmonic [16].

Detailed linearity analysis is described in following paragraphs, which was achieved by Two Tone Inter Modulation test.

4.1.5 Two-Tone Inter-modulation

Two tone excitation is a typical test to see the nonlinear distortion introduced by thePA. The PA is fed by the two tones separated by frequency (A/) and expressed mathematically as follows.

$$\boldsymbol{v_{in}(t) = v_1 \cos(\omega_1 t) + v_2 \cos(\omega_2 t)} \qquad \textbf{2-5}$$

$$\boldsymbol{\omega_1 = 2\pi(fc - \frac{\Delta f}{2}),\ \omega 2 = 2\pi(fc + \frac{\Delta f}{2})} \qquad \textbf{2-6}$$

where$\Delta f = f2 - f2;\ \omega = 2\pi f$

Consider a simple third-order approximation of the PA transfer characteristics given in

$$\boldsymbol{v_o(t) = k_1 \cdot v_{in}(t) + k_2 \cdot v_{in}^2(t) + k_3 \cdot v_{in}^3(t)} \qquad \textbf{2-7}$$

Where:

$v_{in}(t)$ and $v_o(t)$ are the input and output signals to the amplifier respectively$k_1$is the small-signal gain.

$k_2$and $k_3$are the first two coefficients of McLauren series expansion of the PA transfer characteristics, truncated to third order [22].

Inserting the input signal from (2-1) in the PA truncated expansion in (2-3), the output signal becomes:

$$v_{in}(\boldsymbol{t}) = v_1 \boldsymbol{cos}(\omega_1 \boldsymbol{t}) + v_2 \boldsymbol{\cos}(\omega_2 \boldsymbol{t})$$

$$\begin{aligned}
\boldsymbol{v_o(t)} = {} & \frac{k_2 \boldsymbol{v_{in1}^2}}{\boldsymbol{2}} + \frac{k_2 \boldsymbol{v_{in1}^2}}{\boldsymbol{2}} + \boldsymbol{v_{in1}}\left[k_1 + \frac{\boldsymbol{3} k_3 \boldsymbol{v_{in1}^2}}{\boldsymbol{4}} + \frac{\boldsymbol{3} k_3 \boldsymbol{v_{in2}^2}}{\boldsymbol{2}}\right] \boldsymbol{\cos}(\boldsymbol{\omega_1 t}) \\
& + \boldsymbol{v_{in}}\left[k_1 + \frac{\boldsymbol{3} k_3 \boldsymbol{v_{in2}^2}}{\boldsymbol{4}} + \frac{\boldsymbol{3} k_3 \boldsymbol{v_{in1}^2}}{\boldsymbol{2}}\right] \boldsymbol{\cos}(\omega_2 \boldsymbol{t}) + \frac{k_2 \boldsymbol{v_{in1}^2}}{\boldsymbol{2}} \boldsymbol{cos}(\boldsymbol{2\omega_1 t}) \\
& + \frac{k_2 \boldsymbol{v_{in2}^2}}{\boldsymbol{2}} \boldsymbol{cos}(\boldsymbol{2}\omega_2 \boldsymbol{t}) + k_2 \boldsymbol{v_{in1} v_{in2}}[\boldsymbol{\cos}((\omega_2 - \boldsymbol{\omega_1})\, \boldsymbol{t}) + \boldsymbol{\cos}((\omega_2 + \boldsymbol{\omega_1}) \boldsymbol{t})] \\
& + \frac{k_3 \boldsymbol{v_{in1}^3}}{\boldsymbol{4}} \boldsymbol{cos}(\boldsymbol{3\omega_1 t}) + \frac{k_3 \boldsymbol{v_{in2}^3}}{\boldsymbol{4}} \boldsymbol{cos}(\boldsymbol{3}\omega_2 \boldsymbol{t}) + \frac{\boldsymbol{3} k_3 \boldsymbol{v_{in1}^2 v_{in2}}}{\boldsymbol{4}} [\boldsymbol{\cos}((\boldsymbol{2\omega_1} + \omega_2)\, \boldsymbol{t}) \\
& + \boldsymbol{\cos}((\boldsymbol{2\omega_2} - \boldsymbol{\omega_1}) \boldsymbol{t})] + \frac{\boldsymbol{3} k_3 \boldsymbol{v_{in2}^2 v_{in1}}}{\boldsymbol{4}} [\boldsymbol{\cos}((\boldsymbol{2}\omega_2 + \boldsymbol{\omega_1})\, \boldsymbol{t}) + \boldsymbol{\cos}((\boldsymbol{2}\omega_2 \\
& - \boldsymbol{\omega_1}) \boldsymbol{t})]
\end{aligned}$$

Equation 2.8 is used to calculate the harmonics of power spectrum. The interested harmonic in our system is of 3rd order because second order inter-modulation distortion (IMD) is typically outside the desired bandwidth but the third order is inside the signal bandwidth.

2nd order inter-modulation distortion is$\omega_1 + \omega_2$ and $\omega_1 - \omega_2$

3rd order inter-modulation distortion is$+ \omega_2$, $\mathbf{2}\omega_1 - \omega_2$and $2\omega_2 + \omega_1$,$\mathbf{2}\omega_2 - \omega_1$

The output signal spectrum of the PA with two-tone signal is shown in figure 2.3.

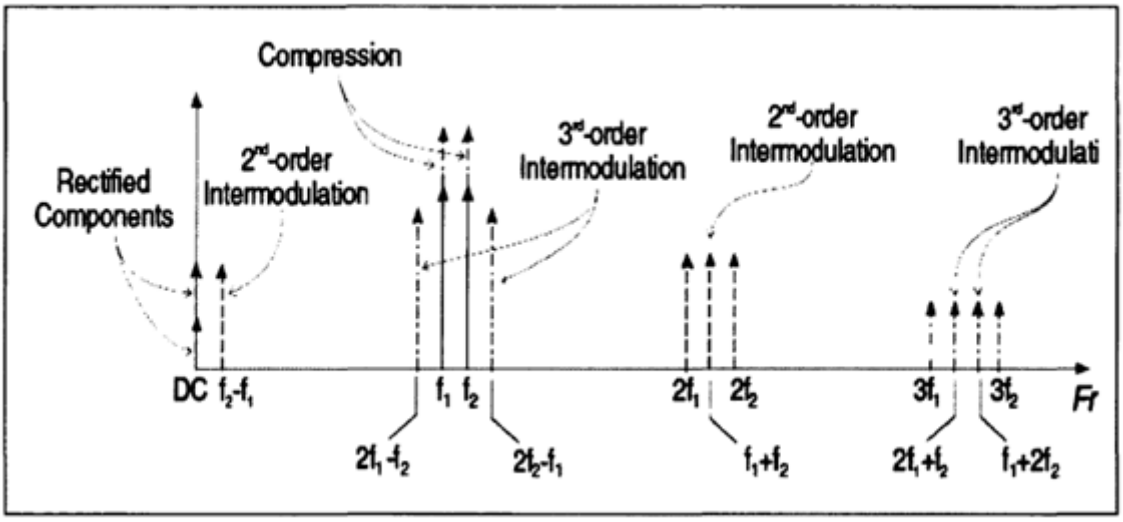

Figure 4-1 Frequency Spectrum on Non-linear PA with two-tone Signal [22]

Although gain compression is obviously a problem for amplifier caused by the third-order nonlinearity, it is the greater concern of inter-modulation products appearing at $2\boldsymbol{\omega}_2 - \boldsymbol{\omega}_1$ and $2\boldsymbol{\omega}_1 - \boldsymbol{\omega}_2$ [22]. These kinds of distortions appear in in-band will distort the desired shape of the original input signal. Because it is in-band distortion, it is impossible to filter out using conventional output filters. Therefore, in order to minimize the effect of signal distortion, the use of linear amplifier is necessary. With different linearization techniques that are available nowadays, the implementation of either any one of the ways is a must to apply in either system level or circuit level. The pay-off is an additional cost in the communication transceiver.

In addition to minimizing noise contribution, the LNA must provide high linearity, the ability to handle large signals. The input inception point (*IIP3*) or the 1-dB compress point (*P1-dB*) are used to characterize the linearity [3, 4].

Definition 4: *IIP*3 = input power when the third-order inter-modulation distortion (IMD3) matches the signal power.

Definition 5: *P*1-dB = input power when power gain decreases by 1 dB.

Third order intercept point is illustrated in figure 2.2.

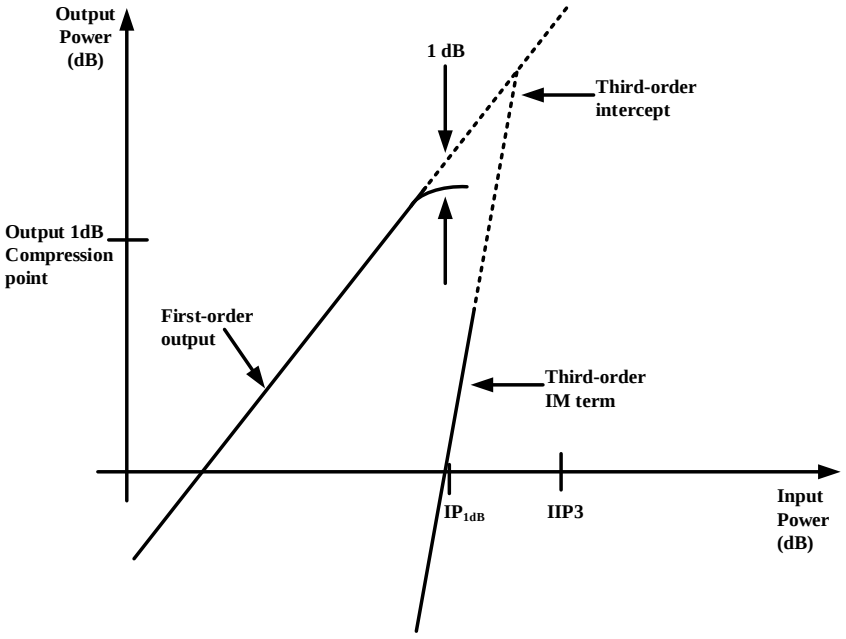

Figure 4-2 Third orders intercept point found by extrapolating

4.2 WILKINSON POWER DIVIDER

Power dividers and directional couplers are passive schemeof microwave theory used for power partition or power combine. In power partition incoming signal being divided in to two or more output signals of less power, whereas a power combiner scheme combines input signals (two or more). At one output portcoupler or dividerassumes to be lossless ideally available in two to four ports depending on their configuration for example; Three-port networks (T-junctions) and four-

port networks (directional couplers and hybrids). Power dividers provides in-phase output signals byequal power division ratio of 3 dB.

The Wilkinson powerdivider is passive microwave network which possess to be lossless when the outputports are matched i.e. only reflected power from the output ports is dissipated at the resistor which has been incorporated in the network.The Wilkinson power divider gives arbitrary power division which is equal-split (3 dB) case. This divider is often made in microstrip line. Summarize power reflection parameters are shown below:

S11 = 0	Zin =1 at port 1
S22 = S33 = 0	Ports 2 and Port 3 matched for even and odd modes
S12 = S21 = $\frac{V_1^e + V_1^o}{V_2^e + V_2^e} = -j/\sqrt{2}$	Symmetry due to reciprocity
S13 = S31 = $-j/\sqrt{2}$	Symmetery of Ports 2 and 3
S23 = S32 = 0	Due to short or open at bisection

4.3 RF Isolator

RF isolators are also passive microwave devices usually of 2 port that helps to prevent RF components from the extra current or signal which undergoes reflection due to mismatch for Example normal Co-axial cable act as RF isolators which is one directional way passage for the RF signals i.e. isolating a source from the load in such a way that any reflected back energy due to mismatch port(load) is trapped or dissipated. Isolators are actually made up of ferrite materials or magnets which will cater the direction of entering signal flow. These RF ferrite isolators have minimum isolation ratings between 16 dB and 20 dB. The greater the isolation the less interference for a signal on one port is present at the other. The amount of isolation is directly affected by the VSWR available at port 3 of the isolator. Another important factor for the isolators is insertion loss which is the parameter normally more important at higher frequency because power loss increases with frequency and higher frequency power sources are considerably more expensive. Thus low insertion loss will save precious power to be wasted.

4.4 Attenuator

Attenuators are also passive microwave circuits that will reduce the input signal fed at its input. Attenuators are designed in two configurations pie and T configuration. Important characteristics of the attenuator is to be accurate in its attenuation value expressed in dB, having low SNR with flat frequency response and its ability to repeat itself likely to be as previous. Power dissipation of the attenuator will determine the size and shape of it. Normally attenuators are used to have a safer power measurement during testing etc.

4.5 Device Selection

Important part in designing a power amplifier is to select a transistor that provides the required output power at a particular frequency and matches the linearity requirements of the system. Cost, availability and non-linear model are also to be seen when selecting a particular device. For high value of P1db transistor a driver stage should also be made either from transistor or MMIC which provides the required level for amplification. In our case we have selected FLL-120MK EUDYNA FET which can perform upto 5GHz from 0.5 GHz, has a P1db of 40dBm and 10db gain and has biasing values of 10V and 1.7A. For driver stage we have chosen an MMIC of BOWEI H162E which is an average efficiency IC requiring 28V and 2A. Other transistors were keenly investigated that can provide the desired response, the output of this through search resulted in trade off among the parameters mentioned above and FLL-120MK and BOWEI 162E were selected as an ideal choice. A comparative table of transistor technology for PA design is shown below

Table 4.5-1Recent Reports on PA design

Ref.	Tech.	Freq.	PAE	Pout	Class
Xie'03[17]	GaN, HEMT	3 G	34%	36dBm	B
Sowlati'03[18]	CMOS	2.4G	45%	23.5	-
Yen'03[19]	CMOS	2.45 G	28%	20dBm	AB

Shirvani'02[20]	CMOS	1.4G	49%	22.6dBm	F
Our work	GaAs FET	2.25GHz	52%	40dBm	AB

Power transistor devices were selected according to the requirement of frequency, gain and P1dB. Comparison of some selected devices is shown below:

Table 4.5-2 Device comparison of critical parameters

Device	Technology	Gain (dB)	P1dB (dBm)	PAE
FLL120MK(Fujitsu/Eudyna)	GaAs FET	10.0	40	64%
MAAP-011022 / MA (MA-COM)	GaAs FET	23	37.5	28%
NPA1003(Nitronix)	GaN	18	30	42%
CGH40006P(Cree)	GaN HEMT	10	32	62%
TGA2237-SM(Toshiba)	GAN HEMT	8	38	50%

As clearly seen from the comparison, FLL120MK is the most optimum device with respect to tradeoff analysis of Gain and power added efficiency.

CHAPTER 3

HIGH POWER AMPLIFIER DESIGNING WITH SIMULATION RESULTS

5 HPA Model development and simulations in ADS

5.1 Measuring the Stability Factor (k) and Measure (b)

The first and foremost in design of power amplifier is to check whether the amplifier is stable at our desired frequency or not. To assess the broadband stability of a transistor, the Rollett Stability Factor (k) and Stability Measure (b) are used [4, 5]. The conditions for unconditional stability are that the stability factor is greater than unity and stability measure is positive. i.e., k>1 and b>0.ADS has the pallets stability measure (StabMeas) and stability factor (StabFact) as shown in figure 4.1.

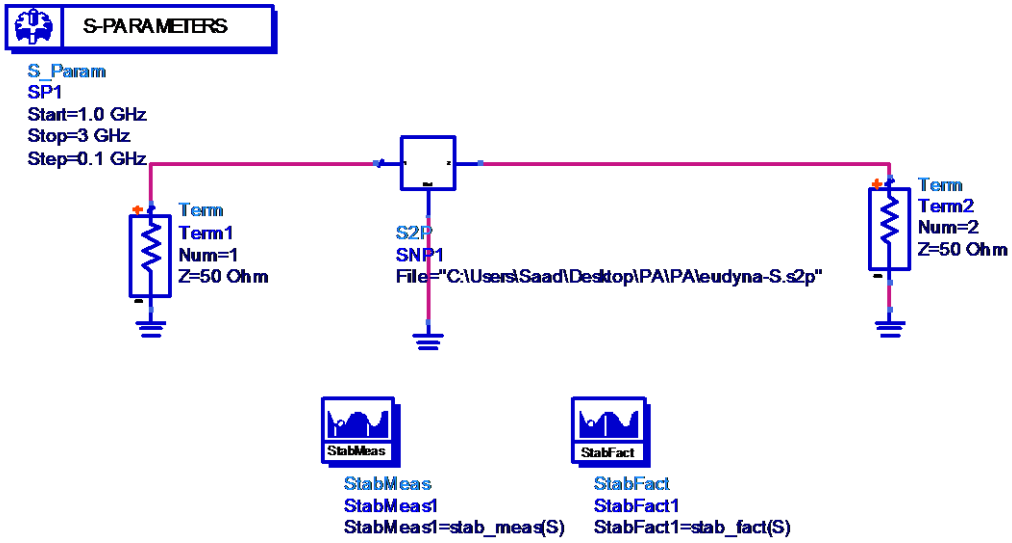

Figure 5-1 Stability measurement of GaAs MESFET

By analyzing figure 4.2 we can see that the stability factor is greater than 1 and stability measure is greater than zero at our desired frequency of 2.25GHz hence fulfilling the Rollet stability criteria.

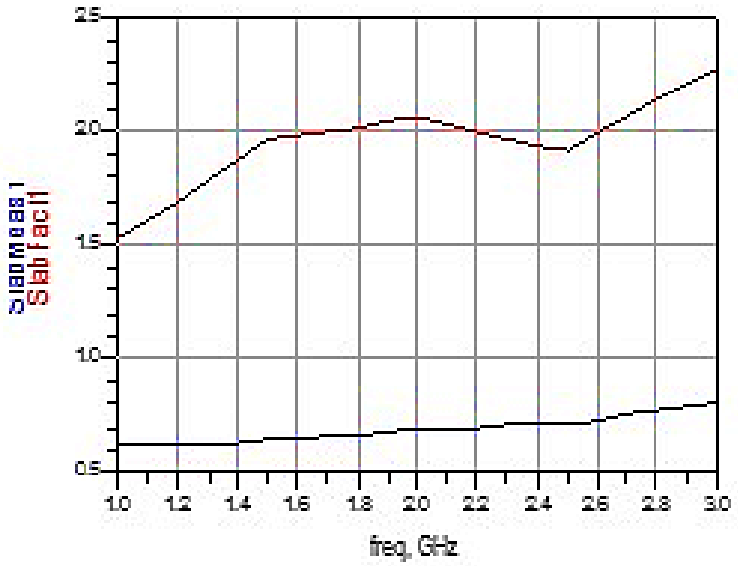

Figure 5-2Stability measure of power amplifier

The S – parameters details were obtained from the datasheet of FLL-120MK FET (Annex A). Further, the simulation tools like *StabFct* and *StabMeas*ure added into the schematic as shown below.

It can be observed that the subject amplifier has stability factor (k) > 1 and stability measure (b) > 0 for the desired frequency. It is therefore, quite stable between 1.0 and 5.0 GHz. The ideal 2 – ports MESFET amplifier is terminated into 50 Ω terminations as shown below. Different analysis tools like *S_StabCircle*, *L_StabCircle*,S_mGamma_1 and $S_mGamma_2$were also added to the schematic. For a 2 – port network, SmGamma1 returns the simultaneous-match input-reflection coefficient; SmGamma2 returns the simultaneous-match output-reflection coefficient, and *S_StabCircle* and *L_StabCircle*describe the regions of stability for the device [4, 5].

The reflection coefficients are needed for simultaneous conjugate matching for the designed circuit. For finding S_mZ_1 and S_mZ_2 values at different frequencies S-parameter is applied as shown in figure 4.3

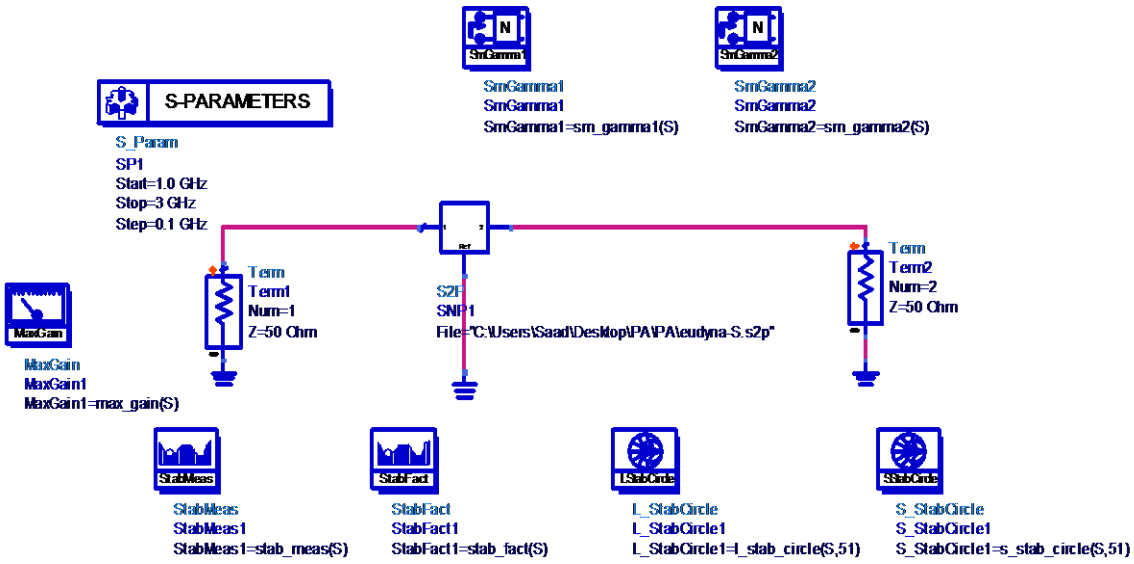

Figure 5-3 Conjugate matching of power amplifier

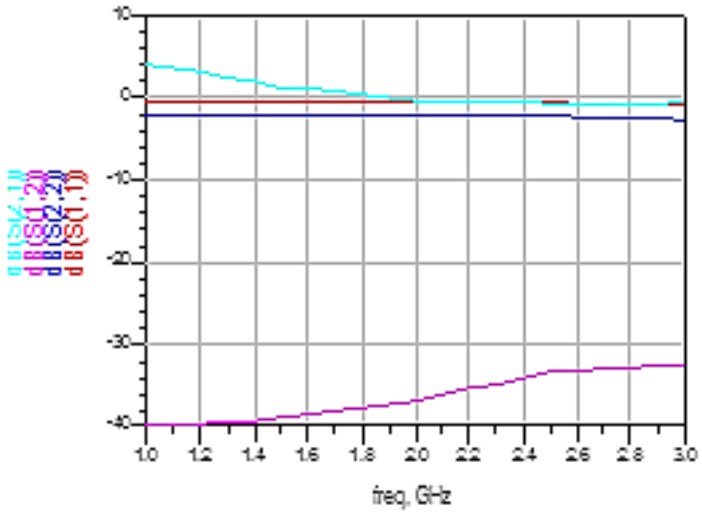

Figure 5-4S-parameters graph before matching

From the S-parameter plots in figure 4.3 it was observed that around 2 GHz, the magnitude of S11 and S22 are less than one and S21 is much larger than S12. It was also observed that S11 is fairly good around 2.25 GHz – this is because there is some internal matching on the input to the device.

Table 5.1-1Input output impedance measurement at different frequencies

freq	SmZ1	SmZ2
1.000 GHz	2.885 / 58.510	8.041 / 25.939
1.050 GHz	2.735 / 55.655	8.112 / 23.522
1.100 GHz	2.590 / 52.547	8.174 / 21.172
1.150 GHz	2.451 / 49.151	8.229 / 18.884
1.200 GHz	2.319 / 45.431	8.276 / 16.654
1.250 GHz	2.196 / 41.352	8.315 / 14.481
1.300 GHz	2.082 / 36.883	8.346 / 12.362
1.350 GHz	1.980 / 32.002	8.368 / 10.295
1.400 GHz	1.892 / 26.702	8.383 / 8.281
1.450 GHz	1.818 / 21.001	8.390 / 6.319
1.500 GHz	1.761 / 14.948	8.389 / 4.408
1.550 GHz	1.740 / 9.178	8.533 / 2.994
1.600 GHz	1.736 / 3.311	8.673 / 1.581
1.650 GHz	1.748 / -2.542	8.809 / 0.172
1.700 GHz	1.776 / -8.274	8.940 / -1.232
1.750 GHz	1.820 / -13.791	9.068 / -2.628
1.800 GHz	1.879 / -19.019	9.190 / -4.015
1.850 GHz	1.950 / -23.912	9.307 / -5.391
1.900 GHz	2.034 / -28.445	9.419 / -6.754
1.950 GHz	2.127 / -32.613	9.525 / -8.102
2.000 GHz	2.230 / -36.427	9.626 / -9.433
2.050 GHz	2.399 / -39.779	9.777 / -10.594
2.100 GHz	2.575 / -42.717	9.927 / -11.755
2.150 GHz	2.757 / -45.305	10.073 / -12.9...
2.200 GHz	2.944 / -47.596	10.218 / -14.0...
2.250 GHz	3.136 / -49.638	10.360 / -15.2...
2.300 GHz	3.332 / -51.466	10.501 / -16.3...
2.350 GHz	3.531 / -53.114	10.639 / -17.4...
2.400 GHz	3.733 / -54.606	10.776 / -18.6...
2.450 GHz	3.937 / -55.964	10.911 / -19.7...

Hence, the simultaneous Match – Input Impedance **SmZ1**and Simultaneous Match – Output Impedance **SmZ2** at 2.25 GHz for **FLL120MK**at V_{ds}= 10Vand I_d = 1.7A are referred from the results table as:

Simultaneous mismatch-Input Impedance **SmZ1**	**Simultaneous mismatch-Output Impedance** **SmZ2**
2.03-j2.39	**9.99-j2.72**

To answer the question, at what frequency this device is potentially unstable, the stability regions of the amplifier were analyzed by studying the stability circles S_StabCircle and L_StabCircle. From these stability circle plots of figure 4.4 and figure 4.5, it was found that below 500 MHz, the design is potentially unstable [4, 5].

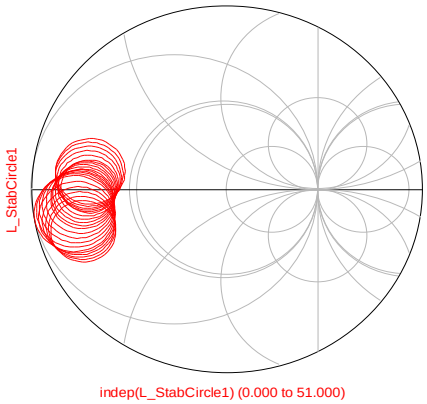

Figure 5-5 L stability circle

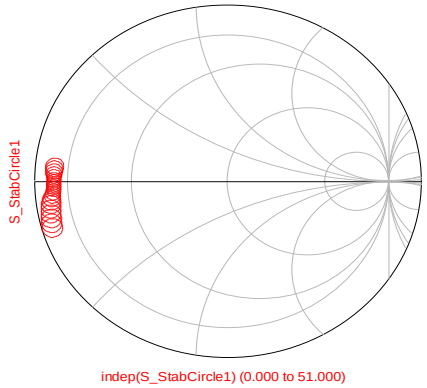

Figure 5-6 S stability circle

It should be noted that the amplifier should be stable across all frequency ranges and steps would have to be taken to ensure unstable regions are avoided. Stability can be improved through resistive loading but this can have a negative effect on achievable gain [4, 5].

5.2 Broad band microwave choke for DC blocking

Microwave devices which use Direct Current source power should also have preventive measure so that the microwave energy may not enter the power supply. Microwave choke used to prevent microwave power from shorting out through the power supply. Thus power supply is microwave isolated from the active micro strip circuit devices, and the DC power is typically blocked using a capacitor. This practice is called bias tree and widely used in almost all microwave designs [26, 27].

CHAPTER 4

HPA MATCHING CIRCUIT DESIGN

6 HPA Matching Circuit design

6.1 ADS simulation Pre-tuning

An initial circuit is designed using input and output power impedances as seen table 4.2. Using smith chart utility and S-parameter pallet from ADS design guide. The initial impedance matching circuit forms the basis of our design, this design is tuned by changing parameters of Width and length of micro strip line which in turn makes results better.

6.2 Input Matching Circuit

Using the power impedances of input side input matching network is made. Substrate pallet is used by from ADS design guide. Parameters of dielectric constant, width of substrate are entered in this pallet, related parameters are also entered which are mentioned in FR4 substrate properties. The designed input matching circuit is shown in figure 5.1

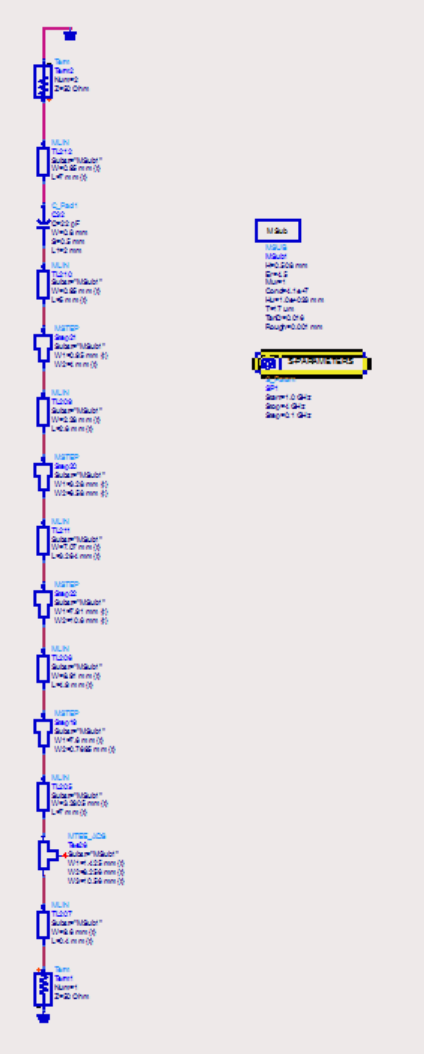

Figure 6-1 Input Matching Circuit

6.2.1 Output Matching Circuit

Using the power impedances of output side input matching network is made. Substrate pallet is used by from ADS design guide. Terminations of 50 ohm is connected on one side and power impedance of load side is connected of other side, Frequency start and stop are added in the S-parameter pallet which defines the simulator at which frequency and at what step size it has to simulate Parameters of dielectric constant, width of substrate are entered in this pallet, related parameters are also entered which are mentioned in FR4 substrate properties. The designed input matching circuit is shown in figure 5.2.

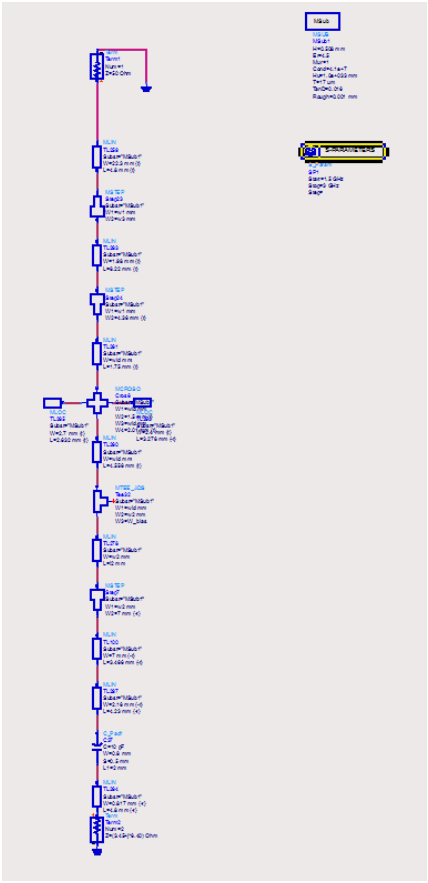

Figure 6-2 Output Matching Circuit

6.2.2 Results

The results in figure 5.3 and 5.4 shows that the matching is poor as both the markers in figure 5.3 are not at 50. Similarly S11 and S22 at 2.25GHz are not at null point in figure 5.4

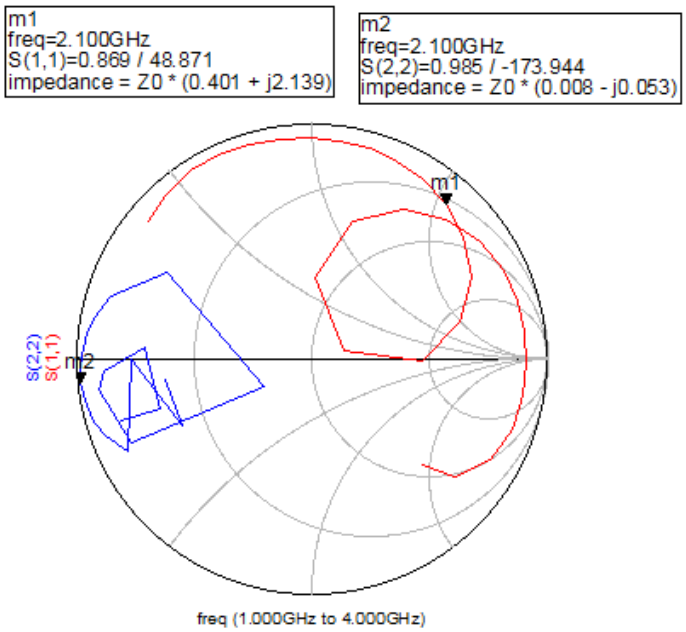

Figure 6-3 Impedance mismatch shown on Smith Chart

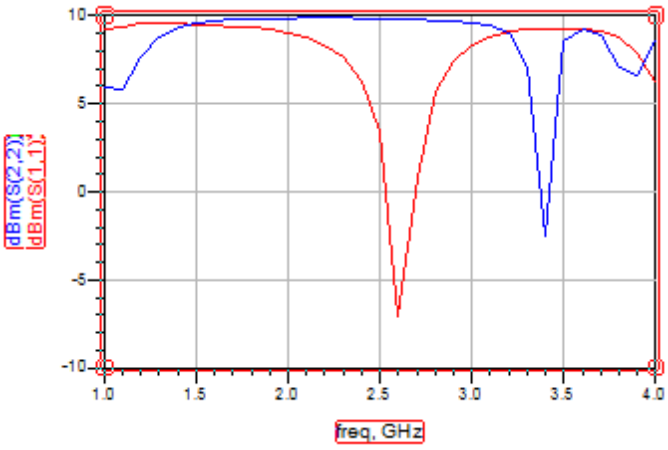

Figure 6-4 Input and Output return loss

Also, S21 which is the gain of amplifier at 2.25GHz is at 4dB. The impedance matching network designed caters only the S-parameters and doesn't include the effects caused by large signal. Hence tuning at this stage in the simulation is a must requirement to achieve required results of S11, S21, S12 and S22

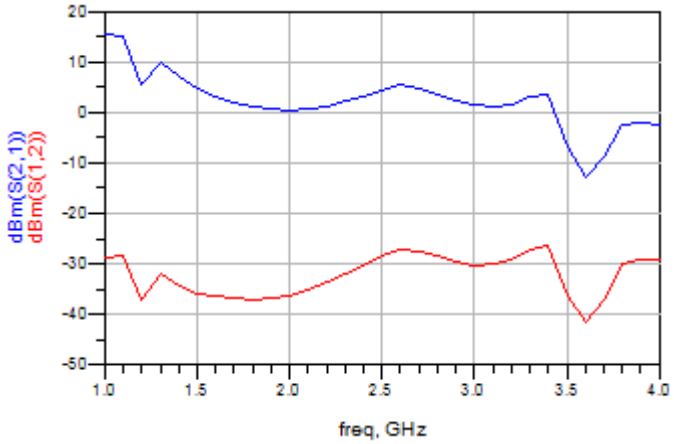

Figure 6-5 Forward and Reverse transmission coefficient

6.3 HPA MATCHING USING LOAD PULL SETUP

6.3.1 Input Matching Circuit

Using the power impedances of input side input matching network is made. Substrate pallet is used by from ADS design guide. Parameters of dielectric constant, width of substrate is entered in this pallet, related parameters are also entered which are mentioned in FR4 substrate properties. The designed input matching circuit is shown in figure 6.1

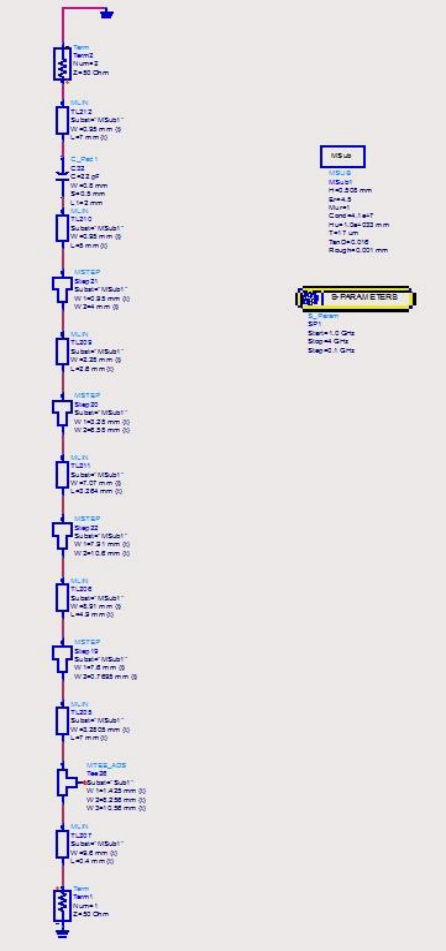

Figure 6-6 Input Matching circuit

Layout is generated using the layout generation utility of ADS. The substrate properties are taken input from the schematic where it is defined using ADS substrate utility.Layout design of output tuned matching circuit shown in figure 6.2.

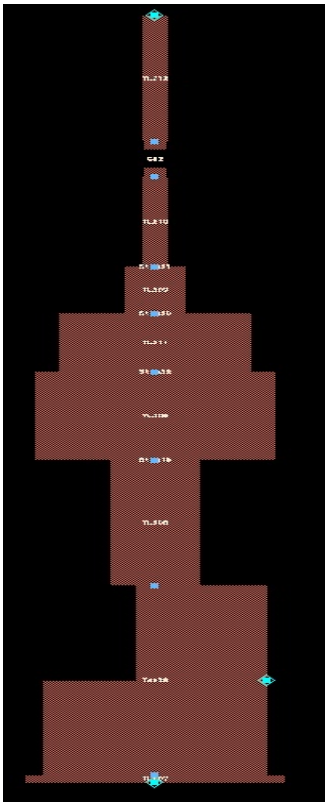

Figure 6-7 layout of input matching circuit

6.3.2 Output Matching Circuit

Using the power impedances of output side input matching network is made. Substrate pallet is used by from ADS design guide. Terminations of 50 ohm is connected on one side and power impedance of load side is connected of other side, Frequency start and stop are added in the S-parameter pallet which defines the simulator at which frequency and at what step size it has to simulate Parameters of dielectric constant, width of substrate are entered in this pallet, related parameters are also entered which are mentioned in FR4 substrate properties. The designed input matching circuit is shown in figure 6.3.

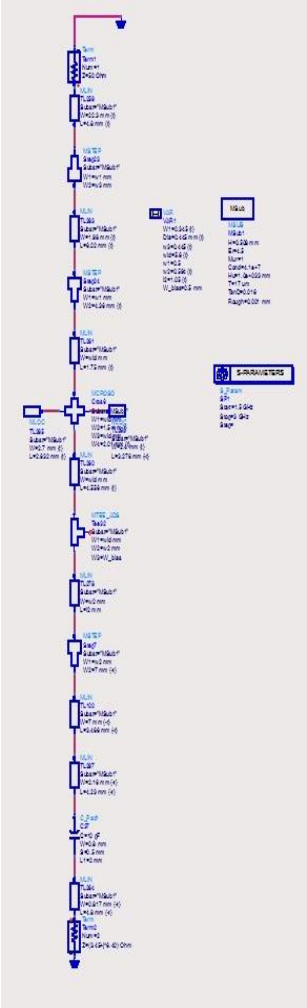

Figure 6-8 Output matching circuit

Layout is generated using the layout generation utility of ADS. The substrate properties are taken input from the schematic where it is defined using ADS substrate utility.Layout design of output tuned matching circuit shown in figure 6.4

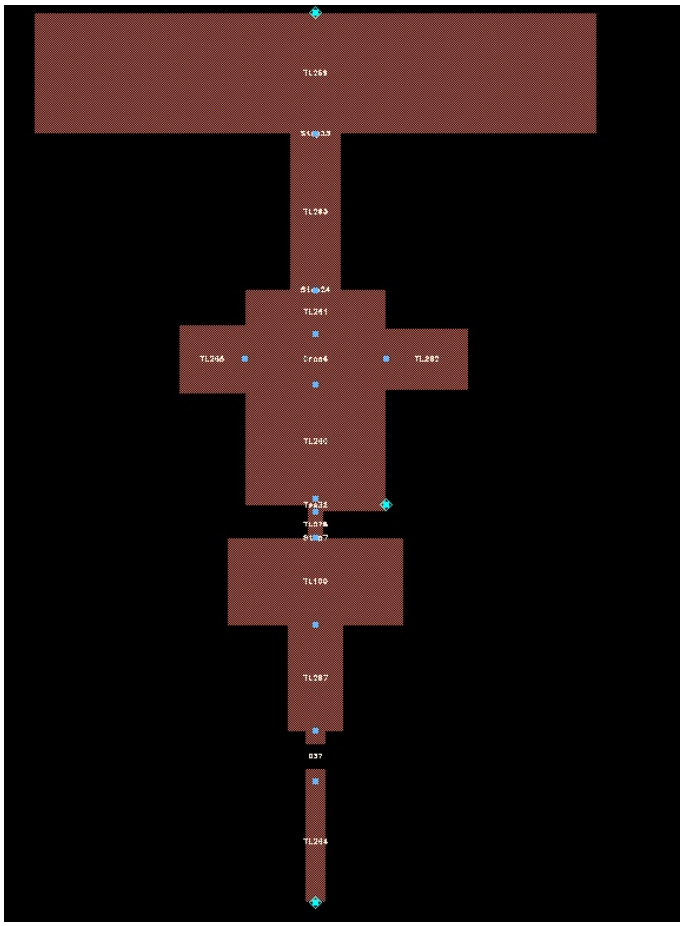

Figure 6-9 Layout Design

Load Termination Impedance: 3.43–j6.85 Ohm
Source Termination Impedance:1.89-j1.74 Ohm

6.3.3 Results

Final results showing null points are 2.25 GHz after tuning from passive load pull and ADS simulations in figure 6.5

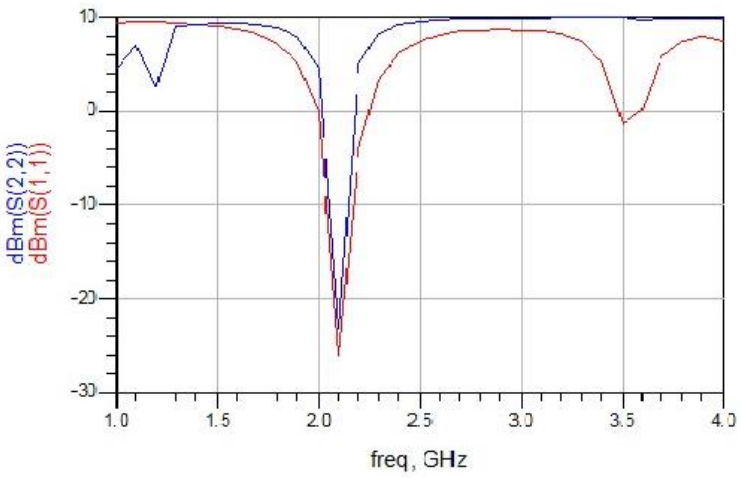

Figure 6-10 Input and Output Return loss

Smith chart showing S11 and S22 matched at 50 ohm in figure 6.6

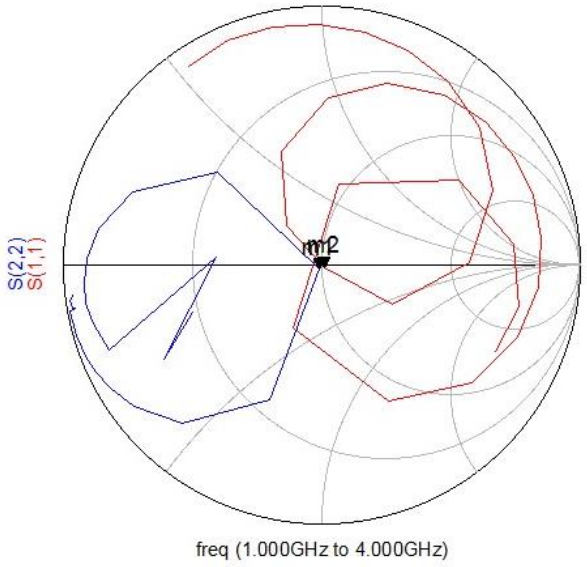

Figure 6-11 Design matched using tuning parameters on Smith Chart

The layout for final Power amplifier stage design withoutbiasingnetwork, the layout is then exported to Gerber file which is sent for PCB designing on desired substrate. Transistorspacing is not calculated at this stage. Complete layout of power amplifier stage is shown in figure 6.7

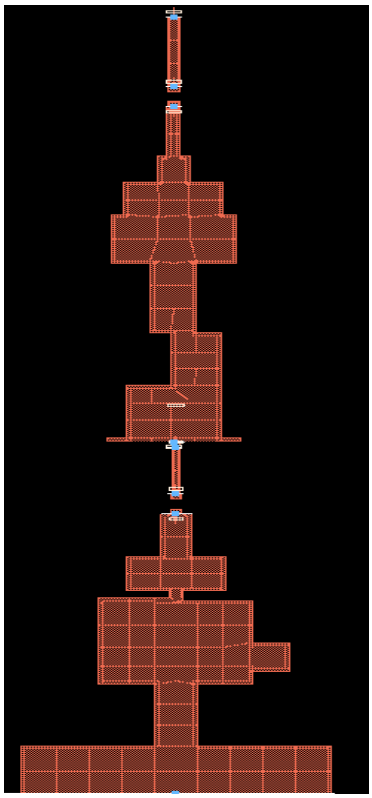

Figure 6-12 Layout design layout design of power amplifier stage without DC biasing

Using the power impedances of input side input matching network is designed. Substrate pallet is used by from ADS design guide. Parameters of dielectric constant, width of substrate is entered in this pallet, related parameters are also entered which are mentioned in FR4 substrate properties. Substrate pallet is used by from ADS design guide. Terminations of 50 ohm is connected on one side and power impedance of load side is connected of other side, Frequency start and stop are added in the S-parameter pallet which defines the simulator at which frequency and at what step size it has to simulate Parameters of dielectric constant, width of substrate are entered in this pallet, related parameters are also entered which are mentioned in FR4 substrate properties. Complete schematic design of power amplifier stage with biasing network this shows the final schematic design which is tunes according to our requirements as shown in figure 6.8.

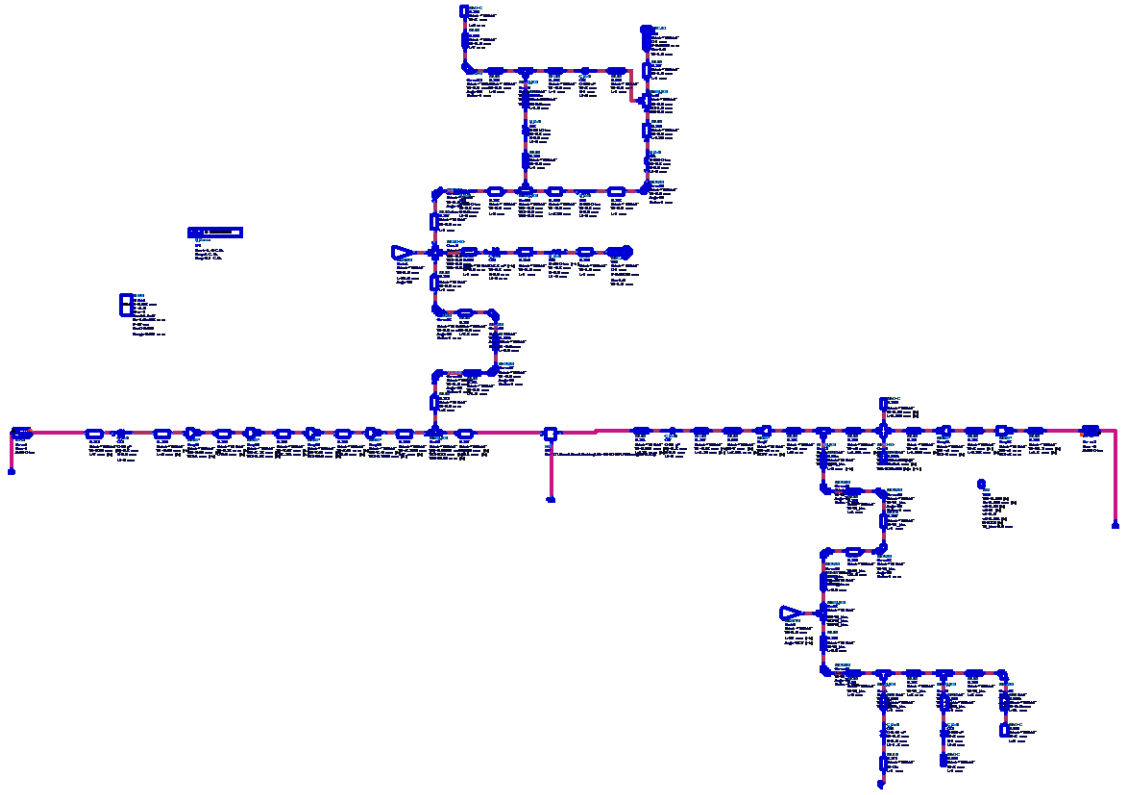

Figure 6-13 Input and output matched impedance circuits with biasing network

Layout generated with biasing network and transistor IC placing is also calculated, the lambda by 4 biasing network is carefully designed as it acts as isolation between RF and DC. Device dimension parameters are also entered so that it can be solder accurately to the matching circuit without any mismatch. The complete layout design of power stage amplifier is shown in figure 6-9.

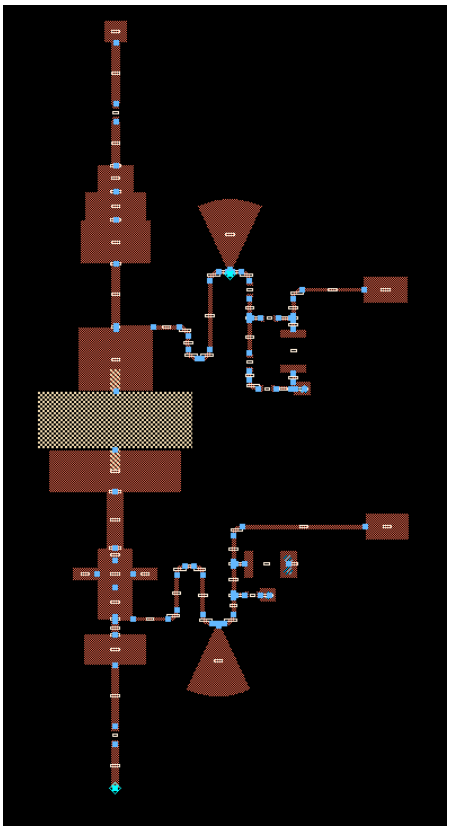

Figure 6-14 Layout design layout design of power amplifier stage without DC biasing

6.3.4 Driver Amplifier Design for P1dB requirement

The driver amplifier BOWEI H162C is used for achieving the P1dB requirement of 30dBmof Power amplifier transistor. The driver amplifier is an MMIC so its matching circuit is designed by manufacturer inside the IC using transistor wafer. The power input and output and biasing network is designed only in ADS. Layout is shown in figure 6.10

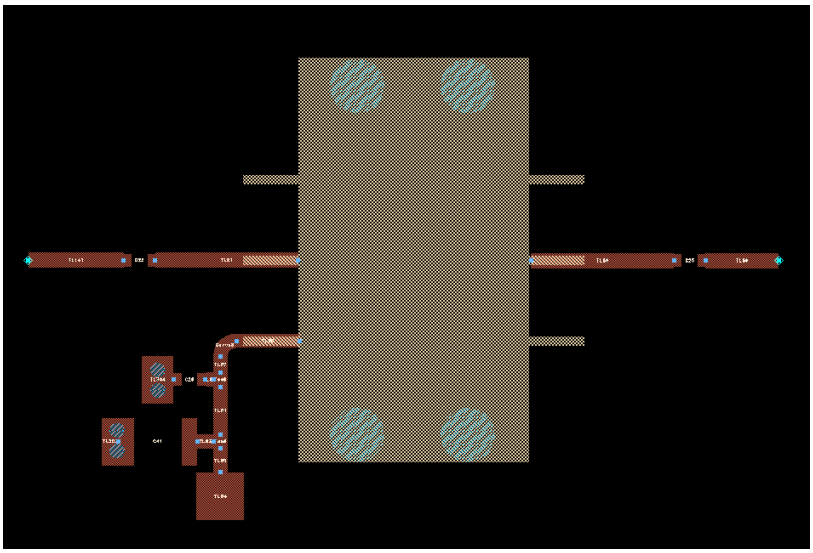

Figure 6-15 Design using Power Impedances

Layout is then merged and complete layout was generated, dimensions of ICs were also measured and incorporated in the layout. Device dimension parameters are also entered so that it can be solder accurately to the matching circuit without any mismatch. The complete layout design of driver stage and power amplifier stage is shown in figure 6-11.

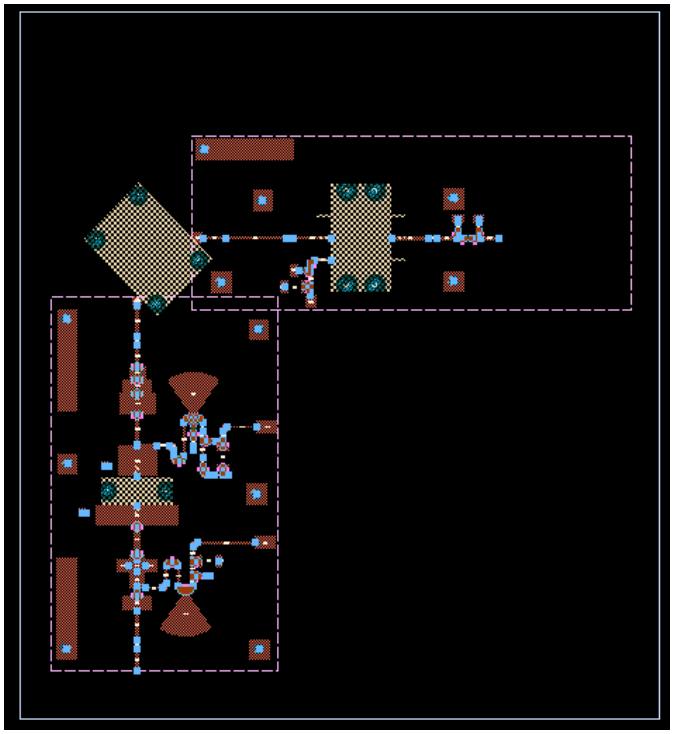

Figure 6-16 Complete layout design with driver amplifier

6.3.5 Wilkinson Combiner for Two-tone testing

The initial problem was to analyze a non-optimum Wilkinson Power Divider and then to optimize it using Agilent ADS and produce the usual values for line impedance (Z) and isolation resistance (R). For this task the single stage Wilkinson Power Divider was implemented as shown in the figure below using the ideal transmission line model as mentioned in CAD Lab – 1.

To determine the initial values of line impedance (Z) and isolation resistance (R), two variables were defined as directed in the CAD Lab – 1: r1 = 50 Ω opt {10 Ω to 500 Ω} z1 = 50 Ω opt {20 Ω to 150Ω} The nominal values of r1 and z1 were specified to be 50 Ω with r1 ranging between 10 Ω to 500 Ω and z1 ranging between 20 Ω to 150 Ω. The nominal value was defined to be taken as the seed value whereas the range was defined as an optimization window. The simulation settings as mentioned below were set to obtain S – parameters,

Start = 2.0 GHz; Step = 250 MHz; Stop = 4.0 GHz

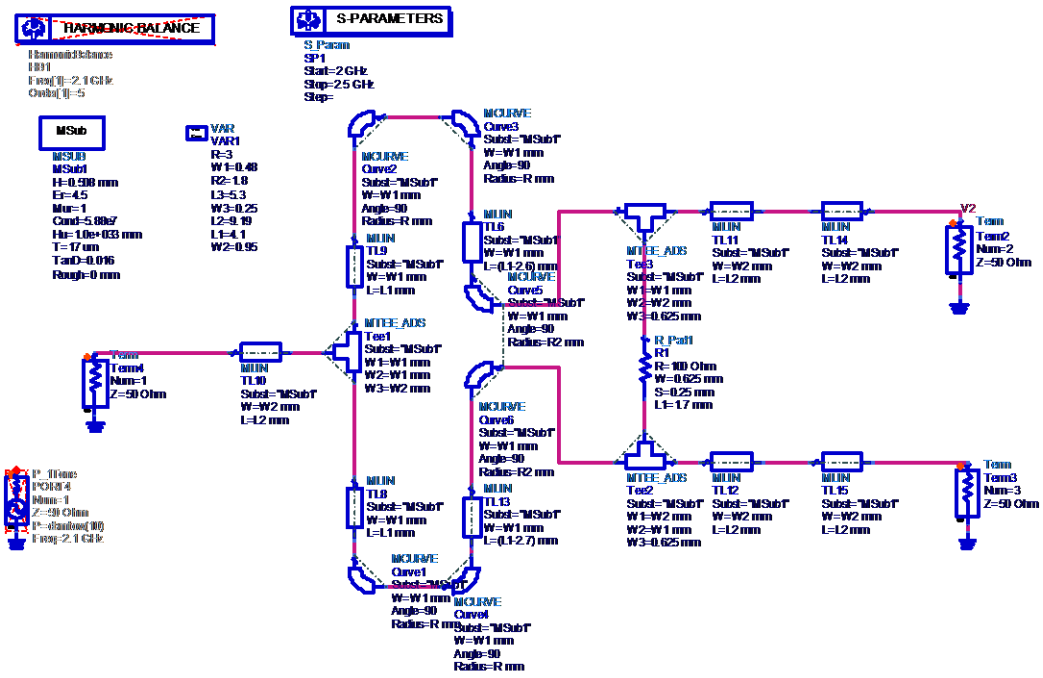

Figure 6-17 Design schematic of S-band Wilkinson power combiner

Designed results of Wilkinson showing S11 and S22 null points at our desired frequency range and maintaining 3 dB at S21 and S12.

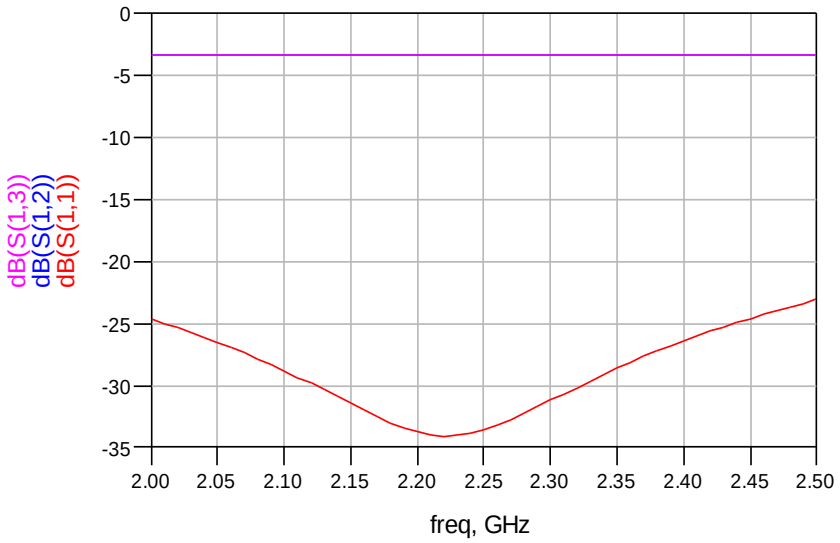

Figure 6-18 S-parameter measurement on ADS

Layout of the designed schematic

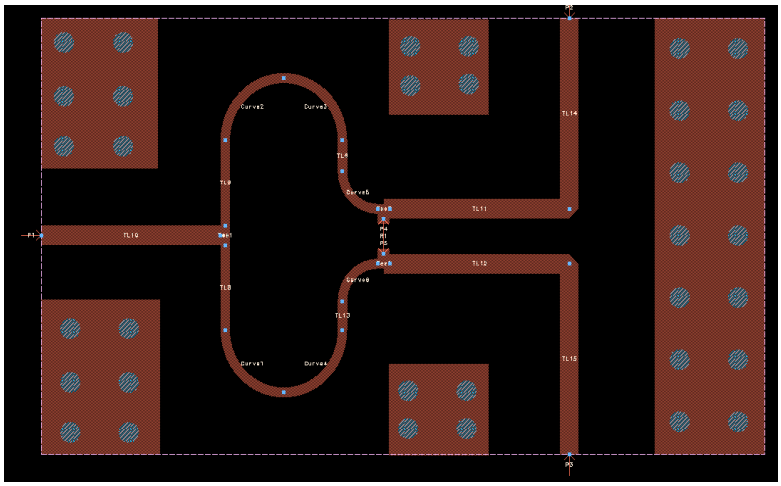

Figure 6-19 Final layout design of Wilkinson power combiner

EM simulations are performed using ADS which further validates our design and shows closer results of actual design,

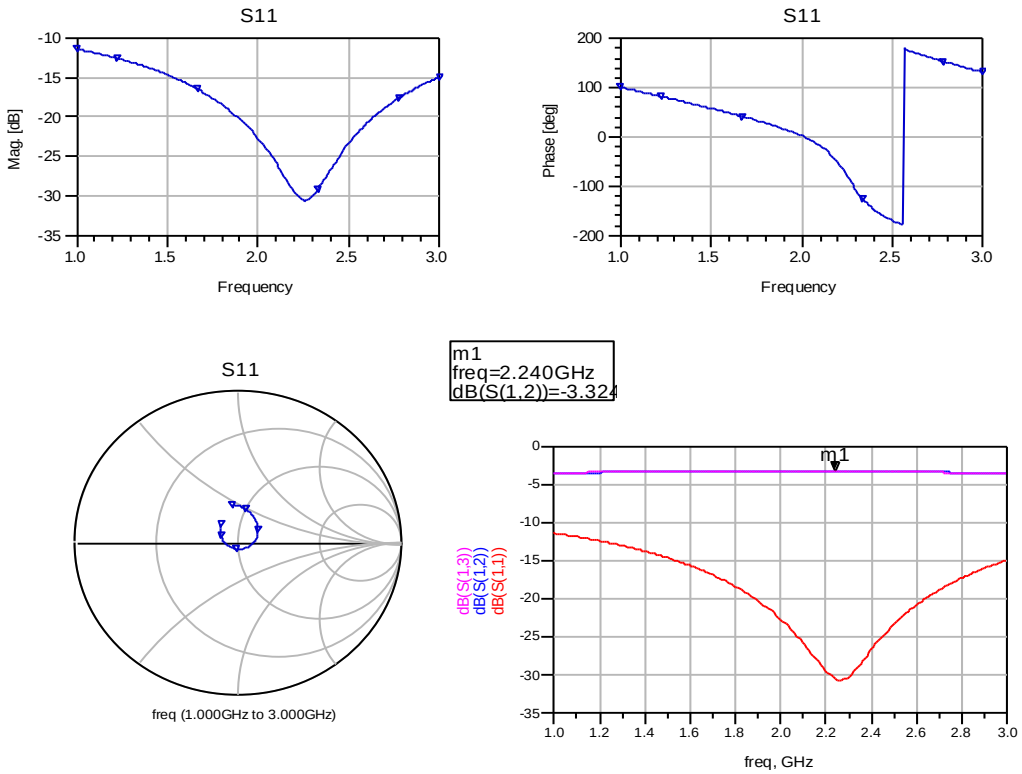

Figure 6-20 EM simulations of Wilkinson power combiner

CHAPTER 5

MODELING USING NON-LINEAR TRANSISTOR LIBRARY

7 MODELLING USING NLTL (Non-linear transistor library)

7.1 Introduction

The most accurate method to design a matching network for a power transistor is to use non-linear model of device. Since we used passive load pull approach in our thesis therefore in this section non-linear method is used to further prove the design scheme. A similar GaN device which has its NLT model available is used in the same frequency range

7.2 DC Analysis (Operating point)

Firstly we need to choose a bias point based on class of operation or vendor/foundry recommendation. Depicted simulation results shows the bias point calculated for a given maximum power. The device (CGH40006P) maximum power of safe operation was put onto it for the evaluation of a proper bias point. The procedure used in the section is described in detail in Annexure D.

Here we will be using the amplifier in class A operation so the bias point is chosen to be at the center of I-V curves. Given transistor is then biased at that point and a sub circuit of it was made for simplicity.

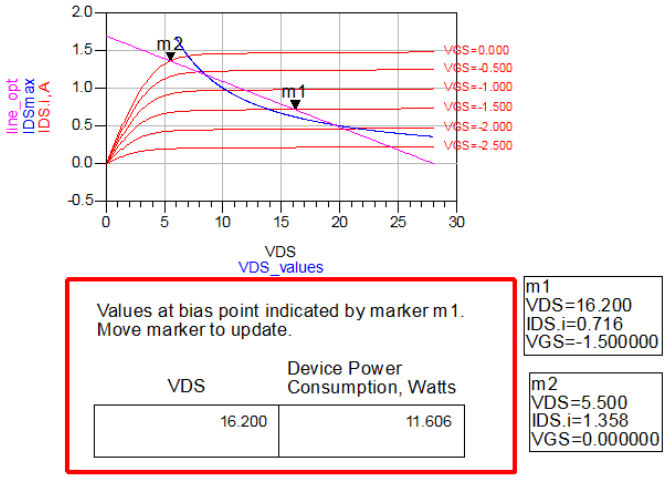

Figure 7-1DC operating point of CGH40006P

7.3 Load-Pull analysis at DC Bias

ADS template performs only load-pull simulations. However, source impedance is estimated assuming some unilateral behavior for the device.

Following impedances were obtained by load pull simulation at that particular PAE and output power:

$$Z_{LOAD} = 23.534 + j3.250$$

$$Z_{SOURCE} = 6.36 + j1.38$$

$$PAE = 54.98\%$$

$$Power_{delivered} = 38.03\ dBm$$

7.4 Small signal analysis

S parameter analyses were done on the required biasing to obtain small signal parameters of the power amplifier. Initial source and load small signal impedances obtained were as follows:

$$S_{11} = 5.119 + j * 4.704\ \Omega$$

$$S_{22} = 26.33 - j * 6.256\ \Omega$$

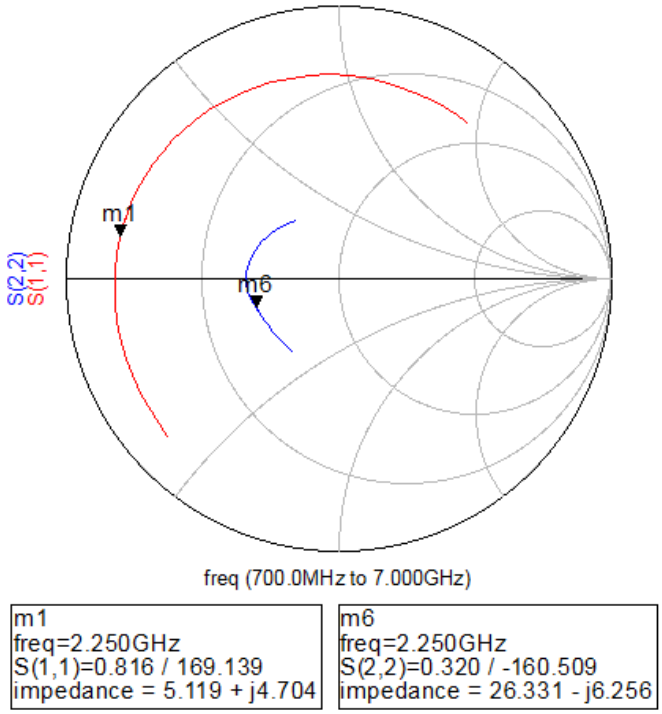

Figure 8-3: Small signal impedances at 2250 MHz

7.5 Small signal matching

Due to bilateral nature of transistor, initially only input side was matched first. For proper matching it was desirable to add series transmission line with open stub in between source and transistor input. Impedances of both of these transmission lines were kept $Zo/\sqrt{2}$ for minimum power loss.

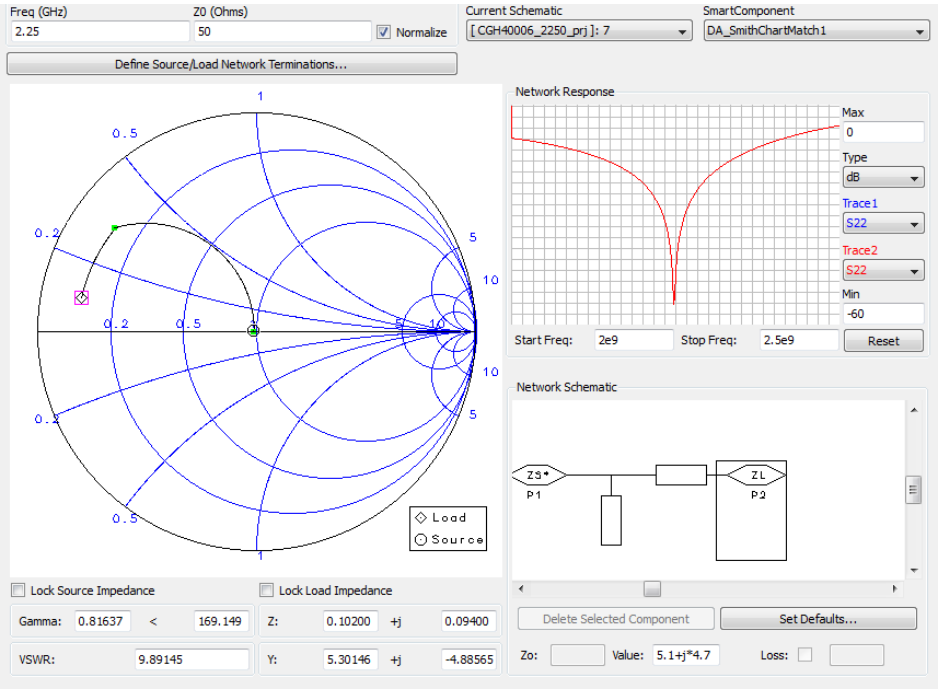

Figure 8-4: Input matching of small signal impedance

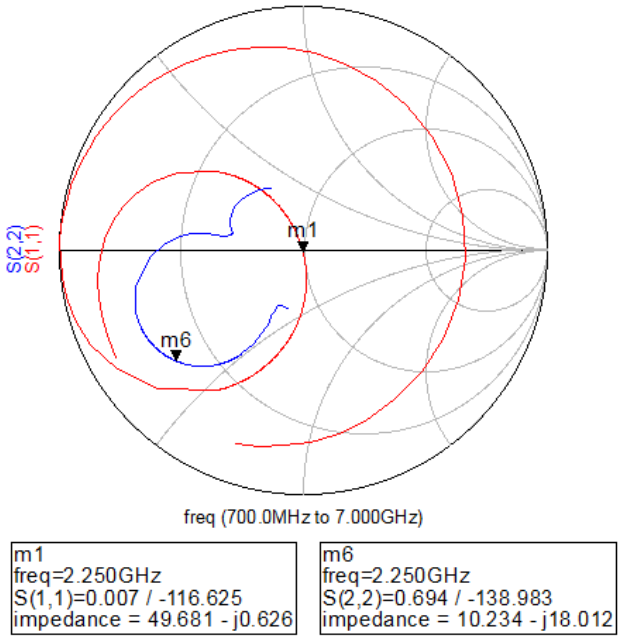

Figure 8-5: Output impedance corresponding to matched small signal input impedance

Small signal load impedance has now become 10.234 - j*18.012 Ω. now conjugate of this impedance would be matched with the transmission lines at the output.

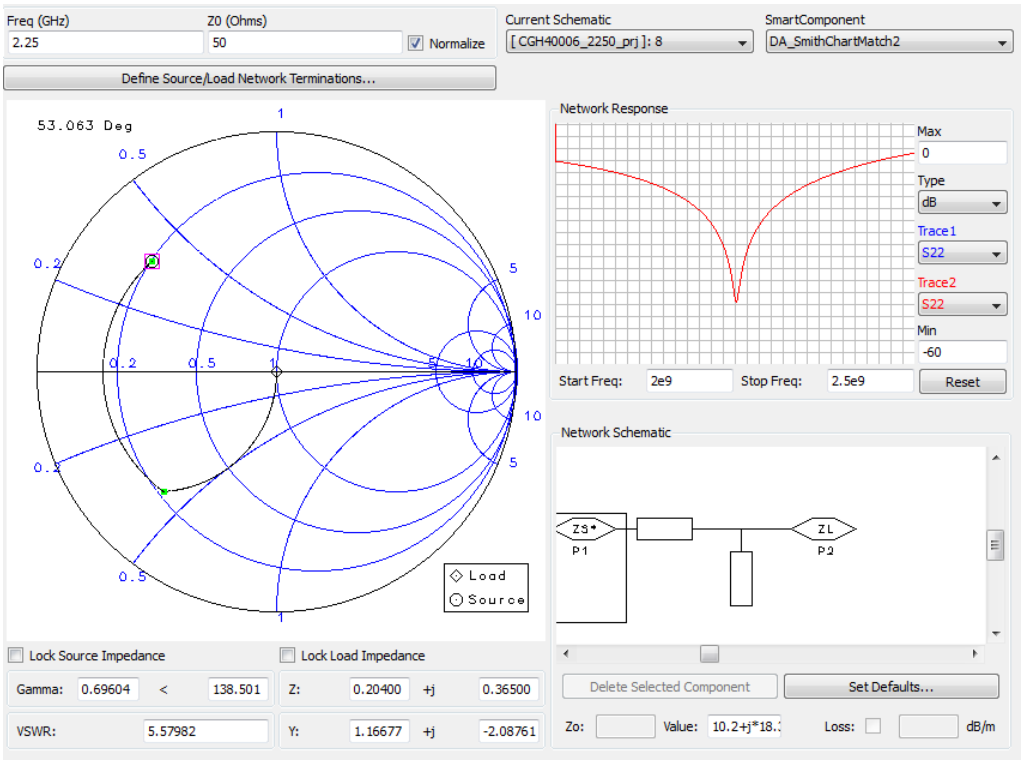

Figure 8-5: Output matching of small signal impedance

The bilateral nature of transistor affects the input matching as well when output is matched. There exist a tradeoff between input and output matching due to this property of transistor. For optimum matched impedances Goal feature of ADS was used to find a suitable result. Optimized reflection losses are shown in following figure:

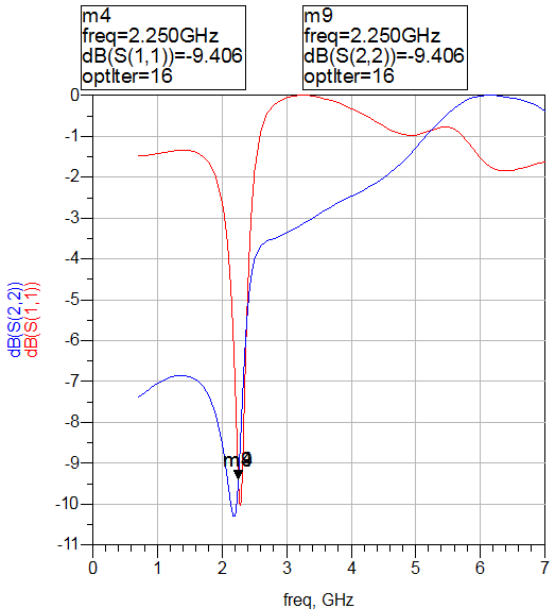

Figure 8-6: Input and output reflection loss corresponding to optimized matching network

7.6 Large signal Impedance matching

1 - With single stub and constant impedance: matching by adding two transmission lines on input and output. One of the transmission line acts as open circuit stub. In this topology the impedance of both transmission lines are kept same while impedance matching is done by changing electrical length of transmission line only.

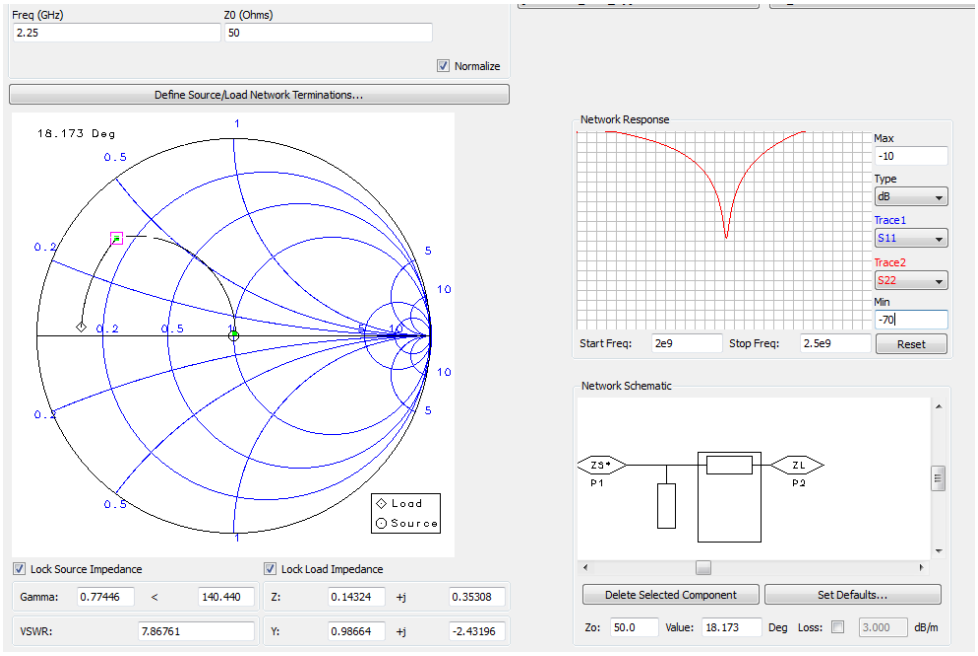

Figure 8-7: Input matching of large signal impedance with double stub

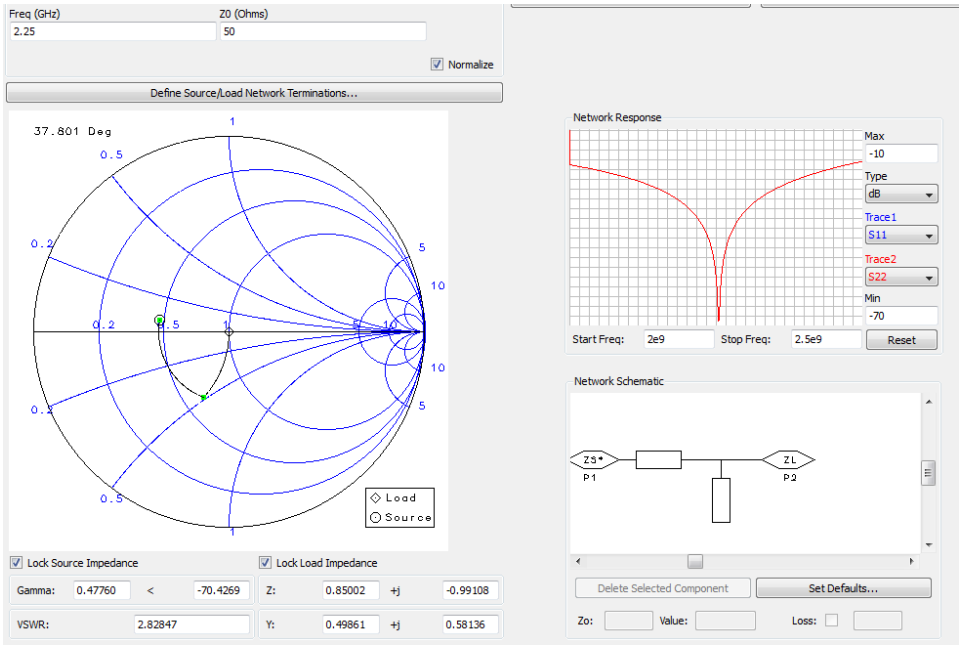

Figure 8-8: Output matching of large signal impedance with double stub

Harmonic balance simulation on matched network gives 37.335 dBmpowers with a gain of 7.335 dB as depicted in figure

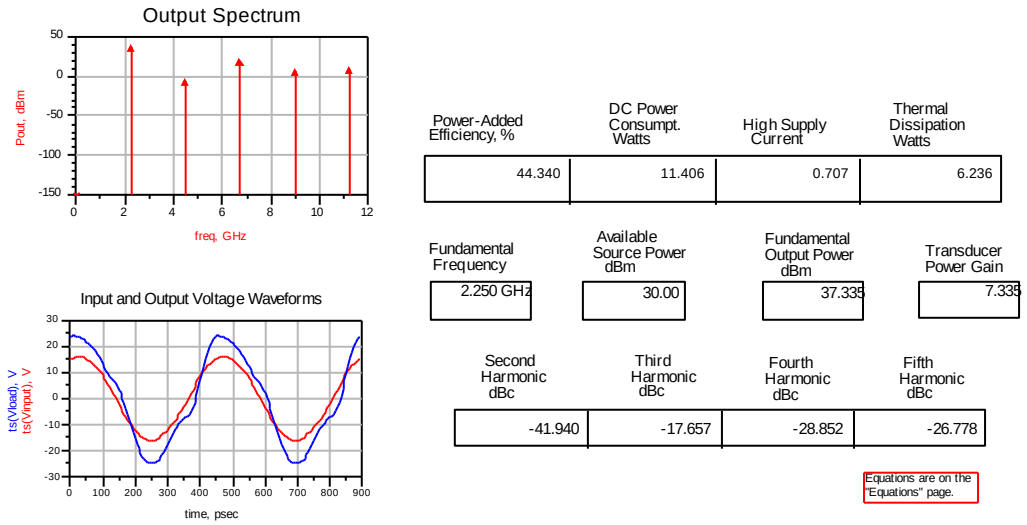

Figure 8-9: Amplifier performance with double stub matched networks

Large signal impedance was matched with Ideal Transmission Line. For realization on hardware, matching circuit should comprise of any of the real transmission lines. for this purpose we have utilized ADS Line Calc tool to calculate width and length of Micro strip Transmission lines corresponding to electrical length and impedance calculated for matching the large signal impedance. for the purpose of DC isolation, a butterfly stub (double radial stub) is also placed after matching network to isolate RF with DC portion. Following figures depict schematic and layout of matched circuit implemented with micro strip lines:

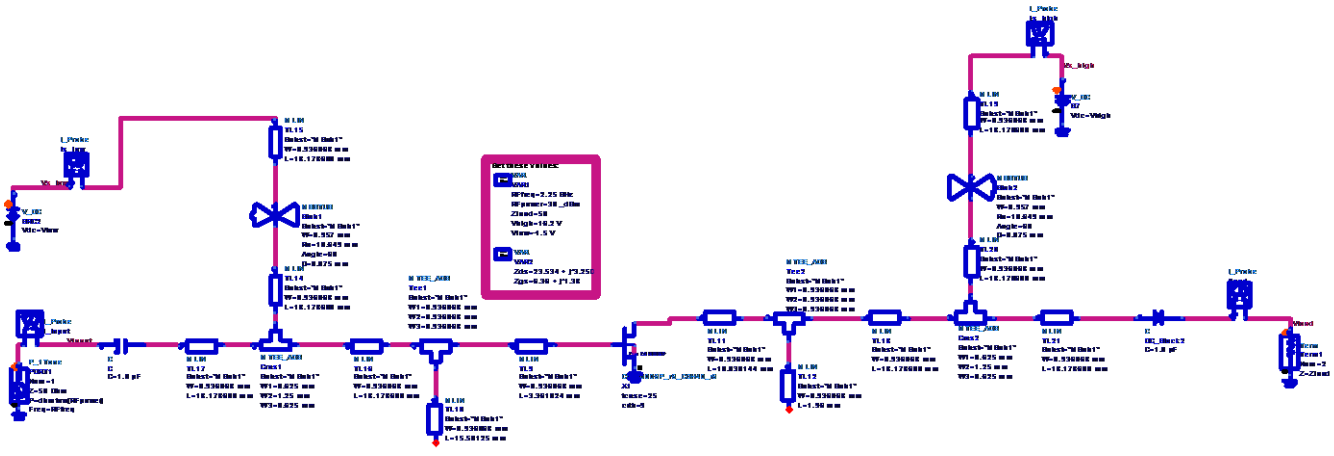

Figure 8-10: Micro strip realization with double stub matching

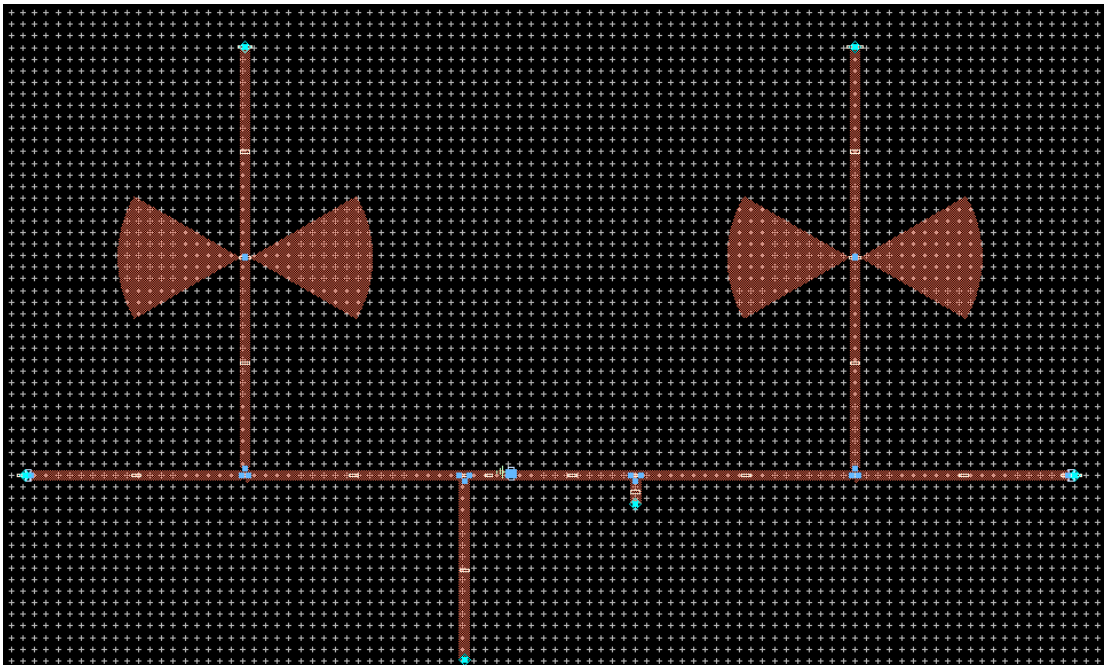

Figure 8-11: Layout of micro strip realization with double stub matching

2 – without stub by varying line impedance: matching by adding a single transmission line. Impedance of that piece of transmission line is varied in addition to electrical length for require matching.

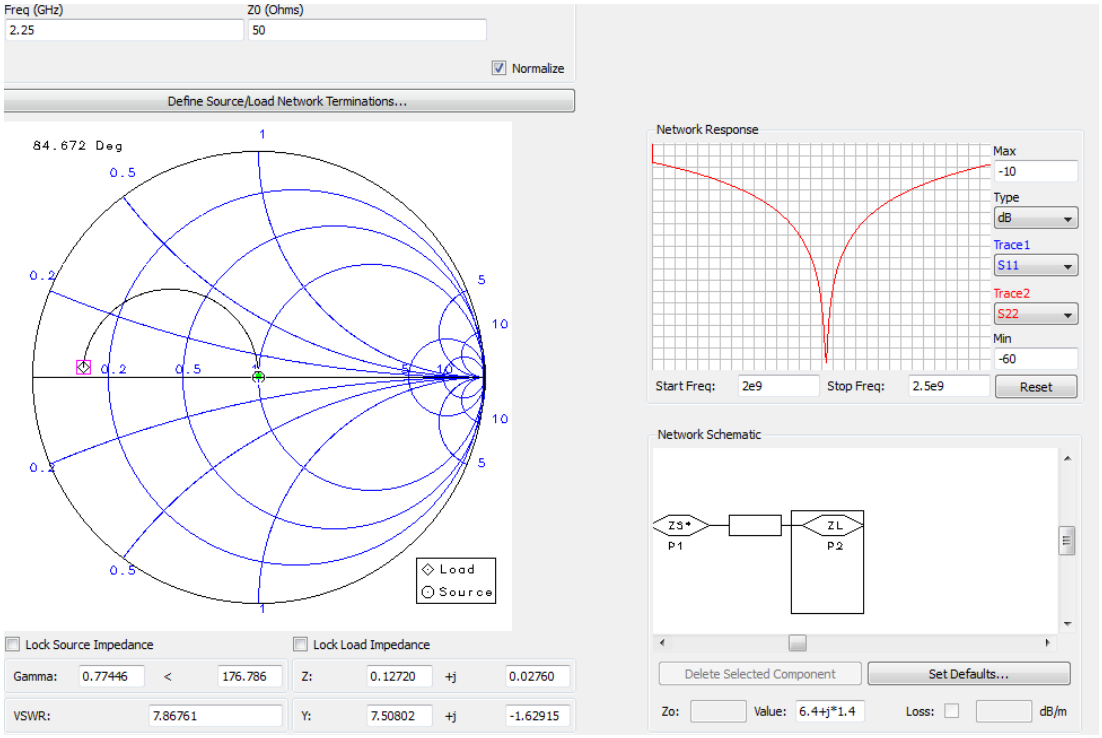

Figure 8-12: Input matching of large signal impedance with single stub

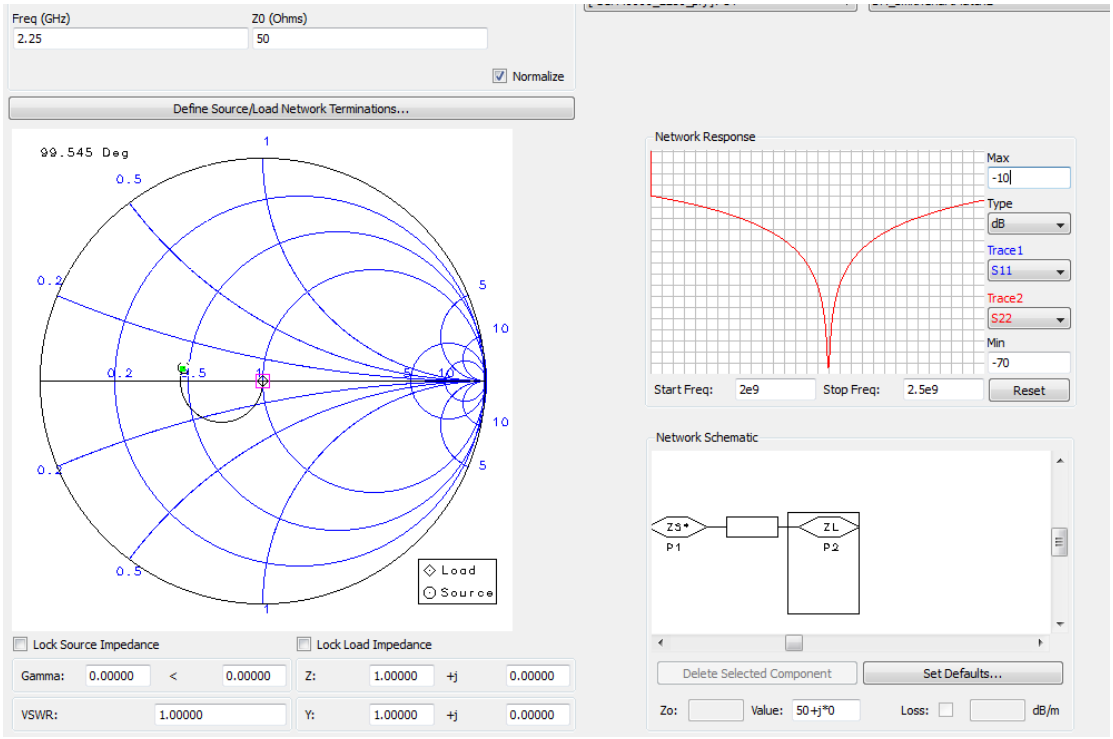

Figure 8-13: Output matching of large signal impedance with single stub

harmonic balance simulation on matched network gives 38.369 dBm power with a gain of 7.369 dB as depicted in figure

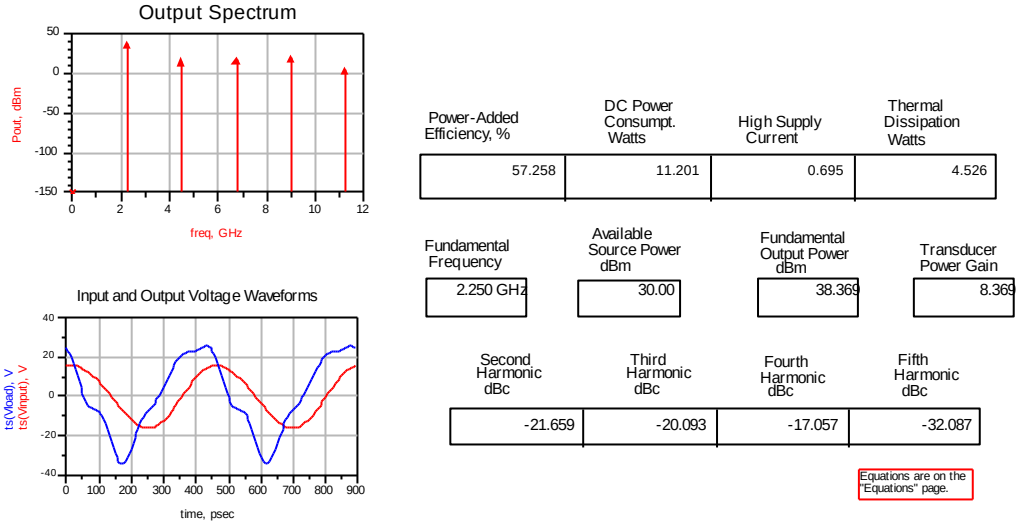

Figure 8-14: Amplifier performance with single stub matching networks

Micro strip realization of this type of matching network is depicted in following figures:

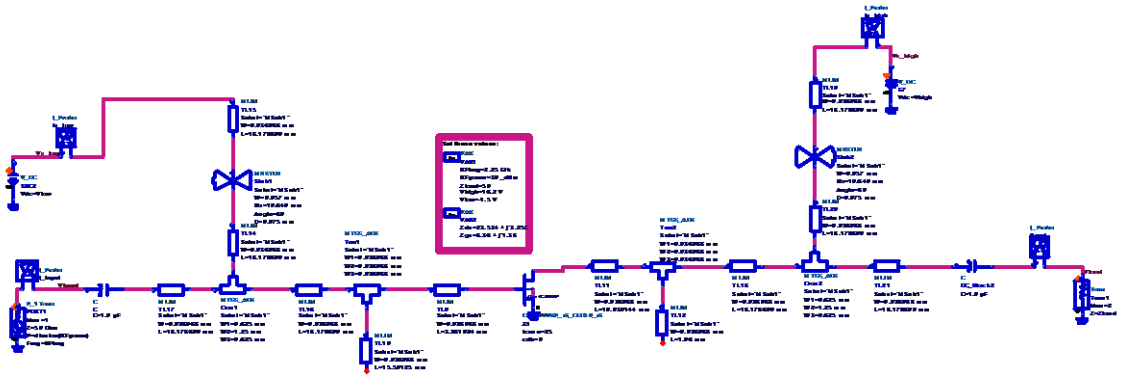

Figure 8-15: Micro strip realization with single stub matching

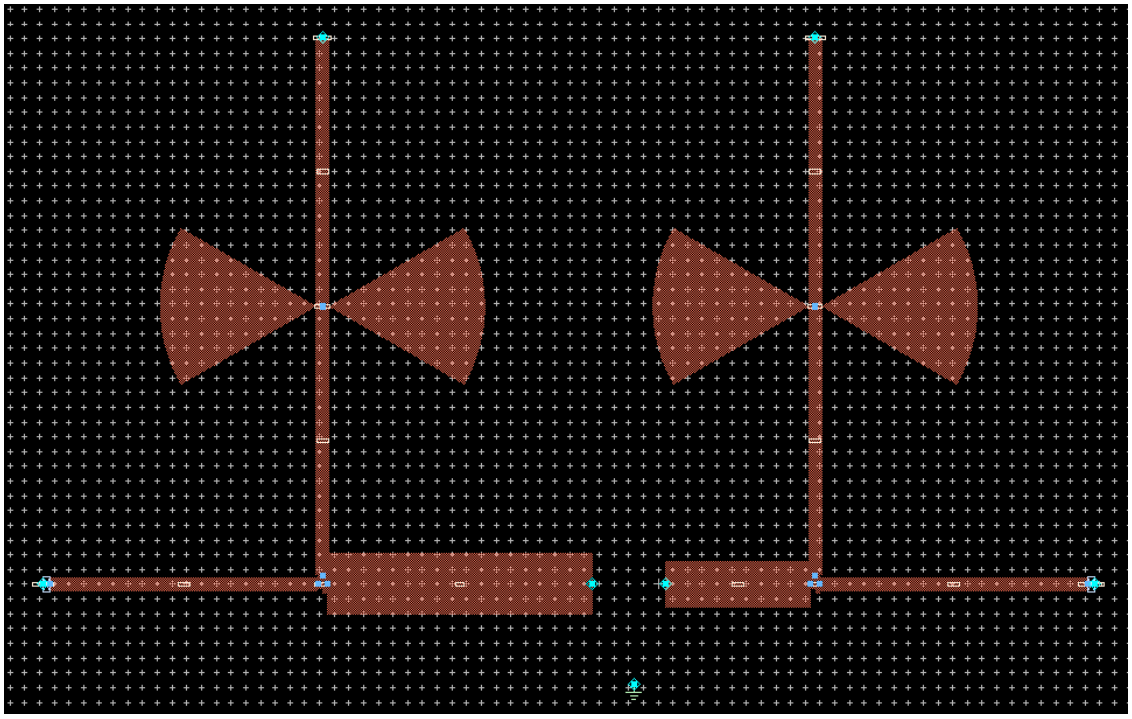

Figure 8-16: Layout of micro strip realization with single stub matching

7.7 Non-Linear Analysis

Non-linear harmonic balance analysis has yielded following main characteristics of the Power Amplifier:

Pin_dBm	Pload_dBm	Transducer_P_Gain
21.062	36.936	15.874

These results are further explained in following sections

7.7.1 Gain analysis

Harmonic balance simulation was carried out with variation of input power. Power curves of amplifier were obtained by it, which was then utilized to find out 1dB compression power and gain.

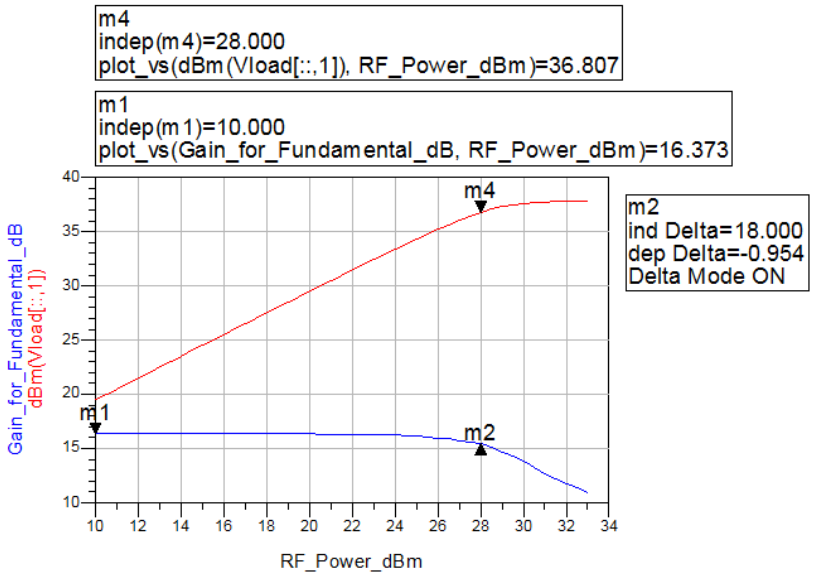

Figure 8-17:P1dB and G1dB of amplifier

Power Added Efficiency was also calculated to find out the performance of the amplifier. Maximum PAE of 38.85% was obtained as depicted in following figure:

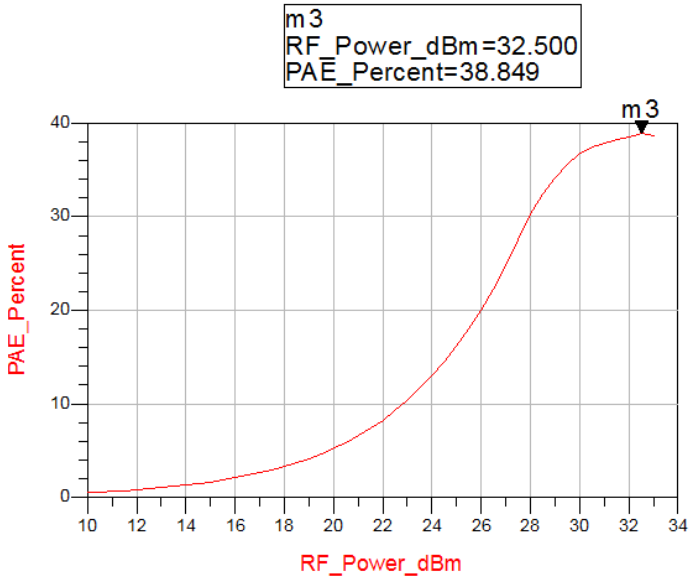

Figure 8-18: PAEvs Input Power

7.7.2 Inter-modulation distortion analysis (Two tone test)

Inter-modulation distortion produced by the amplifier was determined by Two Tone Testing on input side. In this test, in addition to power sweep, input signal of 2MHz frequency spacing was

given to observe different inter-modulation products. Spectrum output to Two Tone Test on a maximum power input is shown in following figure:

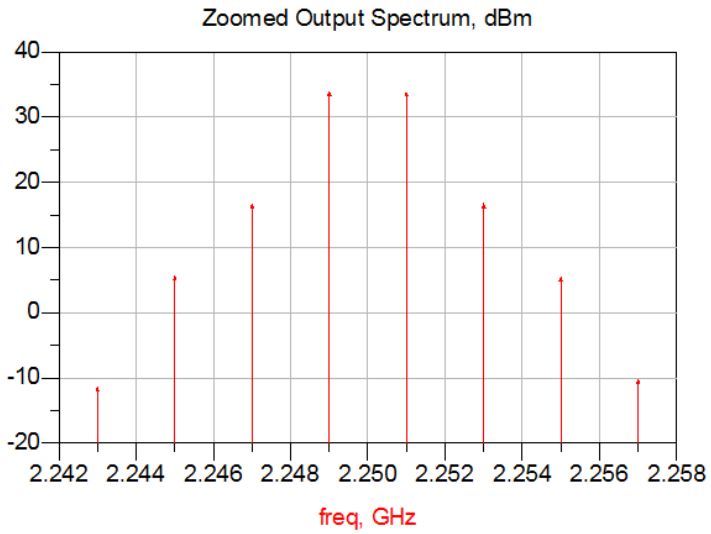

Figure 8-19: Two Tone Test spectrum

Power variation of fundamental and third order harmonic is shown in following figure:

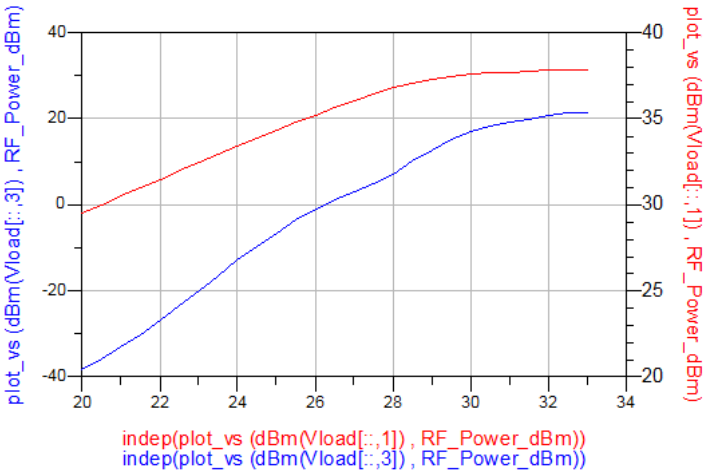

Figure 8-20: Fundamental and third order harmonic

Resultant TOI points obtained are found to be 5dB above P1dB point.

Low and High Side Output TOI Points, dBm

42.62191	42.42838

CHAPTER 6

MEASURED RESULTS AND ANALYSIS

8 Measured Results Analysis

8.1 Pout measurement results

The two stages of power amplifier were tested giving input signal of 2.25GHz and 2.1 GHz and 1 dB compression point is determined, the measured one tone test results are presented in table below,

Table 8.1-1 One tone test results

Input power (dbm)	Frequency (f1)Mhz	Fundamental power (dbm)	Frequency (f2) Mhz	Fundamental power (dbm)
-20	2.25GHz	-8.3	2.1GHz	-8.06
-15		-3.25		-3.12
-11		0.8		1.01
-10		1.91		1.91
-9		2.89		2.86
-8		3.78		3.69
-7		4.83		4.42
-6		5.63		4.99

-5		6.34		5.48
-4		6.8		5.82
-3		7.06		5.99
-2		6.94		6.06
-1		6.95		6.09

Pin vs. Pout graph is plotted using MATLAB at our desired frequency which is 2.25 GHz is shown in figure 7.1

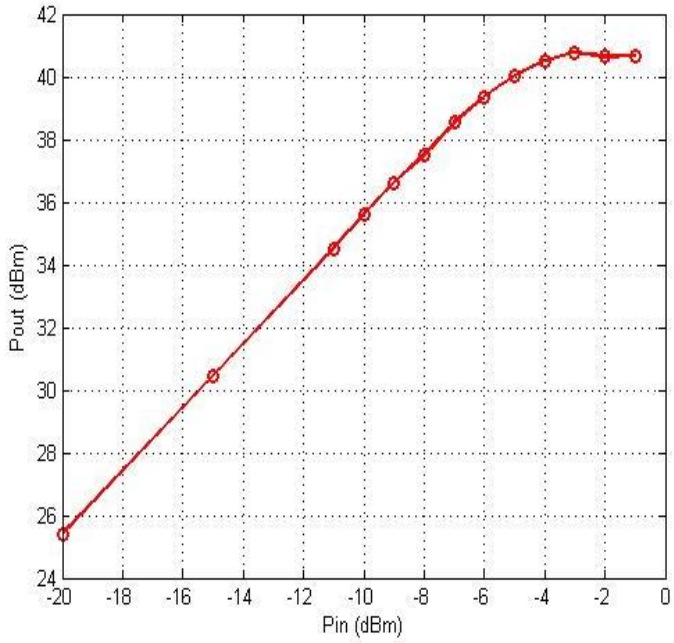

Figure 8-1 Pout in dBm at different input power levels of driver and power amplifier stages

The power spectrum results of Agilent Spectrum analyzer are presented with the output 32dBm attenuated for frequency range of 1.8 and 2.5GHz, showing the gain of amplifier at range of frequencies in figure 7.2

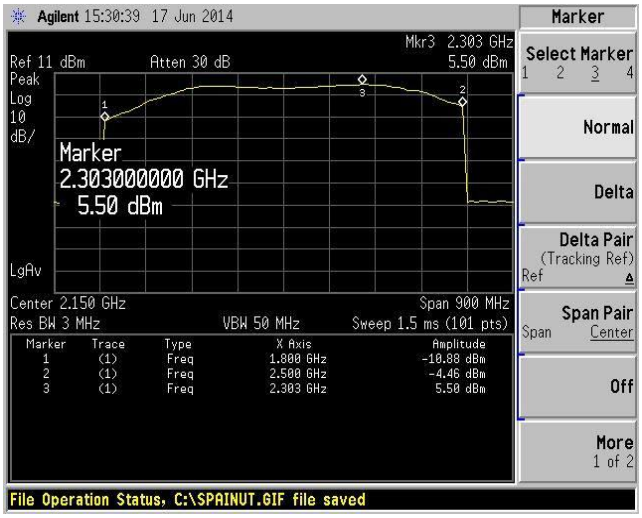

Figure 8-2 Pout in dBm at specific point of frequencies with 32.7dB of attenuation

The power added efficiency is calculated using the formula

By giving frequency sweep on constant power level, PAE is calculated at each point of frequency and plotted, the power amplifier stage has a PAE of about 51.4%.shown in figure 7.3

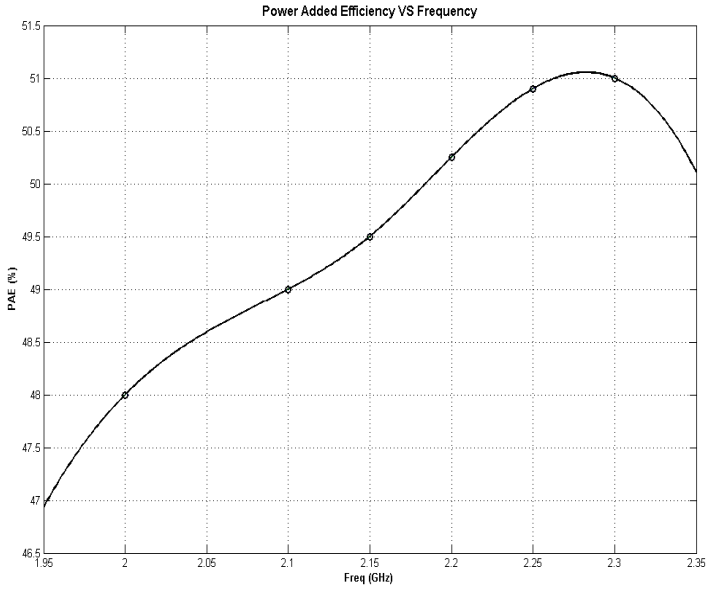

Figure 8-3 PAE of Power amplifier stage

Developed driver state using BOWEI IC, final design snapshot shown in figure 7.4

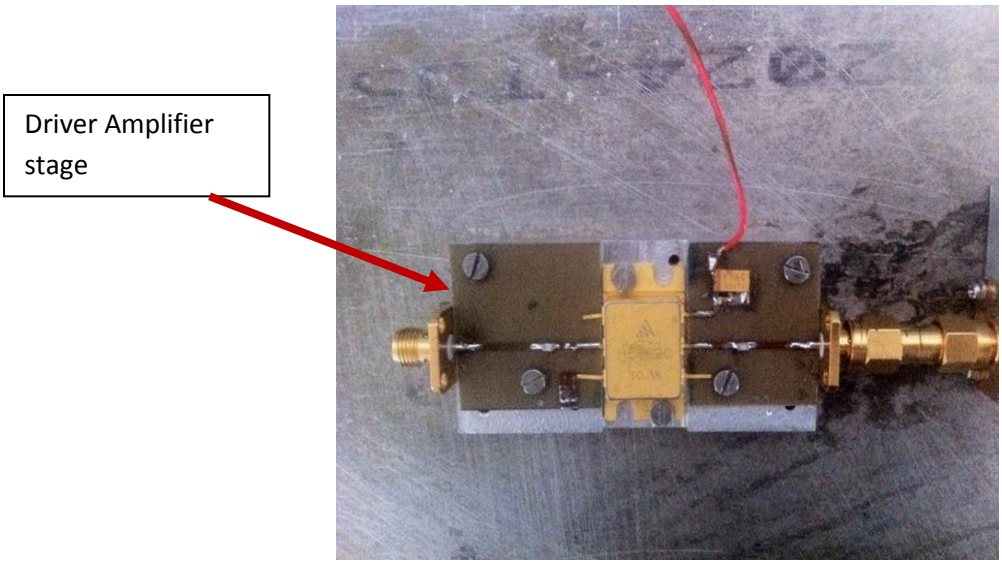

Figure 8-4 Driver stage amplifiers

Developed Power amplifier stage using EudynaFLL-120MK final design with biasing wires shown in figure 7.5

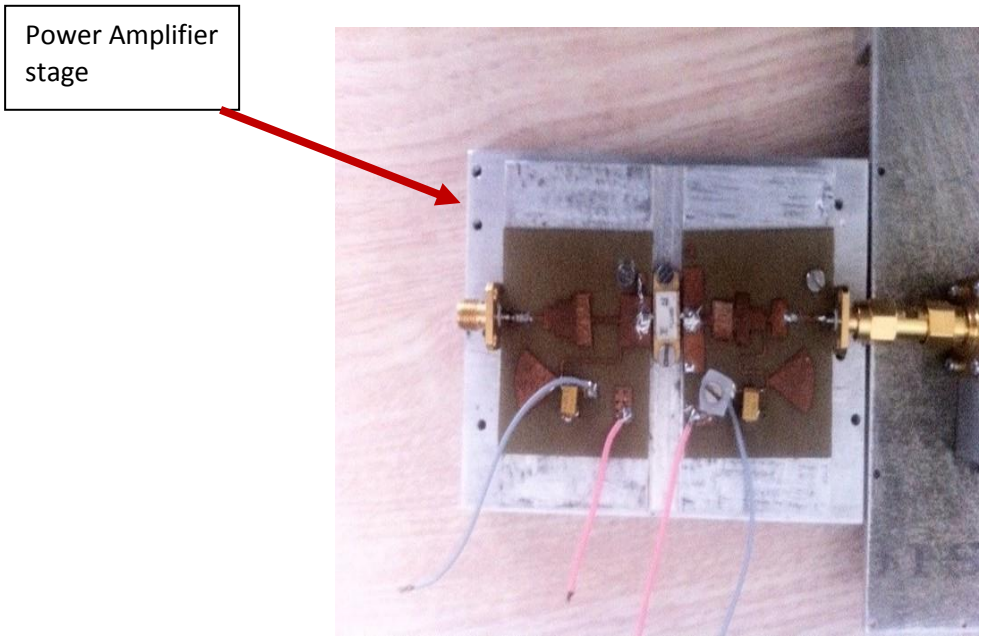

Figure 8-5 Power Stage Amplifier

Snap shot of complete DUT with isolator for protection in between is shown in figure7.6

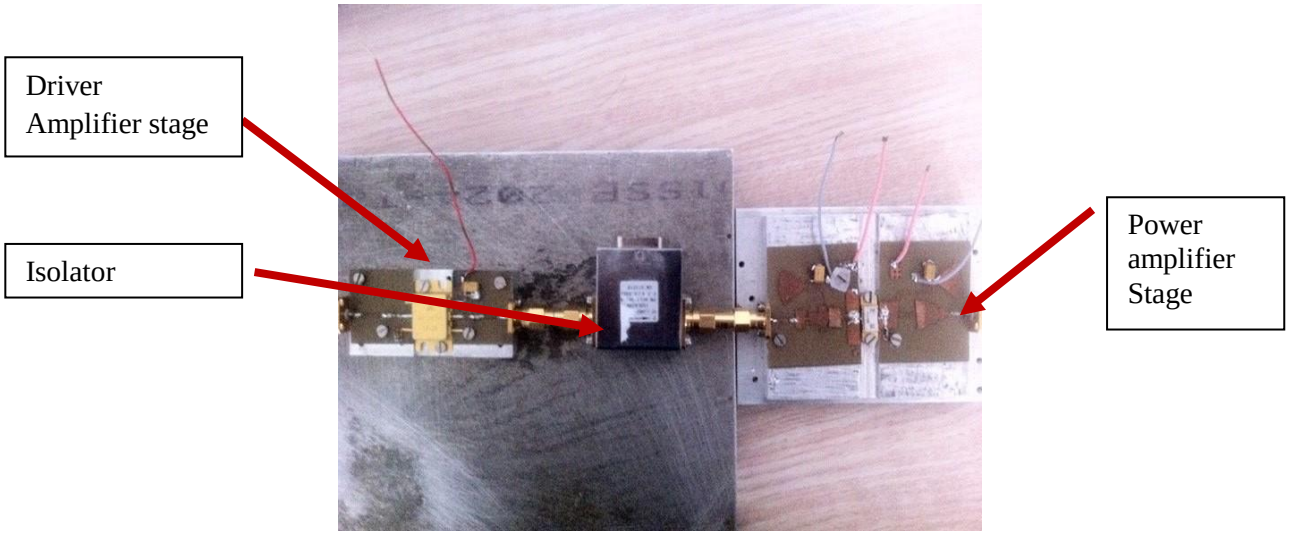

Figure 8-6 Power Amplifier with driver stage and isolator

Power Amplifier stage is shown is figure 7.7

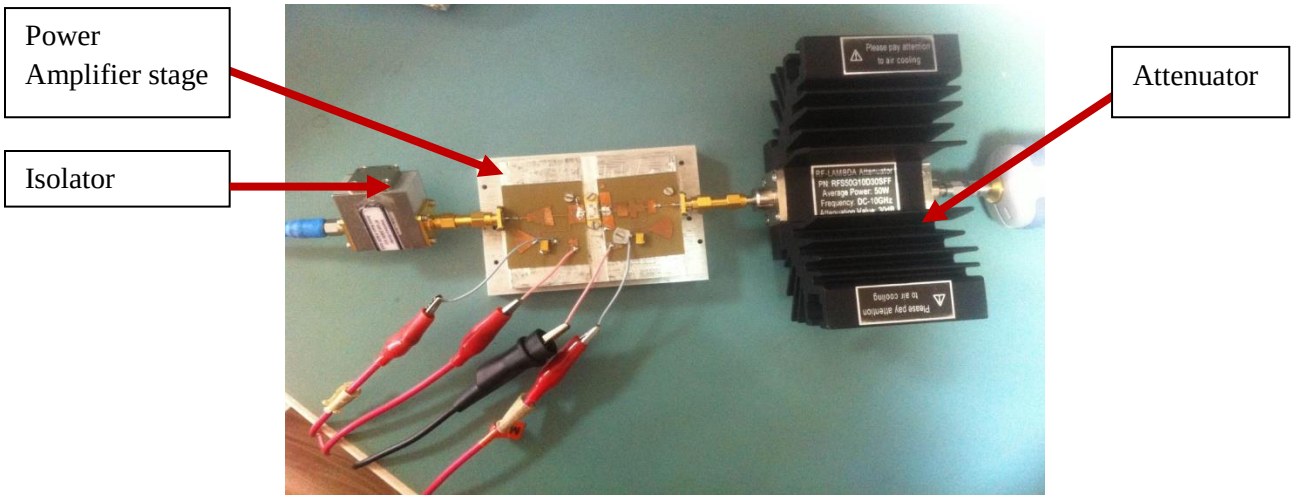

Figure 8-7 Power Amplifier DUT tested with 30dbm attenuator

Input signal applied with 32dBm attenuation shown in figure 7.8

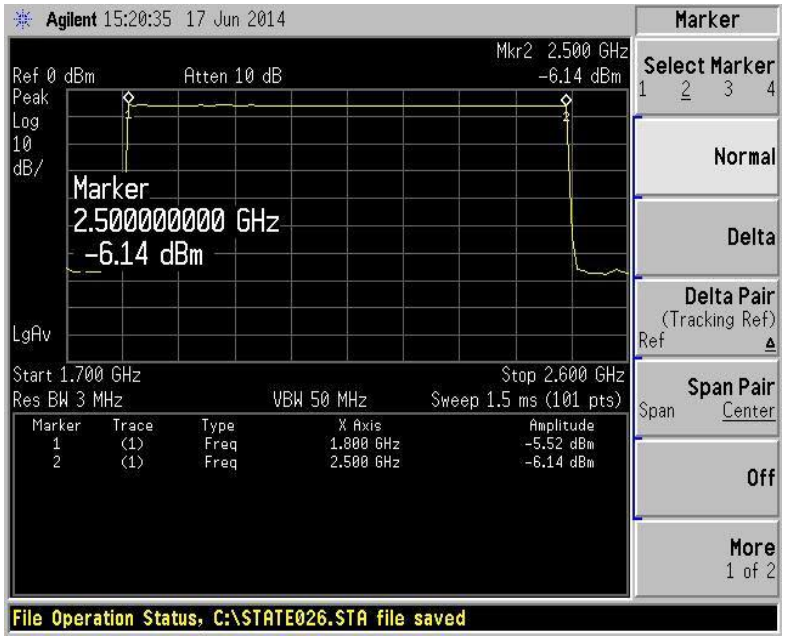

Figure 8-8 Attenuated Input Signal in the frequency range of 1.8GHz and 2.5GHz

Attenuated output form DUT attenuator used is 32dBm in the range of 2.25-2.5GHz

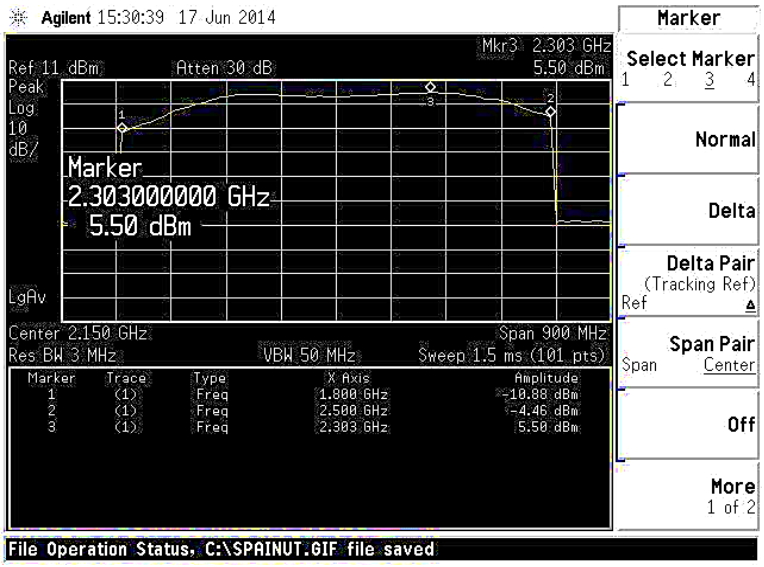

Figure 8-9 Attenuated final output at frequency range of 1.8GHz to 2.5 GHz

8.2 Procedure for measuring inter-modulation performance

Connect the two signal generators to Wilkinson Power Combiner and connect the output ofWilkinson Power divider to RF spectrum analyzer through an attenuator. The frequency

spacing should be at least 2MHz with fundamental at 2.25GHz i.e. 2249 MHz and 2251MHz respectively. Observe the third harmonic at 2f1-f2 which is 2247MHz and 2f2-f1 which is 2253MHz.

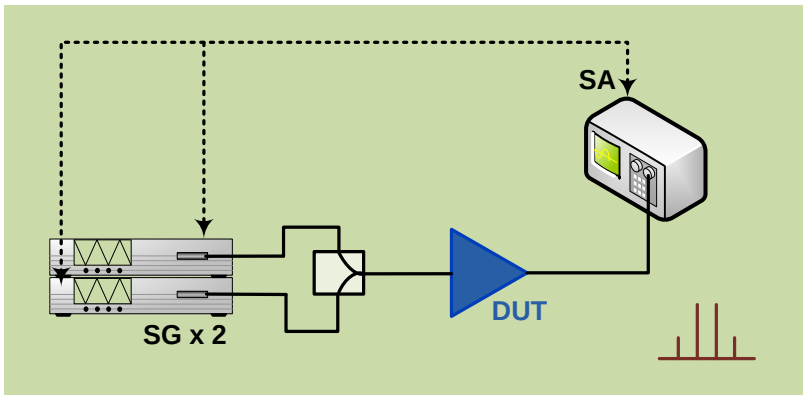

Figure 8-10 Two tone test setup

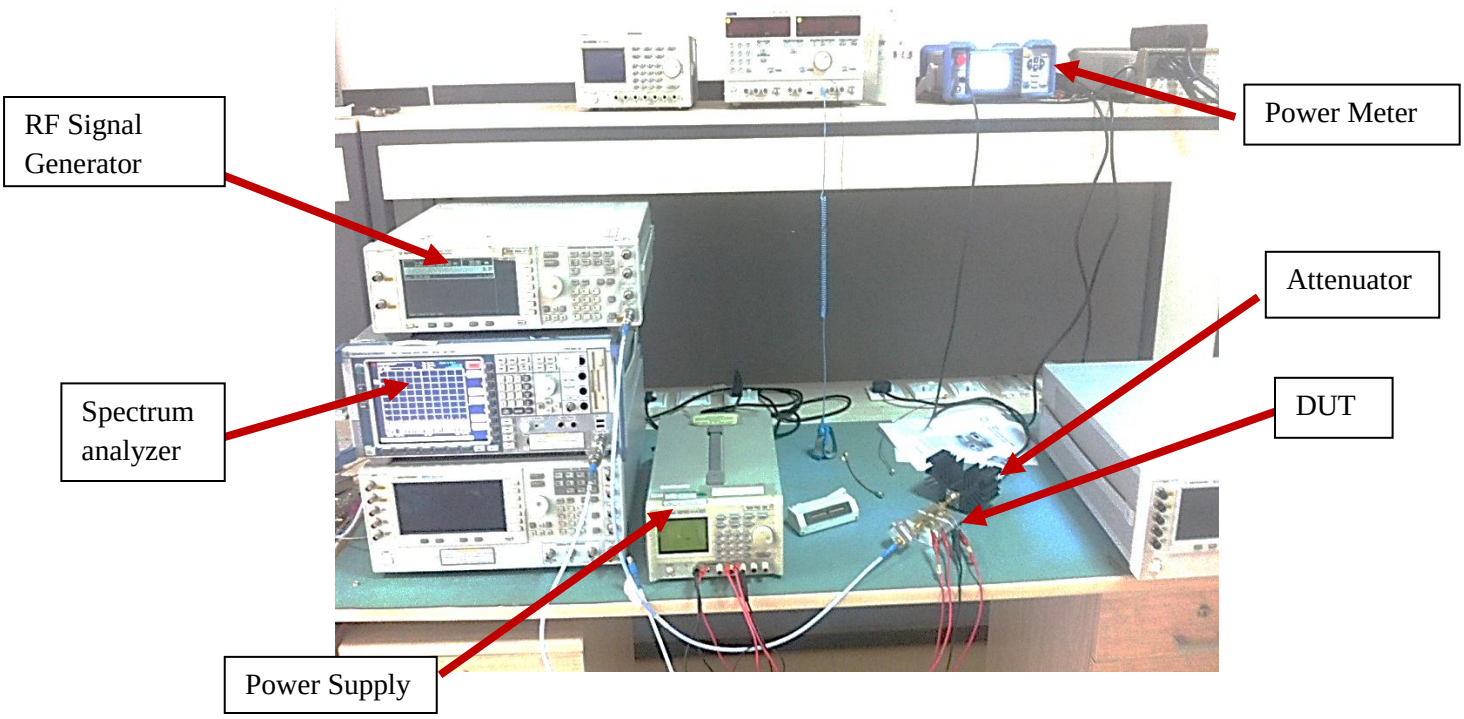

Figure 8-11 Test Setup

The measurement results for two tone testing is described in the following section

8.2.1 Two Tone Test Setup and Measurements

The two tone results were measured using Agilent Signal generators and Spectrum Analyzers the two frequencies used were 2 MHz separated taking 2.25GHx as center frequency

Frequency f1:2249GHz

Frequency f2:2251GHz

Third harmonic 2f1-f2:2247GHz

2f2-f1:2253GHz

Table 8.2-1 Two tone test results

Input power (dbm)	Frequency (f1)Mhz	Fundamental power (dbm)	Frequency (f2) Mhz	Fundamental power (dbm)-32dB(attn)	Third harmonic (Mhz) 2f1-f2	Third order power (dbm)	Third harmonic (Mhz) 2f2-f1	Third order power (dbm)
-20	2249	-12.8	2251	-13.5	2247	-62	2253	-65
-15		-7.6		-8.29		-51.5		-53
-11		-3.39		-3.97		-40.1		-40.4
-10		-2.53		-3.12		-37.1		-39.1
-9		-1.59		-2.25		-33.9		-35.5
-8		-0.7		-1.35		-29.50		-31.5
-7		-0.08		-0.60		-24.9		-24.8
-6		0.56		-0.03		-20.3		-20.1

-5		0.87		0.28		-16.59		-17.3
-4		1.05		0.45		-14.23		-14.19
-3		1.16		0.50		-12.64		-13.07
-2		1.17		0.59		-11.49		-11.9
-1		1.18		0.60		-10.66		-10.99

The graph of frequency f1 and third harmonic 2f1-f2 is presented below similarly third order intercept point can also be calculated by plotting f2 and 2f2-f1. The points plotted on matlab shown in figure 7.12 that the third order intercept point is approximately 10db above the P1db of Power amplifier stage which is desired and it measures the linearity of amplifier.

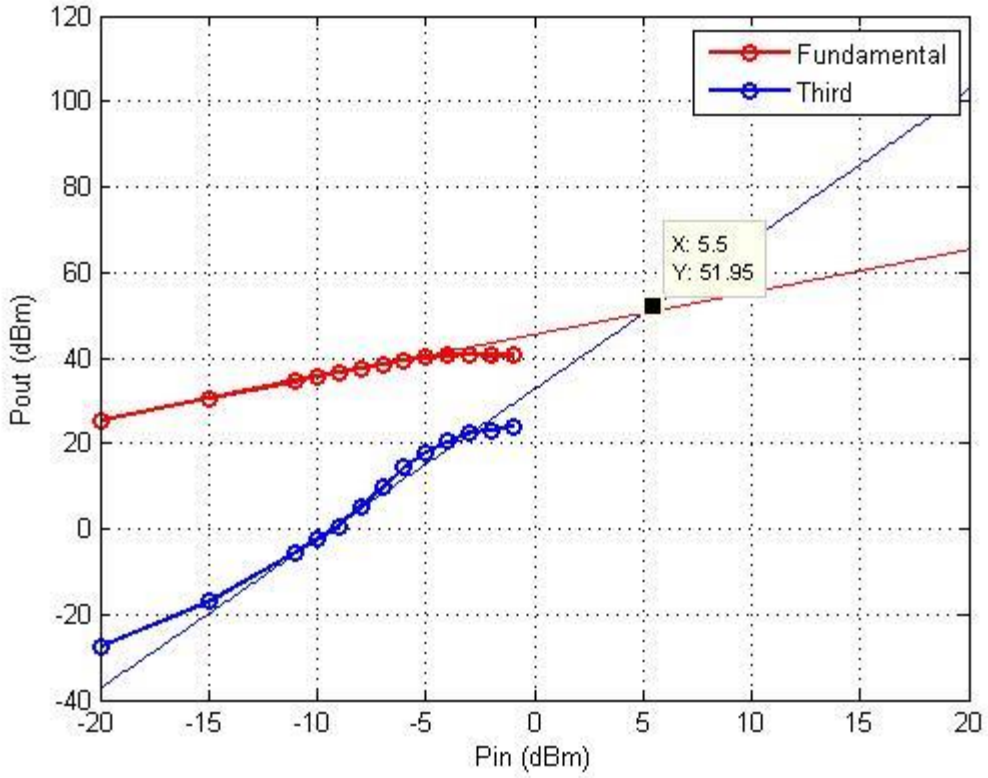

Figure 8-12 Inter-modulation distortion products at 2.25GHz

Hence, Simulation result of S-parameters is verified by measuring Pout of Power amplifier. It achieved required gain and Pout in the same frequency range as simulated.

CHAPTER 7

CONCLUSION

9 Conclusion and Future work

The S band range of 2-2.3Ghz also has applications in LTE (Long term Evolution) of UMTS (Universal mobile telecommunication system). Utilizing the gain of S-band amplifier which is 43dbm it can be used in LTE applications. Testing for amplifier for downlink of LTE data can be done by using OFDMA (Orthogonal frequency domain multiple access). LTE is a standard and its power amplifiers have certain specifications, by slight changing of specifications our amplifier can be used in LTE applications but rigorous testing in this regard will be required. Two tone testing is required to be done, in which two separate signals will be combined and given input to device under test (DUT) [5]. Moreover the designed amplifier can be used in balanced configuration which enables broad band width operation.This thesis enables the researchers to avail the benefits of SSPA's for use in both communication and radar applications, with further two tone testing; S-band amplifiers can also be used for LTE communication products. With the trend of multi carrier modulation and high data capacity digital communication High power amplifiers are in strong need for lower distortion communication systems. As compared to tube based amplifiers which have less life, less ability to reduce spurious and unwanted harmonics and greater size and weight solid state power amplifiers are current trend of market and are replacing tube amplifiers in communication systems [8]. Thermal efficiency of power amplifier can also be improved for its reliable operation in long term systems.

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ANNEX A S-PARAMETERS OF FLL-120MK EUDYNA

MHZ S MA R 50

500 .959 -168.4 3.136 95.8 .008 31.0 .824 179.4

1000 .953 -176.0 1.617 94.1 .010 45.7 .813 178.8

1500 .953 -179.6 1.170 93.8 .011 64.3 .810 177.7

2000 .951 177.0 .978 92.3 .014 82.4 .792 176.5

2500 .939 172.6 .927 91.4 .021 89.1 .778 174.0

3000 .914 165.1 .936 88.0 .024 93.2 .739 168.3

3500 .885 152.7 .990 80.6 .033 94.6 .695 158.9

4000 .836 134.0 1.106 67.1 .051 88.1 .633 145.1

4500 .766 107.3 1.239 48.2 .067 77.3 .559 128.0

5000 .690 71.6 1.415 23.9 .103 60.5 .477 107.3

ANNEX B MATLAB CODE FOR CALCULATING THIRD ORDER INTERCEPT POINTAND PIN VS POUT GRAPH

```
clearall;
closeall;
clc;
Pin = [-20 -15 -11 -10 -9 -8 -7 -6 -5 -4 -3 -2 -1];
Pout_1 = [-8.3 -3.25 0.8 1.91 2.89 3.78 4.83 5.63 6.34 6.8 7.06 6.94 6.95];
Pout = Pout_1 + 31.5 + 2.21;
Poutp = [-62 -51.5 -40.1 -37.1 -33.9 -29.50 -24.9 -20.3 -16.59 -14.23 -12.04 -11.49 -10.66];
Pout3 = Poutp + 3.1 + 31.5;
Poutp_1 = 14:3:50;
plot (Pin,Pout, '-ro', 'LineWidth', 2);
holdon;
plot (Pin,Pout3, '-bo', 'LineWidth', 2);
legend ('Fundamental','Third');
xlabel('Pin (dBm)');
ylabel('Pout (dBm)');
% xlim ([-20 20]);
% ylim ([-30 80]);
gridon;
X_pin = [ones([5 1]) transpose(Pin(3:7))];
b_Pout = regress(transpose(Pout(3:7)),X_pin);
Pin_reg = -20:0.1:20;
Pout_reg = b_Pout(1) + b_Pout(2)* Pin_reg;
X_pin3 = [ones([4 1]) transpose(Pin(3:6))];
```

```
b_Pout3 = regress(transpose(Pout3(3:6)),X_pin3);

Pout3_reg = b_Pout3(1) + b_Pout3(2) * Pin_reg;

plot (Pin_reg,Pout_reg, 'red');

plot (Pin_reg,Pout3_reg, 'blue');

% plot (Pin,Poutp_1);
```

ANNEX C MATLAB CODE FOR CALCULATING POWER ADDED EFFICIENCY

```
clearall;
closeall;
clc;
freq = [2 2.05 2.1 2.15 2.2 2.25 2.3 2.4];
pae = [50 53 55 57 60 62 62 60];
freq_q = 2:0.001:2.4;
pae_q = interp1(freq,pae,freq_q,'spline');
plot(freq,pae,'o',freq_q,pae_q,'LineWidth',2);
holdon;
gridon;
%xlim([1.95 2.35]);
xlabel('Freq (GHz)','FontWeight','bold');
ylabel('PAE (%)','FontWeight','bold');
title('Power Added Efficiency VS Frequency','FontSize',12,'FontWeight','bold');
```