# Experimental Investigation of the effects of Potential Induced Degradation of Poly-crystalline Photovoltaic Modules

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**Session 2018-20**

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**US-Pakistan Center for Advanced Studies in Energy (USPCAS-E)**

**National University of Sciences and Technology (NUST)**

**H-12, Islamabad 44000, Pakistan**


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Date: _____

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# Certificate

This is to certify that work in this thesis has been carried out by **Ms. Quratulain Jamil** and completed under my supervision in Solar laboratory, US-Pakistan Center for Advanced Studies in Energy (USPCAS-E), National University of Sciences and Technology, H-12, Islamabad, Pakistan.

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# Abstract

Potential induced degradation (PID) is one of the most critical degradation phenomena, affecting the reliability of photovoltaic solar modules by causing power losses up to 30% on the system level. In this research, PID is induced on poly-crystalline modules in an environmental chamber in accelerated temperature and humidity conditions under the application of high voltage stress to investigate the degradation phenomenon. The primary focus of this paper is to quantify the degradation extent of PV modules with different encapsulant and superstrate/glass types. The encapsulant types investigated in this work are Ethylene-vinyl acetate (EVA) and newly developed Polyvinyl butyral (PVB). The superstrate types investigated are soda-lime glass and quartz. The progression and severity of degradation were determined through Current-Voltage measurements and Electroluminescence imaging, revealing losses in Maximum power and Fill-factor. The leakage current was measured during the entire PID test and no correlation between leakage current and power was observed. It was demonstrated that the PID loss is strongly depending on the electrical and physical properties of the superstrate and encapsulant types. The module with Quartz/EVA configuration experienced lower (17%) PID losses compared to the Soda-lime/EVA module (32%). Similarly, the module with Soda-lime /PVB configuration experienced lower (10%) PID losses compared to the Soda-lime/EVA module (32%). While the module having both the quartz superstrate and PVB encapsulant, experienced the lowest PID with % degradation in power up to only 1%. The extent of degradation is explained based on the electrical and ionic conductivities of the superstrate and the encapsulant.

## Keywords:

Potential Induced Degradation (PID), Poly-crystalline Silicon Solar Modules, Encapsulation, Maximum Power Determination, Electroluminescence Imaging.

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1. **Quratulain Jamil**, Nadia Shahzad, Hassan Abdullah Khalid, Saeed Iqbal, Adeel Waqas, Afzal H. Kamboh, " ***Experimental Investigation of Potential Induced Degradation of Poly-crystalline Photovoltaic Modules: Influence of Superstrate and Encapsulant Types****"*, under review in "Sustainable Energy Technologies and Assessments".

# List of Abbreviations

| | |
|---|---|
| **PID** | Potential induced degradation |
| **STC** | Standard testing conditions |
| **AM** | Air mass |
| **I-V** | Current voltage |
| **ISC** | Short circuit current |
| **VOC** | Open circuit voltage |
| **Pmax** | Maximum power output |
| **Vmax** | Maximum power point voltage |
| **Imax** | Maximum power point current |
| **c-Si** | Crystalline silicon |
| **FF** | Fill factor |
| **EL** | Electroluminescence imaging |
| **EVA** | Ethylene vinyl acetate |
| **PVB** | Poly vinyl butyral |
| **PET** | Polyethylene terephthalate |
| **VA** | Vinyl acetate |
| **ARC** | Anti-Reflective coating |
| **RH** | Relative humidity |

# Chapter 1

# Introduction

## 1.1 Photovoltaics

Photovoltaics is defined as a process that converts sunlight directly into electricity using solar cells. A photovoltaic cell (PV) cell is basically a semiconducting material that converts the sun rays into electrical energy. The Photovoltaic effect was first time discovered by a French Scientist Edmond Becquerel in the year 1839 [1]. Since then, a variety of PV cells have been developed and great advancements have been made in the PV industry. From single junction crystalline solar cells to thin film technologies including amorphous Si (a-Si) based thin films **solar cells**, Copper Indium Gallium Selenide (CIGS) **solar cells**, Cadmium Telluride/Cadmium Sulfide (CdTe/CdS) **solar cells** to Dye sensitized, Polymer based, organic and concentrated solar cells.

## 1.2 Working of a Solar cell

A typical silicon solar cell is basically a diode that is formed by joining the p-type (usually Boron doped) and n-type (usually phosphorous doped) silicon. When light strikes the surface of a solar cell, the photons easily enter the p-n junction through the thin p-type layer. The light energy in form of photons provides enough energy to the junction and results in formation of electron-hole pairs. The electric field at the p-n junction moves the free electrons towards the n-type of the junction and the holes move towards the p-type side of the junction. The newly created electrons and holes cannot further cross the junction due to barrier potential and are separately extracted to an external circuit contributing to the electric current. In this way solar cell generates electricity [2]. The mechanism of solar cell is illustrated in figure 1.1.

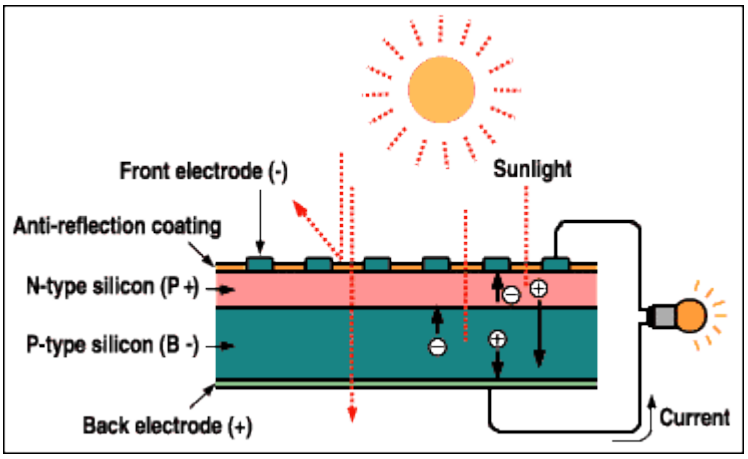


Figure 1.1 Leakage current plotted against voltage applied outside the chamber [2].

## 1.3 Characteristics of Solar Cell

The characteristic curve that is generated by plotting the current against the voltage of the diode is known as IV characteristics of a solar cell. When no light is falling on a solar cell then it acts like a normal diode and is known as Dark IV Characteristics. But when light falls on the solar cell then the light generated current $I_L$ is merely added to the normal dark currents in the diode, so the diode law becomes

$$I = I_O \left[ exp\left(\frac{qV}{nkT}\right) - 1 \right] - I_L \qquad (1)$$

$I$=diode current.

$I_O$=Reverse Saturation current.

$I_L$=Light generated current.

V=Voltage across diode.

n=Ideality factor.

k= Boltzmann constant.

T=Absolute Temperature of p-n junction.

The light has an effect of shifting the I-V Curve to fourth quadrant, from where the power can be extracted as shown in figure 1.2. This I-V curve is mostly represented

as reversed and the output curve is shifted to the first quadrant as shown in figure 1.3. And so, the diode law can be rearranged as in equation 2 [3].

$$I = I_L - I_O \left[ exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (2)$$

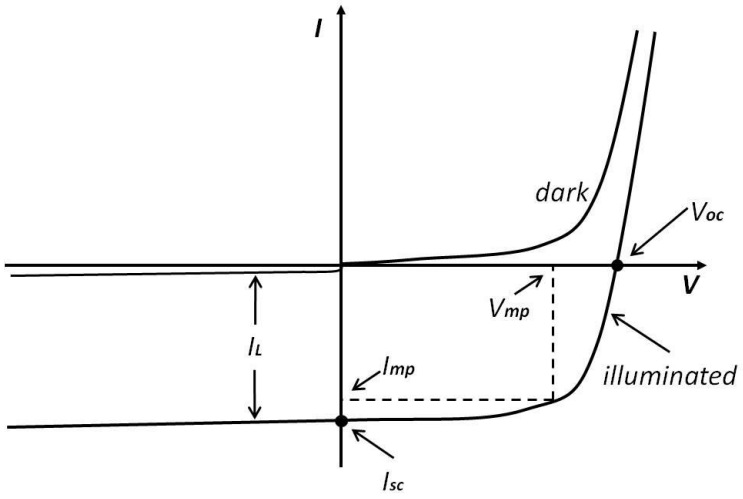


Figure 1.2 Dark and Illuminated I-V Characteristics of a Solar Cell [4].

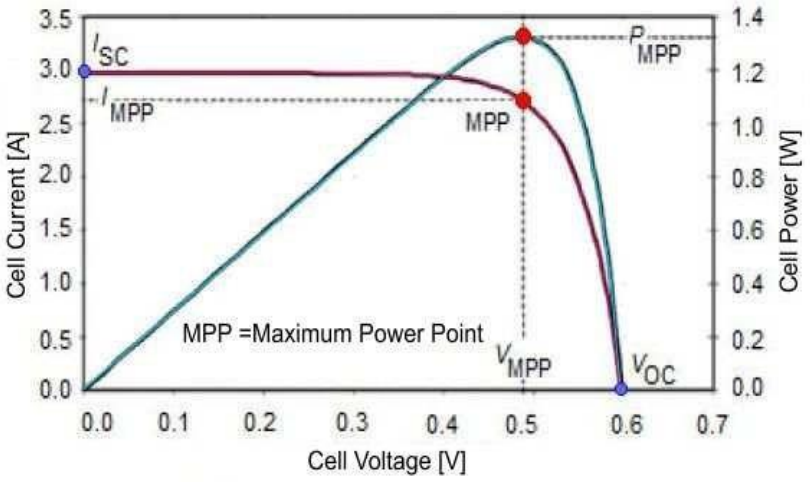


Figure 1.3 Characteristics of a solar cell [5].

The two important limiting parameters used to characterize the output of solar cells is given as:

**1) Short Circuit Current ($I_{sc}$):**

The maximum amount of current as 0 voltages is referred to as short circuit current. V=0, then $I_{sc}=I_L$. Also, the $I_{sc}$ is directly proportional to the light available.

**2) Open Circuit Voltage ($V_{oc}$):**

It is referred to as the voltage at zero current. The value of $V_{oc}$ increases logarithmically with the increasing sunlight.

**3) Maximum Power Point (MPP):**

There is a certain combination of current and voltage at which the power has maximum value, at $V_{mp}$ and $I_{mp.}$ In other words, the point at which the solar cell generates maximum power is known as MPP.

$$MPP= V_{mp}\times I_{mp} \quad (3)$$

**4) Fill Factor (FF):**

Fill factor is the measure of the squareness of the IV Curve. It is the relationship between the maximum power that an array can produce under the normal operating conditions and the product of Open Circuit Voltage and Short circuit current [3].

$$FF=\frac{MPP}{V_{OC}\times I_{SC}} \quad (4)$$

## 1.4 Generations of Solar cell

There are 3 generations of solar cells that include different technologies. Here we will be discussing each one by one.

### 1.4.1 1ST Generation of Solar cell

Generally, 1st generation of solar cells include mono-crystalline and multi-crystalline solar cells. They are the first and the mostly commonly used technology type due to their higher efficiencies. 1st generation solar cells are produced on wafers and if the

whole wafer is only one crystal, it is called Mono-crystalline solar cell. And if the wafer consists of crystal grains, it is called multi-crystalline solar cell. Although mono-crystalline solar cells have higher efficiencies compared to multi-crystalline solar cells, the latter is more commonly used in various applications because of its easier production and lesser cost.

### 1.4.2 2nd Generation Solar cells

The second-generation solar cells also known as thin film technology include amorphous Si (a-Si) based thin films solar cells, Copper Indium Gallium Selenide (CIGS) solar cells, Cadmium Telluride (CdTe) and Cadmium Sulphide (CdS) solar cells. 2nd generation solar cells have less efficiencies compared to 1st generation and are comparatively cheaper. Also 2nd generation technologies have advantages in visual aesthetics and have vast applications in building integrations. Thin film technology can be grown on flexible substrates that add to its advantages. However, thin film materials used in fabrication of the solar cells are difficult to find and cells have much lower efficiencies [6].

### 1.4.3 3rd Generation of Solar cells

3rd Generation of solar cells include 1. Nanocrystal based solar cells 2. Polymer Based Solar cells, 3. Concentrated solar cells 4. Dye sensitized Solar cells. Third-Generation technologies are commercially not proven yet but are promising and novel. Among all the most developed ones are Dye-sensitized solar cells (DSSC's) and concentrated solar cells. DSSC are based on dye molecules between electrodes. Electron-Hole pairs lie in these dye molecules and are transported through $TiO_2$ nanoparticles. DSSC's are cheaper technologies but have very low efficiencies [6]. Also, their fabrication is way easier than other PV technologies. Another promising technology is concentrated solar cells that focus on the principle of concentrating light on smaller region of solar cell. In this way, the amount of semiconductor material can be reduced, decreasing the overall cost.

## 1.5 Efficiencies of Different Generations of Solar Cell

1st generation of solar cells lab-based efficiency is 24.7% and module based is 22.7%. 2nd generation solar cell lab-based efficiency is 18.4% and module based is 13.4%. 3rd generation solar cell efficiencies are very high, greater than 30%. Figure 1.2 represents efficiencies of different generation of solar cells as a function of their cost [6].

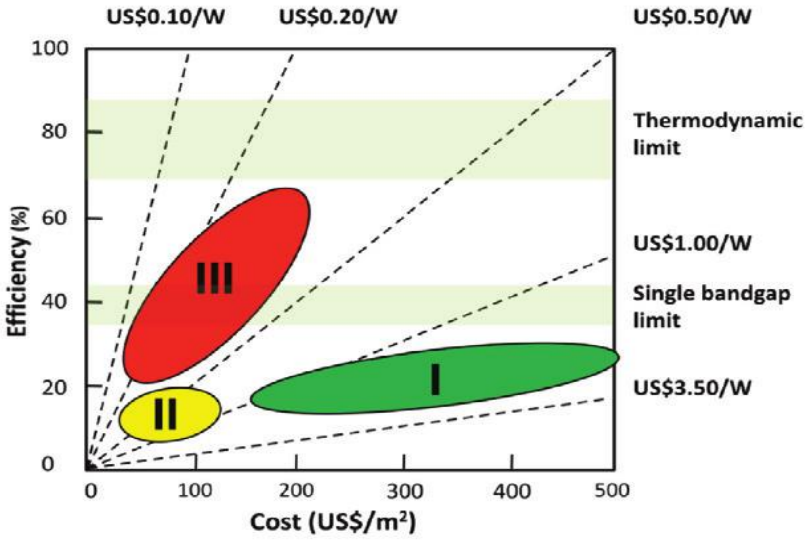


Figure 1.4 Price Vs Efficiency among different generations of solar cell [6].

## 1.6 Solar cell to PV System

A typical multi-crystalline solar cell is capable of producing 0.6V. In cases when higher voltages are a demand, solar cells are connected in series that makes a Module. Modules generally consists of 36 while 60 to 72 cells are used in larger or residential fields.

Module's structure shown in figure 1.3 consist of various parts that includes Front glass that provides mechanical strength and rigidity to module, Encapsulant that is most widely used for lamination is EVA (Ethylene Vinyl Acetate). It has high optical transparency, good electrical insulation and highly adhesive to glass, cells and backsheet. Backsheet is another important component of module structure, provides durability and protects solar cells against corrosion due to moisture and electrically insulates the module. Most commonly used backsheet material is PET (Polyethylene terephthalate). Junction Box consists of one positive and negative terminal and acts as an interface between the external cables and internal circuitry. It contains by-pass diodes that prevents from hotspots. Aluminium frames are used to seal the edges and provide means to firmly mount the PV panel to metal structures. Sealants protect the edges of PV modules from moisture and provides good electrical insulation. Most commonly used sealant is Silicone because of its good adhesion and insulation properties [7].

Modules are then connected in series forming Strings. Strings typically have high voltages to about 600V [8]. While several sets of strings of panels/modules connected in parallel form a solar Array as shown in figure 1.4.

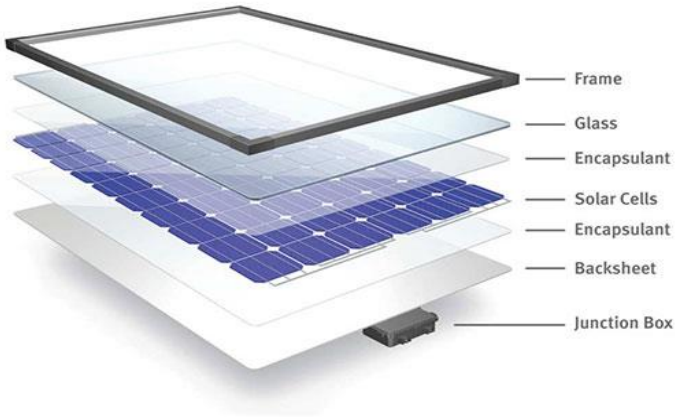


Figure 1.5 Structure of a Crystalline Silicon Photovoltaic module [7].

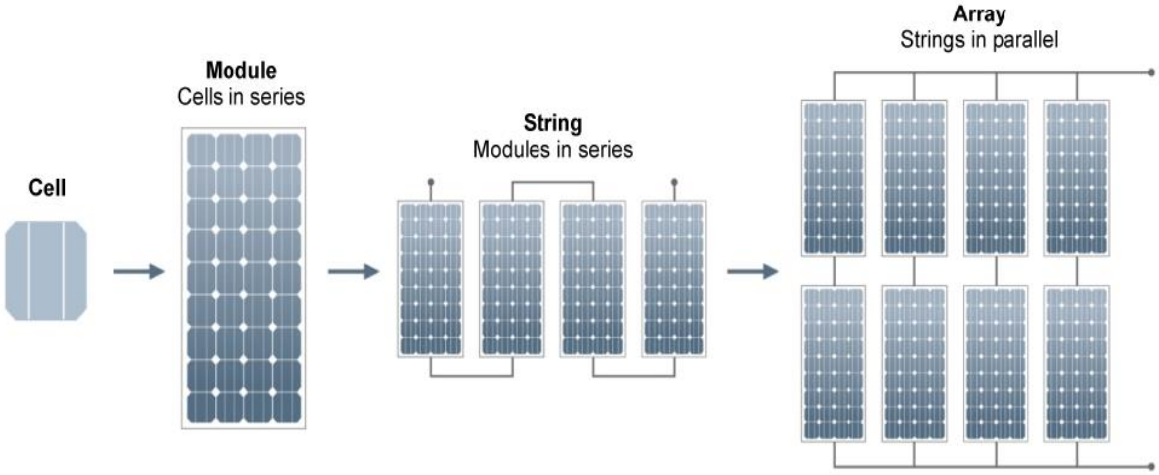


Figure 1.6 PV Configuration from Solar cell to Solar Array [8].

## 1.7 PV Module Degradation Modes

PV modules can drop a considerable amount of efficiency because of certain failures that occur inside the panel either because of the encapsulation, because of broken or damaged solar cells, because of weak connections and insulation and many more. Here we discuss a few failure modes at module level.

1. **Front Surface Soiling:**

Module performance can be reduced due to accumulation of dirt on the top surface. Because of front surface soiling the module can face losses in efficiency to about 10%.

2. **Cell Degradation**:

- Degradation at cell level can also result in decreased performance of module. The main causes of degradation at module level because of cell are:
- Increase in the series resistance ($R_s$) because of corrosion or decreased adherence of the contacts.
- Decrease in the shunt resistance because of the PN junction non-idealities.
- Anti-reflection coating deterioration.
- Interaction of boron-oxygen complexes can result in degradation of cell active p-type layer [3].

3. **Module optical Degradation:**

Discoloration of the encapsulation material can occur because of the UV exposure, temperature and humidity which can result in gradual degradation in module performance.

4. **Short-circuited cells:**

At cell inter-connections this degradation mode is common to occur, since the top and rear contacts are much close together providing a chance for short-circuiting of cells.

5. **Open-circuited cells:**

Cracked cells leads to open circuiting. Cell make crack because of thermal stresses, hailstorms or damage during manufacturing and assembly.

6. **Series Resistance and inter-connected open circuits:**

Inter-connect open circuits occurs as a result of fatigue due to thermal stresses and wind loading. Also, the series resistance can regularly increase with the age. For e.g., when the tin-lead alloy soldering bonds age, the solder becomes brittle, and cracking occurs which causes increased series resistance.

7. **Series Resistance and Module open circuits:**

Ageing effects and open circuit failures may also occur in the module structures, mostly in the bus wiring or junction box.

8. **Module short circuits:**

Module short circuits occur because of manufacturing defects. Although the modules are tested prior to sale, but short circuit may occur as a result of insulation degradation with weathering, which results in delamination, cracking and electro-chemical corrosion.

9. **Module Glass breakage:**

Module glass may break as a result of thermal stresses or hailstorms which may cause the module performance to degrade.

10. **Module Delamination:**

This mode of failure is most observed in hot and humid climates. Moisture migrates through the encapsulant, while sunlight and heat facilitate the chemical reactions that result in module delamination.

11. **Hot-spot failures:**

Hot-spot failures may occur as a result of mismatching, cracking and shading of the cells.

12. **By-pass Diode failures:**

By-pass diodes are used to overcome mismatching problems. These diodes may also face failures due to overheating or because of under-sizing.

13. **Encapsulant Failure:**

UV absorbers and encapsulation stabilizers are used to ensure long life of encapsulation sheets. Yet, depletion of encapsulation may occur as a result of leaching

and diffusion, and once the concentration falls below a critical level, rapid degradation of encapsulation occurs [3].

## 1.8 Potential Induced Degradation

In addition to all the degradation modes discussed prior, Potential Induced Degradation (PID) is fairly new, and it is one of the most critical degradation modes amongst all. The crystalline silicon PV modules have been considered to possess high reliability with about 0.8% of total degradation over a period of 25 years [9]. Where PID has been reported to cause power losses in PV modules at system level to exceed above 30%. The statement potential-induced degradation (PID) was first time proposed in the year 2010 [10]. Potential Induced Degradation is a degradation phenomenon observed in photovoltaic modules as a result of high voltage with respect to ground in the fields during operation. When numerous PV panels are connected in serious to fulfil a greater demand of energy, then the system voltage tends to increase. This voltage gives rise to leakage currents which causes loss in overall power.

The PID mechanism is different in both p-type and n-type polycrystalline solar cells. In p-type crystalline solar cell the main culprit of PID is said to be the sodium ions. When the p-type solar cells are at high negative potential w.r.t. the ground, $Na^+$ ions migrate from the glass surface to the solar cell as a result of the leakage current. While in N-type solar cells, Na+ ions are not the reason for the PID. The main cause is basically the "Surface Polarization". That is when n-type solar cells operate at high positive voltage with respect to the ground, then either negative or positive charges (depending on topology) accumulate in the SiNx anti reflecting coating of the solar cell which causes the front surface recombination to increase, increasing the recombination's of photo generated carriers which causes a decrease in overall power [11].

There are various causes of PID at system level, module level and cell level. At system level PID may result because of grounding configurations or system design, At, module level, the causes of PID may differ, it may occur due to the composition of the cover glass or due to the volume resistivity of the encapsulation material. While on cell level PID may occur because of the Anti-Reflective Coating its SiNx composition, thickness, or Refractive Index. One more possible cause could be the Emitter sheet resistance.

Environmental factors like Temperature and Humidity have also been reported as the possible causes of PID as they accelerate the leakage currents that result in power losses [12]. PID test can be performed on PV modules to determine how much actual loss may occur in the power as a result of such high negative voltages. For this, a very high negative voltage of about 1000V is applied on the PV module w.r.t. the ground. An environmental chamber is used, the test occurs for 96 hours under conditions 60℃ temperature and 85%RH humidity [13].

There are various reduction techniques that could be used to reduce PID. The PID recovery techniques are different on system, module and cell level. Some of the possible recovery techniques are Grounding the system pole, by changing the glass with any quartz material glass or acrylic sheet, by replacing the encapsulant with a greater volume resistivity encapsulant, by replacing the Anti-Reflective coating with one having higher Refractive Index or by applying "Reverse Potential". This process refers to applying reverse positive potential of about 1000V on the PV module in an environmental chamber for a time of 96 hours under conditions 60℃ temperature and 85%RH humidity [14].

## 1.9 Research Outline/Objectives:

Following are the objectives/outline of this research:

- Understanding the mechanism, causes and effects of the Potential Induced Degradation on polycrystalline PV modules.
- Designing an effective PID test for PV modules that could be use by the local manufacturers for testing and ensuring the reliability and performance of their manufactured PV panels prior to introducing them in the market.
- Performing Potential Induced Degradation tests on different polycrystalline PV modules that have been procured nationally and internationally.
- Obtaining results after PID testing procedure, Analysing the effects of PID on the PV modules before and after the PID test and calculating the overall loss in power and other electrical parameters.
- Applying PID Reduction/Recovery technique, by either changing the encapsulation material or glass cover of the PV modules, reperforming the PID

test and regaining the results to understand how the PID phenomenon has effectively reduced by applying reduction/recovery techniques.

## 1.10 Thesis Outline

The organization of the remainder thesis is as follows:

Chapter 1 discusses the introduction to a solar cell, how it works, what are its important parameters, different generations of solar cell, solar cell to PV system configurations, various degradation modes of photovoltaic modules and a brief introduction to the theme of thesis that is Potential Induced Degradation.

Chapter 2 discusses the main topic of the thesis that is Potential Induced Degradation in a detailed manner, from its history to how the actual mechanism occurs in different generation of solar cell like crystalline and thin film solar cells. Chapter 2 also explains the causes of the said phenomenon at system level, module level and cell level, how PID occurs in crystalline PV modules (both n and p-type), different procedures that can be used to perform PID test and various recovery techniques that can be used to reduce the effects of PID phenomenon.

Chapter 3 discusses the methodology on how the PID testing procedures will be designed, the pre and post conditioning procedures prior to the main PID test. Chapter 3 provides detailed explanation of the chamber method that is used to perform PID test on PV modules in an environmental chamber by varying environmental parameters like temperature and humidity and by applying high voltages. It also discusses the recovery techniques that can be applied on the PV modules to reduce the effects of the PID phenomenon.

Chapter 4 discusses the results obtained prior to the PID Chamber test and after the test to analyse the effects of Potential Induced degradation on different polycrystalline PV modules, how the power and other electrical parameters like $R_{sh}$, and $V_{OC}$ have changed before and after performing the chamber test. The comparative analyzation of the results obtained prior to and post inducing PID on various polycrystalline PV modules procured nationally and internationally was also discussed in detail. This chapter also provides detailed analysis of the results by applying recovery techniques on self-laminated

polycrystalline PV modules, performing the PID tests and then concluding the reduction in power losses because of the recovery techniques applied.

Chapter 5 discusses the conclusion drawn from the current dissertation and provides future recommendations for further development on the topic.

## Summary

Chapter 1 is the introductory part that explains what a solar cell is, how it works and what are the important parameters of a solar cell. Different generations of solar cells and how efficient each generation is also discussed. Chapter 1 also provides details of how solar cell is first configured into a module and then into a complete PV array. Different degradation and failure modes in solar modules is also discussed and how they reduce the overall performance. Finally, Potential Induced degradation is introduced briefly providing an insight on the topic of focus during the research. Objectives of the research are also defined while concluding the chapter.

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# Chapter 2

## Literature Review

### 2.1 Introduction

As the PV industry has been rapidly growing in the last few years, the reliability of PV technologies has gained considerable importance in the eyes of manufacturers, researchers, and investors. Continuous development is being made in order to reduce PV technological failures and to improve the overall efficiency of the PV technologies [1]. Due to considerable increase in energy production through renewable resources, the use of PV technologies has rapidly raised from the last decade. A single solar cell has a considerably low voltage i.e., is about 0.6V. To obtain higher voltages the solar cells are connected in series to form modules. Large no of modules are connected in series to form strings. Due increased demand more and more solar modules are connected in series. Recently the photovoltaic industry is shifting to increasing the voltages at system level to about 1500V intended for the purpose of cost reduction [2]. These very high voltage between the two ends of a string causes the phenomenon. The term “Potential-induced degradation (PID)” was first time proposed by “Solon”, a PV specialist, in the year 2010 [3]. The degradation phenomenon has been reported in crystalline PV modules and thin film technologies.

Potential Induced Degradation is a degradation phenomenon observed in photovoltaic modules as a result of high voltage with respect to ground in the fields during operation [4]. This high potential difference gives rise to leakage currents that reduce the overall performance of the PV modules. PID has been reported in both crystalline silicon photovoltaic modules and in thin film technologies. Usually because of the increased use of transformer-less inverters grounding of the system poles is not required, as a result of which one end of the string is at very high positive potential while the other end of the string is at very high negative potential. It has been stated in my research studies that p-type cell can be affected by PID phenomenon due to high negative potential while n-type crystalline solar cell can be affected by PID because of both positive as well as negative potential. In our studies we will be focusing on effect of PID on p-type c-Si cells mainly.

It has also been reported that PID can cause power losses above 30% in PV modules at system level causing it to a be severe form of degradation [5]. So, mitigating PID effect is becoming one important concern.

## 2.2 Leakage current pathways in PV Modules:

In PV systems, a very high difference in potential exists between the solar cell and the solar module frame at both ends of the module string. This results in inducing leakage currents that flows through the module packaging resulting in power loss. In standard crystalline silicon solar modules, the current flow from the metallic frame of the module to the solar cell through different pathways as shown in figure 2.1.

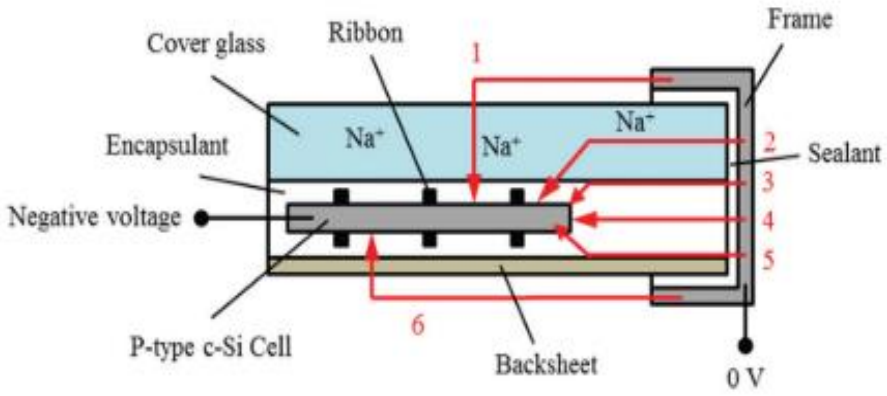


Figure 2.1 Leakage current pathways in a cross-sectional view of p-type c-Si solar module [2].

1) Alongside the glass sheet/superstrate surface, all the way from the bulk of the superstrate and encapsulation sheet into solar cell.
2) All from the bulk of the superstrate (lateral position) and through the bulk of the encapsulation sheet into the solar cell.
3) Alongside the interface between the superstrate and encapsulation and through the bulk of the encapsulation into the solar cell.
4) From the bulk of the encapsulation.
5) Alongside the boundary between the back-sheet and from the bulk of the encapsulation and backsheet.

6) Alongside the surface of the backsheet, through the bulk of the encapsulation and backsheet.

## 2.3 PID Mechanism in different PV technologies

The mechanism of PID differs with different PV technologies like crystalline silicon PV technology and thin film technologies. Also, in both n-type and p-type crystalline PV modules the mechanism appears to be completely different as reported by many researchers [2]. Firstly, we discuss the mechanism of PID in crystalline PV technologies and then in thin film technologies.

### 2.3.1 Crystalline-Silicon (c-Si) based technologies

c-Si based technologies include p-type c-Si and n-type c-Si technology. Both technologies will be discussed based on PID mechanism.

### 2.3.2 PID Mechanism in p-type c-Si technology

The phenomenon that occurs in p-type crystalline silicon solar cells is named as PID shunting. And the main cause of PID in p-type c-Si solar cell is Sodium ($Na^+$) ions present in the cover glass. In p-type cells, when one end of the string is at very high negative potential w.r.t. the ground. It also causes the p-type c-Si solar cells to be at very high negative potential w.r.t. the frame. The p-type solar cells are at very high negative potential that means that the solar cells have more electrons, which creates leakage current. Now this current can drift from frame of the module to the solar cells through various paths as shown in the figure 2.1. This leakage current when moves along the frame into the cover glass, it also causes the positively charged sodium ions to drift along it from the sodium rich cover glass through the anti-reflective coating and cross the p-n junction of the solar cell by penetrating through the crystal defects. This leads to the decrease in the shunt resistance $R_{sh}$ in the diode model of a solar cell and increase in the reverse saturation current as a result of the increased recombination in the space-charge region. A significant loss in fill factor is observed which causes reduction in the maximum power reducing the overall efficiency of the solar cell [5].

The source of the sodium ions is relatively strong. In most studies it has been reported that sodium ions originate from the soda lime rich glass [2]. Many theories have been proposed

to explain the main cause of the PID phenomenon in p-type c-Si solar cells. One of the most discussed model states that, the accretion of the positively charged sodium ions in the anti-reflective coating reverses the “n+ emitter junction” into “p+ conducting region”. Eventually creating a pathway for shunting across the p-n junction of the solar cell. This model is mostly referred to as inversion model and has been discussed in many publications [6]. However, the inversion model was soon nullified by another model that was identified by researchers through various experimentation.

The researchers examined the shunting caused due to PID phenomenon through “Scanning Transmission Electron Microscopy” and detected that the “stacking faults” in the p-n junction of c-Si solar cell were affected by sodium ions migration. As PID occurs, the sodium ions under the effect of strong potential drift towards the “$SiN_x$/Si interface” and gather in the “$SiO_x$ interlayer”. As a result, sodium ions can contaminate the “stacking faults” as shown in fig 2.2 and fig 2.3. Once the sodium ions enter the stacking faults, they are counteracted by the freely moving electrons in n+ emitter junction. The sodium ions move in the stacking faults as a result of diffusion procedure rather than drifting. So, the aforementioned model suggests that PID is caused as a result of Na+ ion contamination in the stacking faults [2].

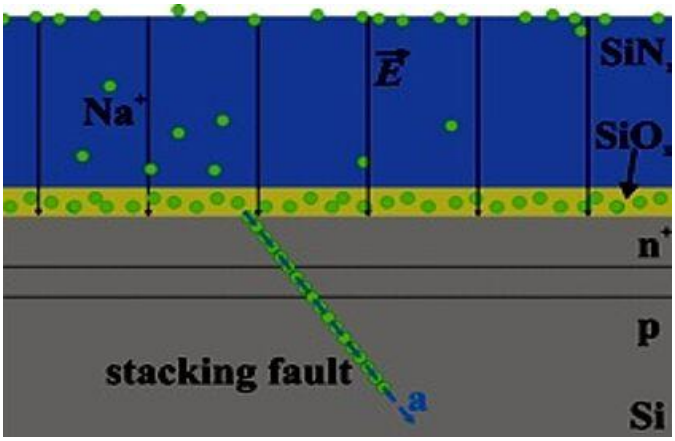


Figure 2.2 Schematic diagram of the cross-sectional area of a solar cell showing movement of Sodium ions (green dots) via the anti-reflective coating and diffusing in to the stacking faults [2].

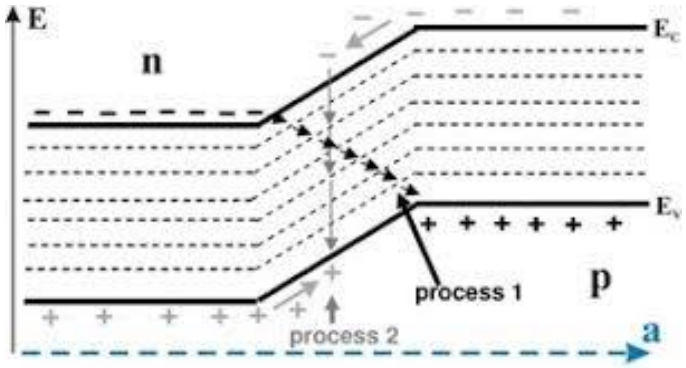


Figure 2.3 The recommended band construction along a sodium ion decorated stacking fault [2].

### 2.3.3 PID Mechanism in n-type c-Si technology

The mechanism that is observed in n-type c-Si cells is referred to as "Surface Polarization" where there are either positively or negatively charged carriers (dependent on the topology) gathered within the SiNx stack that act as a passivating and anti-reflecting coating [5]. This process was first time observed in the brand name "SunPower" crystalline silicon photovoltaic modules manufactured with highly effective n-type back contact crystalline silicon with silicon dioxide surface passivation. In accordance with the studies suggested by Swanson, when n-type back contact c-Si solar cells are subjected to high positive potential then leakage current is created which flows from the cell through the encapsulation and glass sheet to the grounded frame. This causes the accumulation of negatively charged carriers on the surface of anti-reflective coating. These negative charges are imprisoned inside the $SiN_x$ antireflective coating due to high resistivity of $SiO_2$-$SiN_x$, $SiO_2$ or $SiN_x$ coat. So, as an alternative of being gathered by the solar cell's junction, the positive charged photon created holes/carriers located in the anterior area of the solar cell are more engrossed towards the face of the solar cell by the negatively charged carriers present in the antireflective coating. As a result, they recombine with electrons which causes an increase in surface recombination. Due to increased recombinations, the voltage and current drops. In addition, with reduced voltage and current, causing disparity between the cells within a module result in substantial loss in fill factor, which leads to significant loss in efficiency [2].

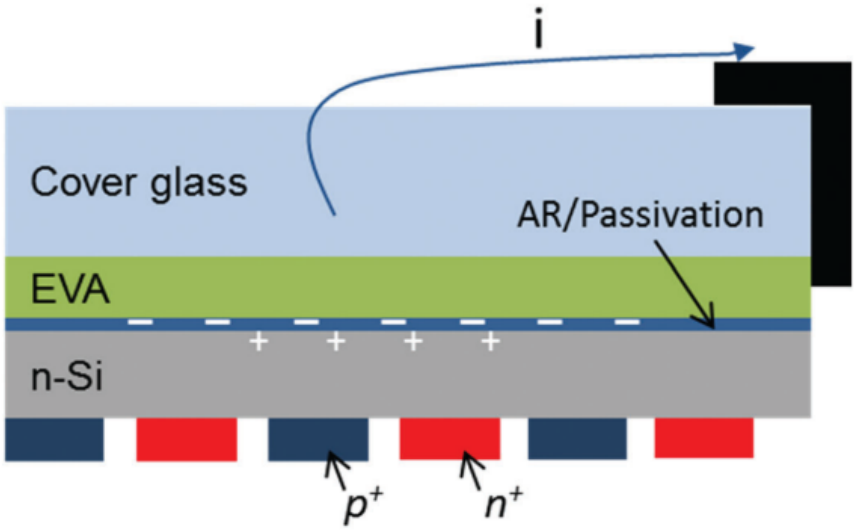


Figure 2.4 Schematic diagram illustrating the effect of SunPower's Surface Polarization on highly efficient n-type back contact c-Si cells [2].

Similarly, a similar behaviour was observed in highly efficient "n-type PERT cells" with the boron-doping on the top most junctions while being subjected to negative bias relative to the ground. The causes of degradation in such cells were suspected to be the increase in surface recombinations because of the accretion of positive charged carriers in the passivation of nitride with/without oxide [7]. Most of the observations in different n-type c-Si solar cells can be explained by the Surface Polarization theory, but it may not be able to explain the degradation effects in n type cells. For example, the n-type single c-Si PV modules with a back-end emitter damaged diffidently when exposed to the negative bias. The modules experienced losses in efficiency, FF and $V_{OC}$ due to increased surface recombinations of minority carriers. These results are completely opposite to that of the Surface Polarization theory, where positively charged ions must be accumulating on the surface of the antireflective film and negatively charged carriers are instead repelled away from the top regions of the cell. A potential reason for degradation could be the sodium ion accumulation in the silicon surface under negative biasing. But this assumption is yet to be verified [2].

## 2.4 PID Mechanism in Thin Film technology

Thin film technologies like amorphous silicon (a-Si), cadmium telluride (CdTe) and copper indium gallium selenide (CIGS) all have been cited in literature to be affected by

PID mechanism when the cells are biased negatively. PID mechanism in thin film technologies is caused due to sodium ion Na+ ion migration. Generally, there are two circumstances that may occur in thin film solar cells depending on the presence of moisture. In the low moisture conditions, that is mostly in dry environments Na ions are reduced to elemental sodium. The accretion of sodium ions effects the electrical parameters of the modules significantly, but the mechanism is observed to be reversible under reverse bias. Generally, excessive impurities in the p-n junction cause recombinations. It has been reported that, the open-circuit-voltage ($V_{oc}$) and the fill-factor (FF) reduces to about 40% and 50% respectively after PID testing in "CIGS" modules with zinc oxide "TCO" layer. Whereas the short-circuit current ($I_{sc}$), shunt-resistance ($R_{sh}$) and series-resistance (Rs) changes slightly. Therefore, it can be concluded that the PID mechanism in the aforementioned modules mainly occur due to increased recombinations. A scenario was also reported in literature that involved shunting, also an increase in the series resistance (Rs) was reported in "CdTe" modules but the root cause of the degradation phenomenon in second generation photovoltaic technologies is yet to be found [2].

## 2.5 Causes of PID

For better understanding of the Potential Induced Degradation phenomenon, we study the causes of PID at three different levels that are as follows:

- At System
- At Module
- At Cell

The causes of PID vary at cell, module, and system level, so it is necessary to study the process at each level individually [8].

### 2.5.1 At System

The difference in potential between the solar cell and the metallic frame is one significant cause for the occurrence of PID at system level. As the no of modules are increased in a string, the voltage is also increased with respect to the ground. Lately, the system voltages have been increased from 600V to 1000V, and to as high as 1500V [9]. The system level

voltage depends upon the number of modules that are serially connected in the string, temperature and on the irradiance. The high potential is associated to the location of the modules connected serially in the string and on the kind of grounding techniques. There are three different types of grounding arrangements:

1. Positive ground configurations.
2. Negative ground configurations.
3. No ground configurations.

When the negative pole of the system is grounded then it is referred to as negative potential, and if positive pole of the system is grounded then it is referred to as positive potential. In case of both positive and negative potential the polarity remains the same throughout the string. But if no pole of the system is grounded then the resulting potential is not fixed, one end of the string is at high positive potential while the other end of the string is at high negative potential w.r.t. the ground. And this phenomenon is referred to as **"Floating Potential"** [10]. Floating potential is observed in the case when transformer-less inverters are used. Transformer-less inverters don't require grounding due to which it gives rise to floating potential. PID is only identified in PV system with a high negative potential of the solar cells w.r.t. the metallic frame as shown in figure 2.5. Also, there was no PID detection in the case when the negative pole of the system was grounded in case of the traditional transformer inverter as shown in figure 2.6(a). However, PID is a serious issue on system level since transformer-less inverters are being commonly used in PV systems because of their higher efficiency and lower cost as compared to inverters with integrated transformers as shown in figure 2.6 (b) [8].

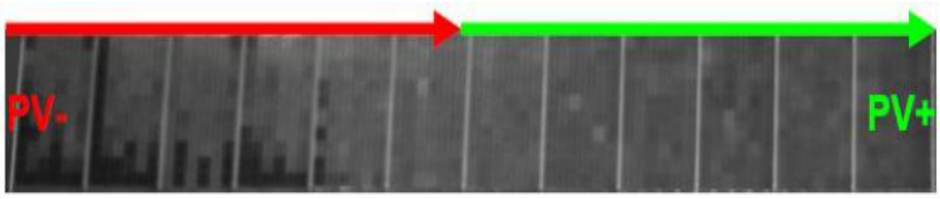


Figure 2.5 Electroluminescence imaging of PV module string with Floating Potential showing that PID is higher at the negative potential [9].

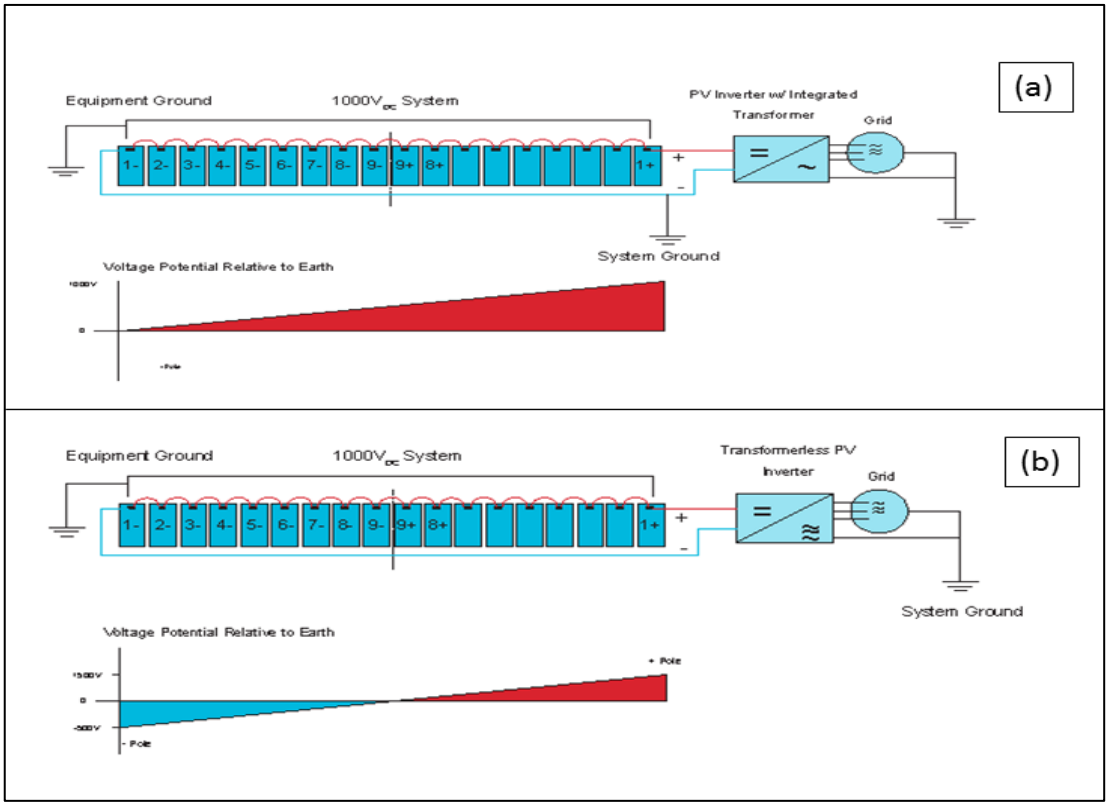


Figure 2.6 (a) PV system with transformer integrated inverter, (b) PV system with transformer-less inverter [11].

### 2.5.2 At Module

It is understood by now that the high potential between the solar cell and frame results in leakage current which comprises of ions. The current depends mainly upon temperature and humidity. The leakage current rises as the temperature and humidity is raised [12]. There are various paths for the flow of leakage current while interacting through the glass, encapsulant sheet, back-sheet and the metallic frame in a module. It has been observed that at high humidity conditions, the leakage current flows from the cover glass through the bulk into the solar cell.

And in case of lower humidity conditions the leakage current flows through the glass-encapsulation interface between the frame and the cell [13]. Since in outdoor conditions high humidity exists so higher is the leakage current observed. So, the path of leakage current most linked with the degradation phenomenon is the path from the metallic frame

to the superstrate through the encapsulation into the solar cell. Other paths are likely to cause PID, but the most relevant one is shown in figure 2.7.

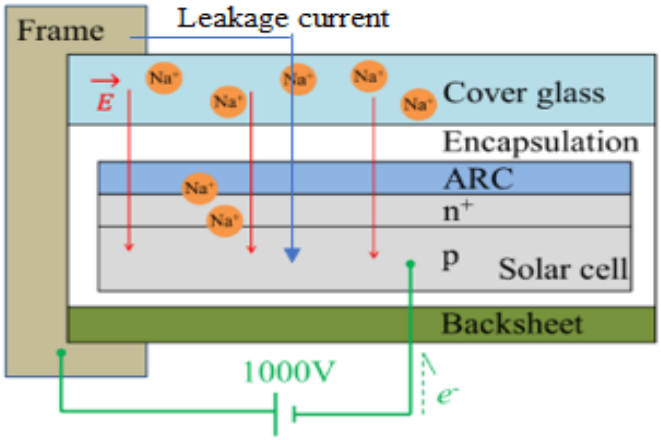


Figure 2.7 Schematic Diagram showing leakage current path in PV module [14].

At module level, different components could be responsible for causing PID i.e., module encapsulation and the cover glass [15]. The Volume Resistivity of the encapsulation material is an important factor causing the PID. It can be defined as the resistance to the path of the leakage current through the body of the encapsulation, glass, and the metallic frame. Higher volume resistivity causes lower leakage currents which results in less conductive encapsulation material. Less conductive encapsulation material causes the PID phenomenon to reduce effectively. Nowadays most commonly used encapsulation material is EVA (Ethylene Vinyl Acetate). EVA is found to be PID susceptible because of its low volume resistivity. Therefore, different PID resistant encapsulations are being used in alternative of EVA having higher volume resistivity like ionomer, silicone, and thermoplastic polyolefin resistivities as shown in figure 2.8. However, EVA is still being used commercially in modules because of its several advantages in spite being PID susceptible for e.g., long-term stability, cost effectiveness and availability.

Table 2.1 Table showing volume resistivity of different encapsulations [16].

| **Polymer** | **Equipment/Method** | **$T_{Processing}$ (°C)** | **$t_{processing}$ (min)** |
|---|---|---|---|
| EVA | Vacuum Laminator | 140-160 | 8-20 |
| Silicone | Casting process, dispenser | 80 | 30 |
| PVB | Vacuum Laminator, Roll lamination and Autoclave | 140-160 | 8-20 |
| Ionomer | Vacuum Laminator | 140-160 | 10 |
| TPSE | Vacuum Laminator, Roll lamination and Autoclave | 160-170 | 7-10 |
| TPO | Vacuum Laminator | 140-160 | 10-14 |

The material of cover sheet can also be one potential cause of PID. Most commonly used material as cover sheet is soda lime glass. The glass cover used is sodium rich which causes sodium ion migration which is root cause of PID in crystalline PV modules. Therefore, alternatives to cover glass are being reported for e.g., Quartz glass that potentially reduce sodium ion migration resulting in lowering PID phenomenon in PV modules. Also, it has been reported in several journals that acrylic film can be used as a substitute to cover glass and it showed it remarkable resistance against PID [1].

Table 2.2 Electrical parameters of single celled acrylic film and glass cover modules after PID test (85℃, 1000V, applied for 24 hours) [1]

| **Module Parameters** | **$V_{OC}$** | | **$I_{SC}$** | | **$P_{max}$** | | **FF** | |
|---|---|---|---|---|---|---|---|---|
| | **Ave.** | **max** / **min** | **Ave.** | **max** / **min** | **Ave.** | **max** / **min** | **Ave.** | **max** / **min** |
| Glass cover sheet | 9.4 | 14.0 / 4.6 | 61.0 | 71.5 / 49.7 | 2.1 | 3.4 / 0.8 | 34.4 | 35.2 / 33.8 |
| Acrylic-film cover sheet | 100.1 | 100.1 / 100.0 | 99.5 | 99.6 / 99.5 | 99.7 | 99.9 / 99.5 | 100.1 | 100.2 / 100.0 |

### 2.5.3 At Cell

On cell level, the effect of the degradation phenomenon on p type polycrystalline PV modules is mainly reliant on the solar cell properties such as the base resistivity, anti-reflective coating, and emitter sheet resistance. In the following we state the factors that are known to have a major impact on cell level.

#### 2.5.3.1 Base Resistivity

It has been experimentally proved that increasing the base resistivity of p-type crystalline solar cells leads to more resistant solar cells as demonstrated in the figure 2.10. As smaller “base doping” with “greater base resistivity” causes broader depletion region at the p-n junction when the emitter-doping is held constant. Also, lower quality silicon and or comparatively higher crystal defects increase the PID effect. But in-depth study needs to be carried out to further prove these cell dependencies [3].

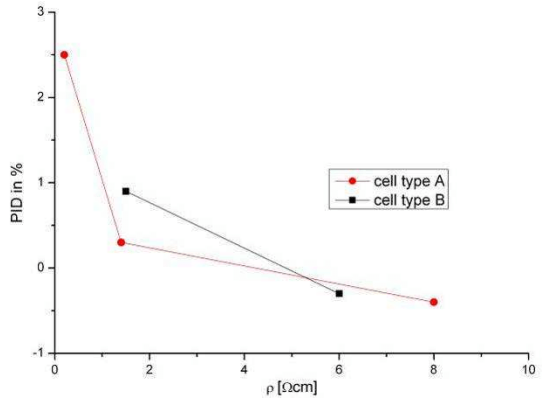


Figure 2.8 Graph showing PID dependency on base resistivity [3].

2.5.3.2 Emitter Diffusion

Cell processing basically starts with cleaning then texturing. In the texturing phase, based on the type of wafer and process alkaline or acidic, textures are applied onto the cell. Studies reveal that if texturization is not complete, or in case any excesses are left on the surface, may affect the subsequent steps of cell processing eventually causing PID. Next step to texturing in cell processing is the emitter diffusion, which was expected to be affected and was confirmed after the PID testing [3]. Increasing the emitter sheet resistance causes higher chances of PID which means that cell process optimization by increasing the emitter resistance could lead to higher tendency of the PID effect as shown in figure 2.11.

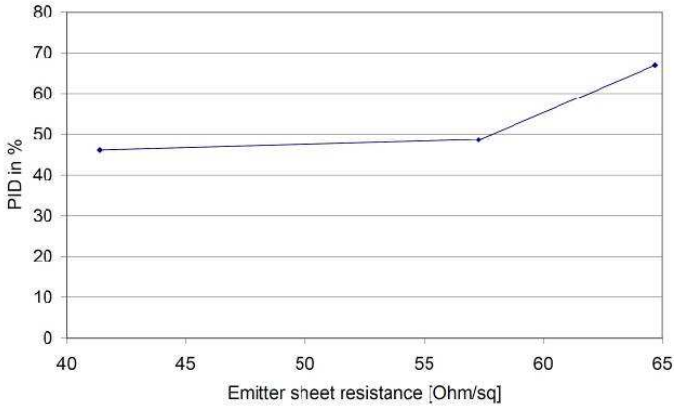


Figure 2.9 Graph showing PID dependence on Emitter sheet Resistance [3].

#### 2.5.3.3 Edge Isolation and Emitter back Etching

Many cell manufacturers, for the purpose of removing the dead layer of the emitter use techniques like emitter back etching. Depending on the cell processing parameters, the sheet resistance may increase resulting in PID. A study reveals that by process of emitter back etching not only the emitter was isolated from the edges, but also the emitter was removed from the surface resulting in higher emitter resistance. This shows that cell processing methods that are considered to have no affects later on, can lead to serious degradation when subjected to high potential in field [3].

#### 2.5.3.4 Anti-Reflective coating

The step in cell processing and production that is the most important concerning PID is Anti-Reflective Coating (ARC) deposition. SunPower detected that $SiN_x$ antireflective coating has a considerable impact on the polarization effect of the n-type crystalline solar cells. Also, this layer is extensively employed in the p-type crystalline cells, so the properties of the layer are a very significant parameter relating to the PID phenomenon. In standard crystalline solar cells, this layer consists of N and Si, the deposition technique, the ratio of these elements and layer thickness define the characteristic of this layer. Figure 2.11 shows a graph representing the dependence of PID on the Si-N ratio, corresponding to the refractive index and optical characteristics [3].

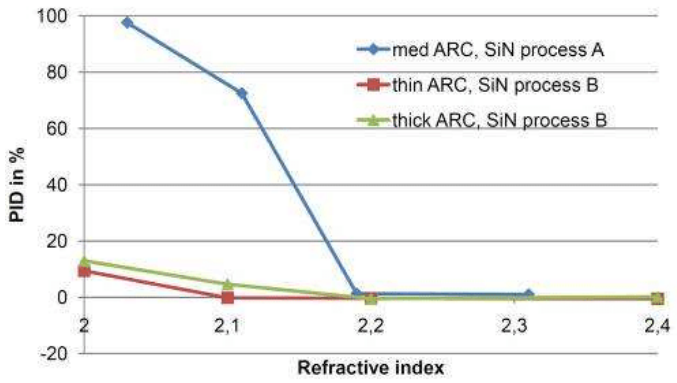


Figure 2.10 Dependence of PID on RI, thickness, and deposition method [3].

Three results can be estimated from the figure. First, the N-rich layers show higher degradation than Si-rich layers. Other than the refractive index, the layer thickness is an important parameter as these two parameters must be adjusted accordingly to reduce the

reflectivity of the cell. The second result that can be deducted from the figure is that reducing the layer thickness can result in lower PID susceptibility. The third parameter that has an impact on PID susceptibility is the homogeneity of the Si-N layer. However, a homogeneous process, standard thickness and RI can help in reducing the risk of PID [3]. The effect of PID can be reduced by increasing the RI, though it is not advised to raise it above the value 2.1 because of the increase in the light absorption pattern in the antireflective coating [17]. Also, experiments have been performed involving multiple layers of $SiN_x$ ARC to reduce the effect of PID but results from various experiments showed that these multiple layers had a smaller effect on preventing PID [18]. Some studies also reveal that SiNx deposition equipment also impacts PID, so selecting the appropriate equipment for deposition of ARC is very important to produce PID free cells [17].

## 2.6 PID Test Methods

Potential induced degradation is becoming an important reliability issue in PV systems because of considerable loss in the $P_{max}$. The major concerns regarding PID at commercial level is that it cannot be inspected by performance and qualification tests, the "International Electrotechnical Commission" (IEC) 61215 edition number 2, set of standards. Thus, the commission introduced standards for system durability and qualification under the draft IEC-62804. In this draft several PID test methods have been introduced for crystalline and thin film technologies at cell and module level.

### 2.6.1 Environmental Chamber Method

In this method an environmental/climate chamber is used to create the PID conditions that are experienced in field. According to the IEC 62804-1 draft, the stress level for performing PID test in the environmental chamber is 60℃ ±2℃ temperature, 85% ±5% relative humidity (RH) and dwelling time of 96 hours [2]. Along with stress parameters, negative potential (-600Vdc or -1000Vdc) is applied to the shortened leads of the c-Si PV modules. A typical PID setup is indicated in picture 2.12(a). Both terminals of the module are short and connected to the negative terminal of the high voltage power supply. The frame of the module is earthed and connected to the positive probe of the DC power supply [2]. The leakage current is measured using an additional apparatus as shown in the figure

2.12(b). The current can be measured by using a voltage meter across a resistive circuit, such as a “RI resistor”. Resistor typically of very high voltage for e.g., 10kΩ is connected in series in between the dc power supply and the PV module metallic frame. Leakage current can be computed by measuring the voltage across the resistor using a voltmeter, and then the current is calculated by dividing the obtained voltage with the resistance [19].

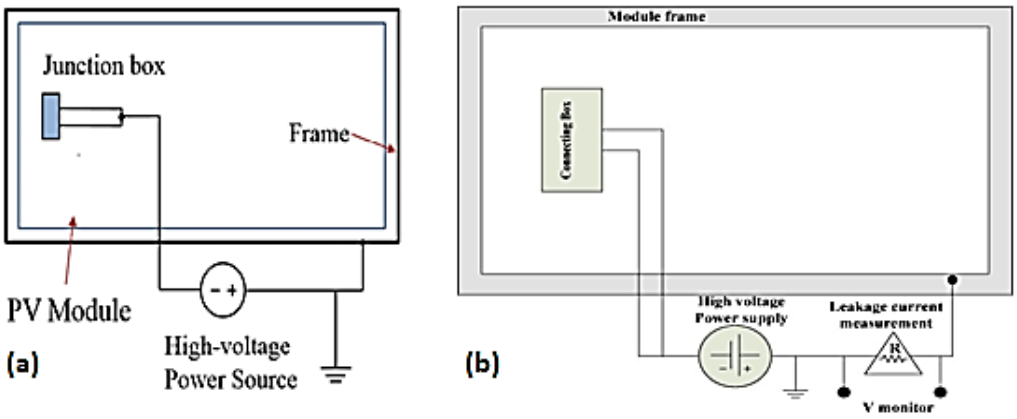


Figure 2.11 Schematic diagram of PID test setup using chamber method (left) and (b) Leakage current measurement setup (right) [2][19].

### 2.6.2 Stress Method

Stress method is the second method for determining the effect of PID on crystalline PV modules as mentioned in the IEC 62804-1 draft. Also called the Metal foil method as it does not require an environmental chamber. This method is less expensive comparative to the environmental chamber method but is a slower process to identify the PID effect. Stress method applies even grounding potential over the surface of the module. The module surface is covered with an electrically conductive medium for e.g., copper, or aluminium foil to provide which uniform surface contact. The IEC 62804-1 standards draft sets certain specific minimum stress levels for PID detection that is the experiment should be performed in a 25℃ ambient room temperature and the relative humidity should be less than 60%. The dwell time for stress method test is 168 hours. The voltage should be applied on the shortened module leads at the start of the stress test, should be continuously applied over the course of the test and switched off at the end of the test [20].

This test is more favourable for heavily soiled modules [21].

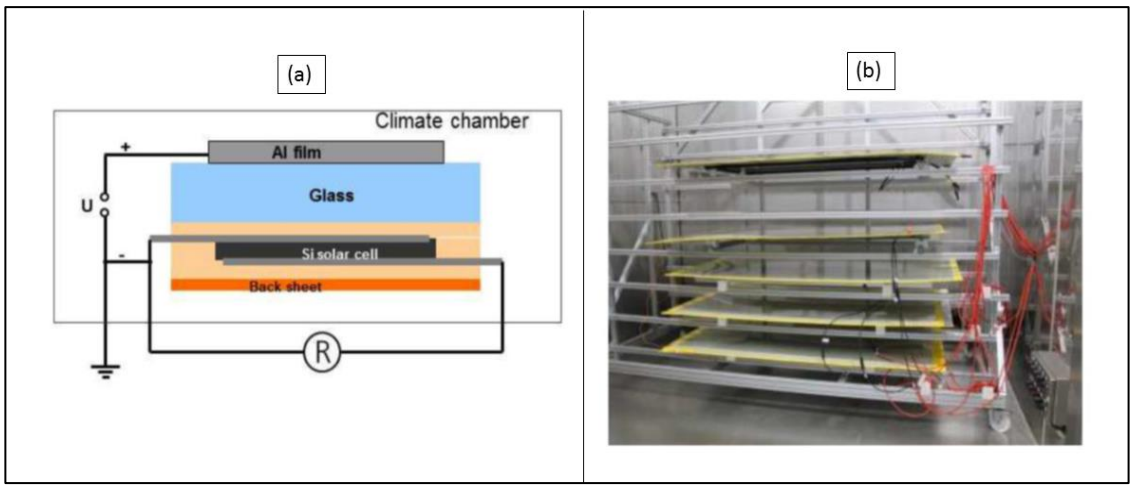


Figure 2.12 Schematic representation of Stress method and (b) a picture showing the Lab setup [22].

### 2.6.3 Corona Discharge Method

PID testing is very important at cell-level, as it provides opportunities for the researchers to investigate the main cause of PID. In the presence of the encapsulations, it is very hard to isolate the damaged solar cells for microscopic research. Also, the cell level PID testing technique is cost effective, as bare cells can be directly tested and do not require module laminations. A simple schematic diagram is shown in Figure 2.13. Positive charged carriers are deposited at the top of a fine wire because of high positive potential (~11kV), which are then gathered on the front area of the test sample [22][2]. Electric field is said to be generated on the surface of the solar cell sample by these positive charges. This test method is considered convenient and quick for carrying out PID testing, but the nature of the positive ions deposited on the test sample are considered to be different and not the actual representation of the Na+ ions on the modules in field. It has been proposed that the positive ions deposited on the sample solar cell may damage the “SiNx film” with passage of time, resulting it to be a less feasible method for PID testing [2].

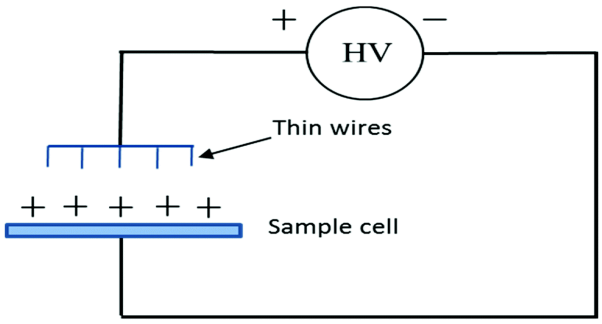


Figure 2.13 A simple schematic drawing of the “Corona Discharge Method” for PID test [2].

## 2.7 Solutions of PID

As the phenomenon of PID is relatively newer, a lot of work is being done to reduce or completely recover the PV modules. The PID mechanism can be avoided at cell, module, and system level.

### 2.7.1 On Cell

One of the most common methods to reduce the PID at cell level is to modify the $SiN_x$ anti-reflective coating. [5]. PID susceptibility has been reported to be affected by the refractive index (RI) of SiNx ARC. It was observed that by increasing the refractive index of the ARC layer, PID can be re reduced reasonably [23]. The deposition method of the ARC is also reported to reduce the PID susceptibility for e.g. ARC films prepared by “Multi-hollow cathode plasma-enhanced chemical vapor deposition (PECVD)” [24]. It was observed that by increasing the refractive index of the ARC layer, the efficiency of solar cell drops. So, another method was investigated by inserting additional layers of ARC with different refractive indexes which slightly raised the stability against PID as shown in figure 2.14. Another technique is to add a fine oxide (Silicon dioxide) layer between the $SiN_x$ and the emitter layer of the solar cell [18]. This oxide layer can play an important role in charge accumulation, thus helping the $SiN_x$ film in retaining their positive charges. These $SiO_2$ layers have been reported to be replaced by $Al_2O_3$ layers for better resistance to PID [25]. Recently it also has been observed that a thin layer of phosphosilicate glass (PSG) between the emitter and $SiN_x$ was able to provide resistance against PID [26].

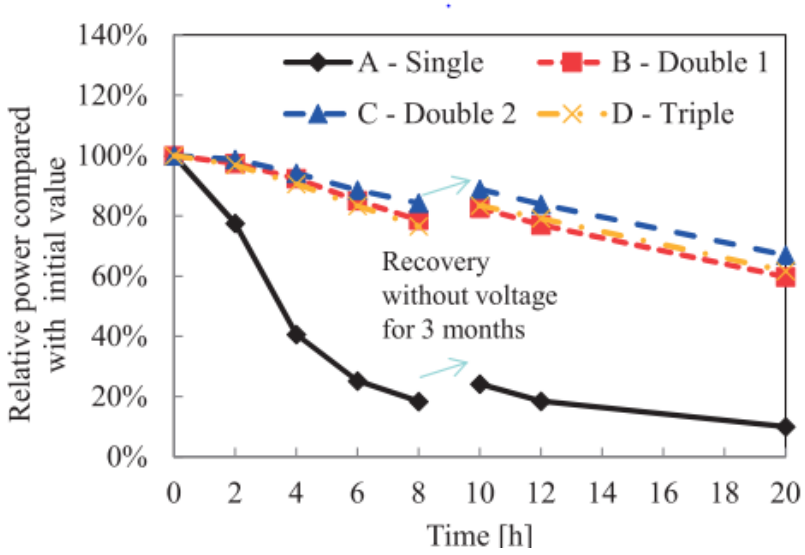


Figure 2.14 Graphical representation of the effects of PID test w.r.t. time on cells having single, double and triple layers of ARC [25].

### 2.7.2 On Module

At module level, the PID can be reduced by either changing the cover glass or the encapsulation sheet. The cover glass used mostly in PV modules is made of soda lime, having higher concentrations of the sodium ions that is suspected to be the main cause of PID. Alternative glass like Quartz glass can bused instead as it has lesser concentration of sodium [13]. Another method has also been reported to reduce the PID susceptibility that is by replacing the glass with acrylic film namely Polymethyl methacrylate (PMMA) was used. It was observed that only a small amount of s sodium delated ions occurred between the cell and cover sheet in the acrylic-film module as confirmed through ToF-SIMS analysis. Thus, it was confirmed that acrylic-film PV modules had remarkable resistance against PID [1].

Encapsulation sheet replacement may also play an important role in reducing the effect of PID at module level. The volume resistivity of the encapsulation play an important role in resisting the leakage current to flow from the glass cover to the solar cell through the encapsulation. Higher the volume resistivity smaller the amount of leakage current flow and so less PID. Therefore, PID can be suppressed using encapsulation materials having higher volume resistivity for e.g., polyolefin and ionomer instead of standard encapsulant

that is EVA ($1 \times 10^{14}$ Ω-cm) [27][12]. Another technique is to add an additional layer between the module glass and the cell. It has been demonstrated that using thin polyethylene film (having volume resistivity material of $1.81 \times 10^{17}$) between the glass and the encapsulation (EVA) can reduce the effect of PID [28]. Coating of a TiO2 film on the module glass surface also showed great resistance to PID [29].

Table 2.3 Optical and Electrical properties of different encapsulations [12].

| **Encapsulation type** | **Volume Resistivity (Ω-cm)** | **Transmittance (%)** |
|---|---|---|
| EVA | 1.0x $10^{14}$ | 91.0 |
| PVB | 4.8x $10^{12}$ | 91.0 |
| TPU | 2.7x $10^{14}$ | 90.0 |
| Silicone | 6.0x $10^{15}$ | 98.9 |
| Polyolefin | 2.0x $10^{16}$ | 92.0 |
| Ionomer | 7.1x $10^{16}$ | 93.4 |

### 2.7.3 On System

In PV systems, the inverter is a crucial component of the balance of systems, it converts the direct current output in to alternating current. Depending on different topologies, inverters are characterized into two main types: “Transformer-based inverters” and “Transformer-less inverters”. In case of the prior one, either the positive or the negative pole of the system is earthed, that leads to either positive or negative charged cells with respect to the ground. As stated earlier the negatively biased p-type polycrystalline silicon solar cells are susceptible to PID phenomenon and so a possible solution is to ground the negative pole of the PV system in case of the transformer-based inverter [8][2][30]. This shall affirm that all the modules are positively biased, eradicating the effect of PID in the crystalline modules.

There also exists a strong concept of transformer-less inverters in the PV industry because of various factors for e.g., transformer-less inverters are lighter in weight. more compact and most importantly the “Conversion efficiency” of the PV systems increases by 1-2 %.

Transformer-less inverters require no grounding, which results in a floating potential resulting in some of the solar cells to be biased negatively and others to be biased positively w.r.t. the ground [2]. One solution that can be applied in case of transformer-less inverter is the “Recovery Potential”, that means applying reverse bias voltage (above +600V) to the modules during the night [4]. Another paper reports the recovery of the PID effected modules could be ensured by applying reverse voltage of +850V on the modules for 300 hours, at room temperature [9]. Another paper suggested the recovery of PID panels by temperature referred to as “Thermal Recovery”, in which recovery close to 100% was achieved by storing panels at 100℃ for 10 hours [8] as shown in figure 2.15.

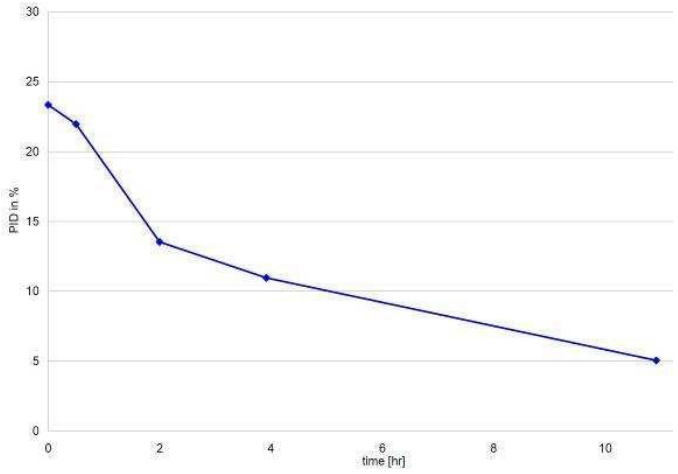


Figure 2.15 Recovery of PID affected modules by applying temperature (~ 100℃) [8].

A photovoltaic inverter manufacturing company “SMA” has been providing a solution of PID at system level called as the “PV Offset Box”. It is a device that works with the inverter and enables recovery of the PID affected PV modules during night time via reversing the potential. Therefore, the PV modules that have been affected by PID during the day can be regained during the night [31].

Micro-inverters can also help reduce PID at system level. Mostly the “Micro inverters” have ratings matching a single solar module, hence DC voltage of the system is less than 50 $V_{dc}$ using micro-inverters. This voltage can be referred to as “Extra Low Voltage”, while the standard system voltages employing a conventional inverter is up to 1000V. And such small voltage at system level results in effective mitigation of PID phenomenon [31].

## Summary

Chapter 2 discusses about the phenomenon of "Potential Induced Degradation", what it actually is, how and when it initiated, and its causes, testing procedures, its effects on crystalline PV modules and how it can be eliminated. The mechanism of PID differs in different PV technologies like crystalline silicon solar cells (Mono-crystalline and polycrystalline solar cells) and thin film solar cells (CIGS and CdTe), which has been discussed thoroughly for better understanding of the phenomenon. The causes of PID have been explained individually at cell level, module level and system level giving a better insight of how it occurs at different levels. Major emphasis has been made on the PID phenomenon on p-type c-Si as it is the key focus of the study in this research. Various test methods for measuring the PID phenomenon on crystalline-Si solar modules have been discussed as drafted by the IEC standards specifically designed for PID testing. PID tests have also been independently explained on module level and cell level making it easier for choosing a specific testing procedure according to the requirements. The effects of PID have been also discussed in this chapter explaining how the said phenomenon affects the PV technologies at cell, module, and system level. Lastly, variety of solutions have been addressed to completely eliminate or to reduce this critical phenomenon on various levels. For this purpose, numerous research articles have been referred to providing solutions to PID that have been discussed up to date. In this way, chapter 2 sums up by providing comprehensive understanding of the PID Phenomenon its mechanism, causes, affects and solutions at various levels.

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# Chapter 3

# Methodology

## 3.1 Introduction

Potential Induced Degradation testing requires a series of tests to be performed to investigate the effects of PID on the poly c-Si PV modules. In order to determine the changes in electrical parameters and overall performance of the PV modules a sequence of tests is performed prior and post the main PID test. The testing procedures can be divided into three phases:

- Pre-testing.
- The Main PID test.
- Post-testing.

The pre and post testing procedures are performed under testing standard IEC 61215:2015 and the main PID test is performed under the standards IEC 62804-1 for crystalline silicon solar modules.

The pre-testing phase starts with stabilization of modules by natural sunlight exposure and is followed by detailed visual inspection of the modules to detect visible defects that can be distinguished through naked eye. After visual inspection maximum power determination is performed using IV curve tracer setup, following this dry and wet leakage current tests are performed. The last procedure in pre-testing is the Electroluminescence imaging that is performed by using an EL camera in a dark room. Subsequently PID test is performed inside an environmental chamber under application of voltage stress and varied environmental conditions.

After the PID test is performed post PID tests are performed to investigate the effects of PID phenomenon on the poly-crystalline PV modules. for this all the pre-testing procedures including Pmax determination, EL imaging, dry insulation and wet leakage current tests are repeated in similar manner as before PID main test.

The pre and post results are recorded, and results are analysed to determine how different modules are being affected by the potential induced degradation phenomenon. The flow chart for the complete testing procedures is shown in figure 3.1 that shows different tests that are performed before and after PID test in a sequential manner.

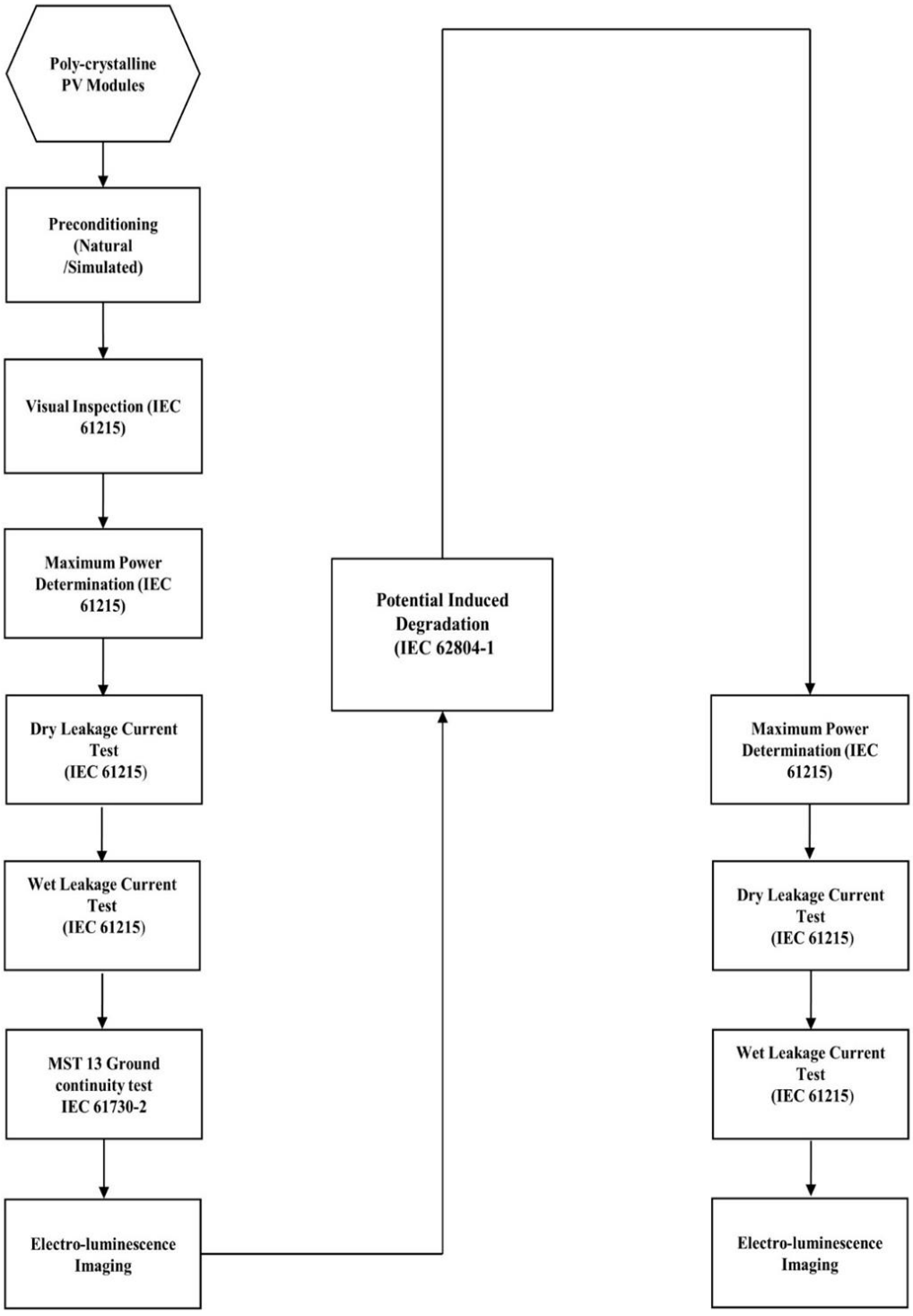


Figure 3.1 PID Test Flow Chart.

## 3.2 Module specifications

The modules undergoing tests are a total of five different modules. One module is imported from China while the remaining four modules are self-laminated and procured locally. The China imported module is claimed to be PID resistant because of use of PID free poly-crystalline solar cells. Remaining four modules are customized in a way that they differ on basis of glass type and encapsulation type. But all the modules are similar in cell technology i.e., poly-crystalline PV solar cells. All modules consist of four multi c-Si solar cell in a (2×2) order i.e., two cells in each column and row. All the self-customized modules were laminated in the same industry via the vacuum lamination method. The modules were laminated in a vacuum laminator for 20-25 mins at a temperature of 135 °C [1]. The customization of modules is further explained in the table as under:

Table 3.1 Module Specifications.

| **Panel Designation** | **Manufacturer** | **Type of Cells** | **Glass type** | **Encapsulation film type** | **Maximum Output Power** |
|---|---|---|---|---|---|
| **1** | International | Polycrystalline | Soda Lime Glass | EVA film | 11.7 |
| **2** | Local | Polycrystalline | Quartz glass | EVA film | 15.6 |
| **3** | Local | Polycrystalline | Soda lime Glass | PVB film | 14.4 |
| **4** | Local | Polycrystalline | Quartz Glass | PVB film | 11.9 |
| **5** | Local | Polycrystalline | Soda Lime Glass | EVA film | 11.8 |

## 3.3 Pre-testing procedures

Pre-testing procedures include various tests for determining the electrical, physical and performance parameters of the PV modules before the PID phenomenon is applied. The pre-testing procedures include various tests mainly starting with Stabilization of PV panels, Maximum power determination, Visual Inspection, Dry Insulation test, wet leakage current test (Optional), Ground continuity test (Optional), IR imaging (Optional) and Electroluminescence Imaging (Optional). Some additional/optional tests can be performed depending upon the availability of the testing machinery and conditions. Here some of the pretesting procedures that are to be performed practically are explained in detail.

### 3.3.1 Stabilization of PV panels

The stabilization also known as preconditioning is the preliminary step for testing of photovoltaic modules. For this process all the modules are to be exposed to sunlight (real or stimulated) to an irradiance level equal to 5kWh.m$^{-2}$ while open circuited. The modules can be exposed to natural sunlight or stimulated light through a solar simulator. The preconditioning/stabilization of the modules is performed strictly following the IEC 61215 standards [2].

In this case, the panels were mounted on stands having tilt angle equal to 33.6. The panels were connected to load equal to the characteristic resistance of the PV modules, that was calculated by dividing the $V_{MP}$ by $I_{MP}$ i.e.

$$Rsh=V_{MP}/I_{MP}$$

The modules were exposed to direct sunlight for 3 days. The equipment used to measure the irradiance during the stabilization period is a Hukseflux Pyranometer (LP02) as shown in figure 3.1.

Once the panels were exposed to the required irradiance levels according to IEC standards 61215, the panels are stated as stabilized.

Figure 3.2 Stabilization of Modules by sunlight exposure.

### 3.3.2 Visual inspection

Visual inspection is carried out for type approval and design qualification of the photovoltaic modules before testing. The defects included in visual inspection are:

- Broken or cracked external surfaces that include substrates, superstrates, metallic frame and junction box.
- Delaminations or bubbling which result in forming a continuous path between the edge of the module and any part of the electrical circuit.
- Cracks on the solar cell surfaces in worst case scenarios can remove 10% of the cell's area from the electrical circuit of the module.
- Loss of mechanical reliability, to the extent that the operation of the module would be impaired [2].

All the modules were visually inspected in order to reveal any visual defects. The front glass, laminations, edge seal, frame, junction box, bus bars, encapsulant, back-sheet and bypass diodes are thoroughly inspected to reveal any damages. This test can be done by taking HD pictures of the modules and then studying detailed images to reveal any defects. The figure shows the picture of a module taken during visual inspection. The visual inspection is done following IEC standards 61215 [2].

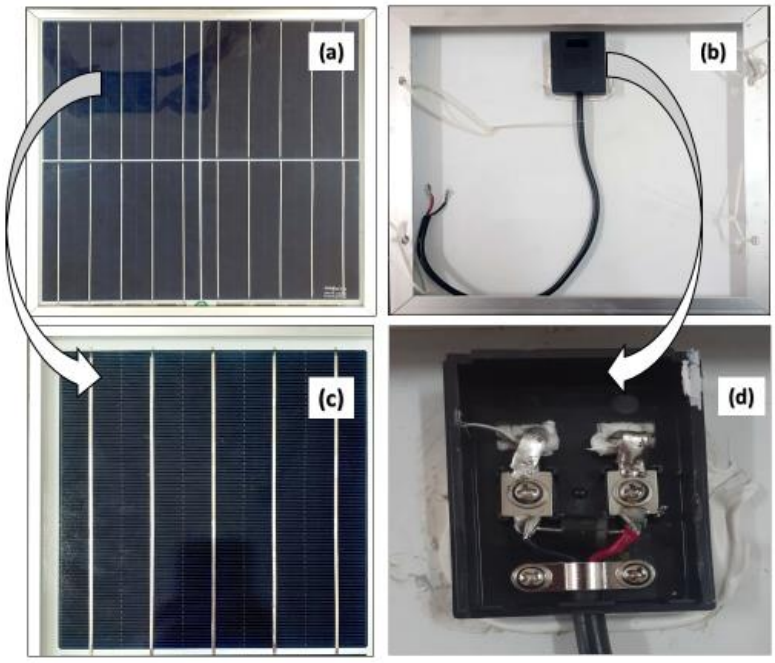


Figure 3.3 (a) Front-view of poly-crystalline PV module (b) Back view of module (c) Close-up image showing single poly-crystalline PV cell and frame (d) Closeup image of junction box.

### 3.3.3 Maximum Power Determination

This test is performed to determine the maximum power of the module before and after various environmental tests. The test is performed strictly under standards IEC 60904. The most important factor of this test is the repeatability. A radiant source or solar simulator is used as a source of light for performing the test. Test specimen along with a reference device; reference device having the same size and cell technology as the test specimen are used. The current and voltage determination is done at a specific set of temperature and irradiance conditions in accordance with IEC standards 60904-1. Current, voltage, irradiance and temperature monitoring devices are used to determine the I-V characteristics of the PV modules. The repeatability of this test should be better than ±1%. Accuracy in measuring the current, voltage and temperature of the test specimen and reference device is essential in the entire test setup [2].

Maximum power determination is performed on all the modules before and after the PID test in order to determine the effects of PID on the modules. As a result of which maximum

power determination is one of the most important performance tests to be performed on the modules as it reveals important parameters like $V_{OC}$, $I_{SC}$, $P_{max}$ and FF. The equipment used for the test is Daystar D-1000 IV Curve Tracer. And the software used for normalising and editing graphs is called IVPC. For temperature and irradiance measurement thermocouples and irradiance meters are used. The test is performed in natural sunlight following the IEC standards 60904. The results are concluded in form of an IV curve in IVPC software via computer/laptop interface revealing various parameters like $I_{SC}$, $V_{OC}$, $P_{max}$, $I_{max}$, $V_{max}$, and FF of the module under testing. The IV curve obtained is normalised by entering the temperature coefficient value of $V_{OC}$ ($\beta$) of the module tested in the software using approximation method. Figure shows the outdoor testing setup of a poly-crystalline module using the IV curve tracer.

Figure 3.4 Daystar IV Curve Tracing Setup showing module during test.

### 3.3.4 Electroluminescence imaging

Electroluminescence imaging is a powerful diagnostic tool in determining the effects of PID mechanism on PV modules before and after performing the PID test. The electronic and optical characteristics of the module are effectively determined by this testing procedure. Defects limiting the performance like PID, cell fractures and micro-cracks are noticeable through EL imaging. The EL image is detected when recombination of charge

carries occurs in a semi-conductor p-n junction of the solar cells in a PV module. The electroluminescence intensity is directly proportional to the number of available minority charge carriers. Thus, a low intensity electroluminescence indicates the presence of defects in crystal structure that limits the radiative recombination process [3]. The EL testing setup includes a dark room with CCD (Charge-coupled device) camera, a programmable power supply and measurement software. The camera used in the test setup is NIKON D5300. The EL image obtained as a result of the test clearly displays the effect on the solar cells after PID tests. The defected solar cells of a PV module appear darker as compared to the cells before PID test was performed [4]

The EL imaging is performed both before and after the main PID test, in order to determine the effects of the potential induced degradation mechanism on the modules. The test is performed by applying the $V_{OC}$ and $I_{SC}$ values of the module under test through a DC power supply. The injected $I_{SC}$ and $V_{OC}$ values result in a better glow when the picture is taken in the dark using EL camera following the phenomenon of Electroluminescence. The captured EL image is then saved in an EL imaging software via computer interfacing. The schematic setup of an EL imaging test is shown in figure [5].

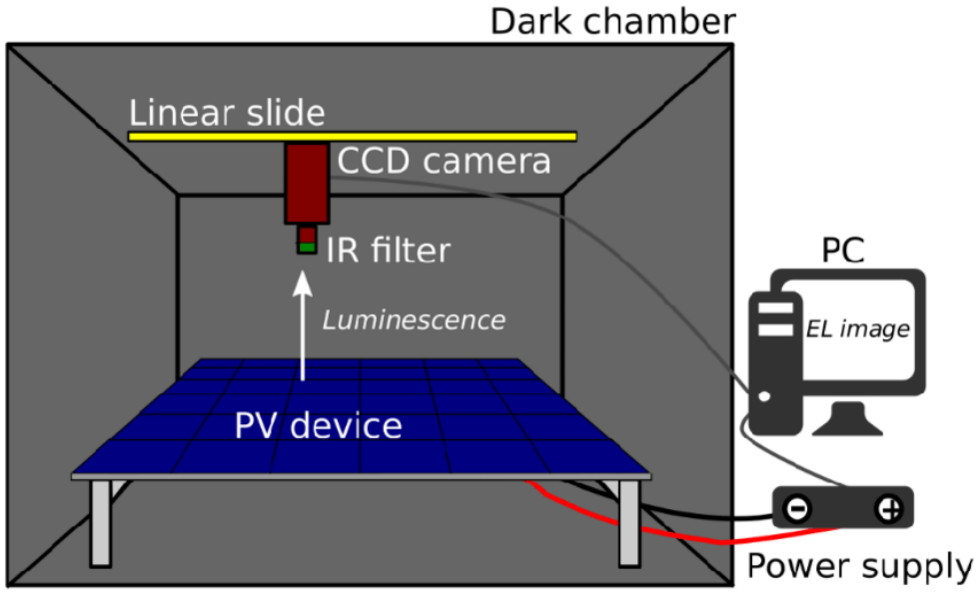


Figure 3.5 Schematic diagram of EL imaging setup [5].

### 3.3.5 Dry Insulation Test

The insulation test is performed to determine whether the module under test is adequately insulated between the frame and the current carrying parts or the outside world. The test is performed strictly under standards IEC 61215. The test is performed on modules at ambient temperature and on relative humidity not greater than 75%. The equipment required for the test consists of:

- DC Voltage source capable of applying 500 or 1000V plus twice the system voltages of the module under test.
- An instrument to measure insulation resistance, if not available then an instrument that measures leakage current can be used so that insulation resistance can be calculated from the measure leakage current values using formulas as shown in equations 5 and 6 [2].

Insulation test procedure is as follows:

- Place the module on a wooden table to provide insulation for safety purposes.
- Short the output terminals of the module and connect it to the positive probe of the DC voltage source.
- Next connect the negative probe of the voltage source to the exposed metal part of the module i.e., the frame.
- If module is having system voltages not exceeding 50V, then apply voltage equal to 500V plus twice the system voltages on the module for 1 minute i.e., the dwelling time. Apply the voltages at ramp rate not exceeding 500V/sec.
- In case module has system voltages greater than 50V, apply voltages equal to 1000V plus twice the system voltages on the module for 1 minute i.e., the dwelling time.
- Reduce voltages to zero and short circuit the terminals to discharge build up charges.
- Then remove the short circuit and again apply voltages (not exceeding the rate of 500V/sec) equal to system voltages of the module for dwell time equal to 2 minutes.

- Determine the insulation resistance or leakage current at this point, in case of leakage current determine insulation resistance through formula:

$$R_{insulation} = \frac{\text{Applied Voltage}}{\text{Leakage Current}} \quad (5)$$

And

$$\text{Resistivity } (\rho) = \text{Resistance} \times \text{Area}(m^2) \quad (6)$$

- In case of panels having area greater than 1 $m^2$, the resistivity should not be less than 40 MΩ-$m^2$, while for panels having area less than 1 $m^2$ the insulation resistance should not be less than 400 MΩ [2].

The test is performed before and after PID test to determine the changes in insulation resistance after being subjected to PID. The figure shows the setup for dry insulation test.


Figure 3.6 Dry Insulation test setup showing module under test.

### 3.3.6 Wet Leakage Current test

Wet leakage current test is similar test to dry insulation test but is performed by immersing modules in a water tank upside down with the glass side immersed in the water. The test is performed strictly under standards IEC 61215. The wet leakage current test procedure as follows:

- The water used to perform the test must be at room temperature (22°C±3°C).
- The resistivity of water must be less than 3500Ω-cm.

- Detergents and dishwashing soaps are used to reduce the resistivity of water.
- In case of outdoor testing, the modules are sprayed with water than being immersed in water tank.
- Immerse a copper wire or any conducting material like iron rod in the water (as an electrode) and connect the other end (the dry end) to the negative probe of the DC voltage source.
- Connect the shorted terminals of the module to the positive probe of the DC voltage source.
- Make sure the connections made with the DC voltage source are dry.
- Rest all the procedure is similar to dry insulation test including executing the test and recording the results [2]. The test setup is shown below in figure.


Figure 3.7 Wet Leakage current test setup showing module under test.

## 3.4 PID Test Setup

The Potential Induced Degradation test is performed in an environmental chamber capable enough to induce and maintain the environmental conditions required for the test. The chamber is accompanied by a DC Voltage power supply that is capable to apply voltages greater than 600V on the modules under PID tests. An insulating stand is also required for PID test that can hold the PV modules under test and provide insulation to the environmental chamber from the module that is under high voltage stress. The PID test

setup is the most important and crucial stage because it requires preliminary examination of the entire set up to prevent any hazard due to high voltages applied on the module under accelerated environmental conditions during the PID test. The step-by-step process in preparing PID testing setup is explained in detail below.

### 3.4.1 Environmental Chamber

An environmental chamber is used to induce desired temperature and relative humidity conditions that are required for the PID test. The chamber used for the PID test is UTSTESTER E001 Programmable Temperature and Humidity Chamber. The chamber consists of fixed test and programmable test options. The PID test program is designed under the chamber's programmed test option. The programming inside the chamber is controlled through Proportional Integral Derivative (PID) controllers. For production of humidity inside the chamber, distilled water is used, that can be introduced and removed from the chamber when required. The chamber is provided with a provision for inlet of the testing cables/wires. The chamber is supported with USB interfacing, the required data and graphs can be exported in an USB in excel format via USB port. The chamber used in the test is shown below.


Figure 3.8 Environmental Chamber.

### 3.4.2 Insulation Stand

In an environmental chamber during PID test high voltages (above 600V) are applied on the PV module. In order to prevent the internal body of the chamber from being exposed to such higher voltages that may cause a serious hazard, an insulating stand is devised. The insulation is provided through 1500KV pin insulators. The two insulators are held on an iron hollow square bar and are fastened in position using the pin of the insulator.

The insulating stand has a PVC pipe structure held tight on the insulator pins, to hold the shorted module terminals under negative high voltages during the PID test. Cable ties are used to hold the module in horizontal position with glass side facing toward the bottom of the chamber. As the modules are light in weight, cable ties provide strong hold. Figure shows the insulating stand holding PV module in position inside the environmental chamber.

Figure 3.9 Insulation Stand for holding PV module inside environmental chamber.

### 3.4.3 DC Power Supply

DC Power Supply is used in PID test to provide the required voltage stress. The power supply used in the test must have low current rating and very high precision for accurate readings. The low current rating (in milliamperes) helps prevent hazardous conditions under high voltage stresses. The DC power supply used in the test is Stanford PS350 that can apply voltages up to 5000 V and with a maximum current rating of 5mA. Before inducing voltage stress in the PID test, the DC power supply is tested by applying voltages on a PV module in open environment and recording the current using a sensitive ammeter as shown in figure. This is done to ensure that the nameplate values of voltages and current of the power supply emulate the real time testing values and are in safe limit for performing PID test.


Figure 3.10 Outdoor application of high voltages on module using Standford DC power supply.

### 3.4.4 Ground continuity test

Ground continuity test is performed to verify that electrical continuity exists between the exposed conductive parts of the of the PV modules. The test is performed strictly under standards IEC 617320-2. The test verifies the capability of modules to provide protection against shock during use. For this purpose, a ground continuity tester is used to determine the maximum acceptable resistance and 0.1Ω has been commonly used as the maximum acceptable resistance of the PV modules. The ground continuity tester used is Kyoritsu electrical continuity tester 3005A. The insulation resistance can be tested at three rated test voltages 250, 500 and 1000V. The insulation resistance is measured at the module's rated system voltages. The measured resistance values of all the modules should be within the maximum limits of acceptable insulation resistance, so that the PID test can be performed with complete safety.

## 3.5 PID Test

The PID test is performed following the IEC standards 62804. The standard PID test is performed at 60°C temperature and 85% relative humidity (RH) for 96 hours inside environmental chamber. Module's rated voltage is applied between the modules shorted leads and metallic frame during the test. In this case the test is designed to be conducted at 60°C, 85% RH for 5 hours dwell time at module's rated system voltage i.e., 1000V [6].

### 3.5.1 Procedure:

The module under test is mounted on the insulating stand and held firmly on place inside the chamber using cable ties. The module's positive and negative terminals are short and attached to negative probe of the DC power supply and positive probe of the power supply is attached to the exposed part of the metallic frame. The connections are thoroughly checked to avoid any path for leakage current [6]. The environmental chamber is then turned on and set on program test. The environmental chamber is programmed with four basic tasks to achieve desired temperature and humidity conditions for the PID test.

1. Stabilization: Task 1 is programmed to achieve 70°C temperature and 50% RH in time duration of 7 minutes. This step is performed to dry out any accumulated moisture or droplets on the module surface or the internal chamber body before the start of the PID test. This is done to reduce the leakage current in the start of the test.
2. Ramp up: Task 2 is programmed to achieve the 60°C and 85% RH in time duration of 15 minutes. This step is performed to achieve the desired PID testing conditions. As the chamber's temperature and relative humidity can only be functioned simultaneously so the program is created to achieve both the testing conditions at a time. Once the desired environmental conditions are achieved the voltage is turned on and is ramped up gradually up to 1000V with increment of 100V. The leakage current is recorded during each increment of 100V up to 1000V using the same Stanford power supply.
3. Dwell Time: Task 3 is the programmed to maintain the 60°C temperature and 85% RH for a duration of 5 hours. During the dwell time, the voltage is maintained at 1000V. The leakage current of the modules under test is recorded every 5 minutes during the entire dwelling time.
4. Ramp Down: Task 4 is programmed to ramp down the chamber to ambient conditions i.e., 30°C and 60% humidity in a time duration of 5 minutes. Once ambient conditions are achieved the DC power supply is turned off. Following the chamber is switched off and the module is removed from the chamber.

All the modules are tested following the same procedure. The PID testing procedure can be further elaborated through figure as shown below.

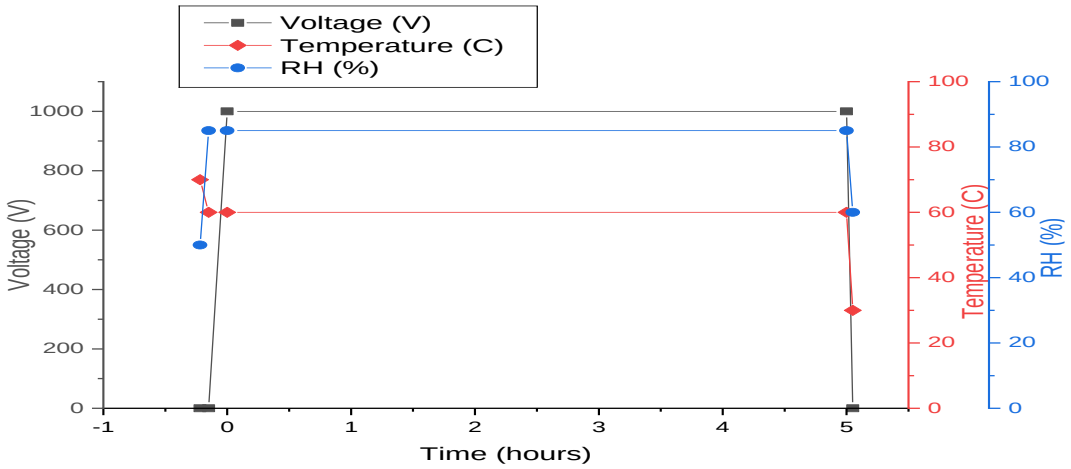


Figure 3.11 PID test voltage time-temperature-humidity profile for application of stress in an environmental chamber.

## 3.6 Post testing

The PID test is performed on the module, it is necessary to conduct the Pmax determination test, dry and wet insulation test within 8 hours of the PID test for accurate results. The EL imaging can be performed within 12 hours duration post PID test for best results. The tests have been thoroughly discussed in sections 3.2.3, 3.2.4, 3.2.5, 3.2.6. The tests are performed in the similar manner as explained earlier in this chapter and results are recorded. Further analysis is performed on the results obtained for better interpretation of the tests performed.

## Summary

In this chapter, the methodology to perform the various tests for PID is explained. A detailed flow chart explains the workflow on how the tests are designed systematically. For the main PID test a series of pre and post testing procedures are required to be performed and that are explained in detail in this chapter. The standards for the pre-testing procedure, PID testing, and post testing procedures are discussed in detail. The tests include stabilization, Visual inspection, Pmax determination, dry insulation test, wet insulation test, EL imaging and the main PID test. The standards for these procedures that are IEC 61215 AND IEC 62804 are also discussed in detail. The main PID test and the prerequisite procedures required for PID tests are also explained in detail in this chapter. Real time testing images are also shared in detail in this chapter to further explain how the tests are performed in real time. This chapter thoroughly explains each detail required for understanding how the testing procedures are performed. The main focus i.e., the PID test is methodically explained, starting from how it is specified in standards and how the testing conditions can be altered to suit your requirements.

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# Chapter 4

# Results and Discussion

## 4.1 Introduction

The chapter contains test results and data analysis performed for investigating the effects of PID on poly-crystalline PV modules. The electrical parameters before and after the test were analysed to conclude the effect of PID on the modules tested. The leakage current graphs were plotted to determine how the leakage current behaviour changes with temperature, humidity, and voltage stress. IV curve graphs for all modules were observed before and after PID test. EL imaging was performed on modules before and after the main

PID test to detect any visible defects on modules. And insulation resistance of modules is calculated using formulas before and after the PID test by performing dry and wet leakage current tests. Firstly, the module's leakage currents are analysed before the test and during the test to determine how leakage current's behaviour varies in module having different encapsulation and glass.

## 4.2 Leakage current behaviour of modules

All the modules were tested outside the PID chamber under ambient conditions and inside the chamber under PID testing conditions by applying negative voltages using DC power supply. The leakage current for all the modules were logged and analysed to determine how the currents vary before PID test and during PID test. Leakage current measurements for the PID stress test are primarily used as an indicator of stability of the test environment (i.e., chamber conditions; temperature, and humidity). Initially leakage current behaviour is analysed outside the chamber and later during the PID test.

### 4.2.1 Before PID test leakage current behaviour:

All the modules are tested outside the chamber under ambient conditions to determine the leakage current behaviour. The modules are tested by applying negative voltages on modules starting from 100V up to 1000V with an increment of 100V and results are

obtained. Graphs of leakage currents of all modules are plotted against voltages to determine the variation of currents with higher voltages and to determine that the module's currents are within safe limits to perform PID test as shown in figure 4.1

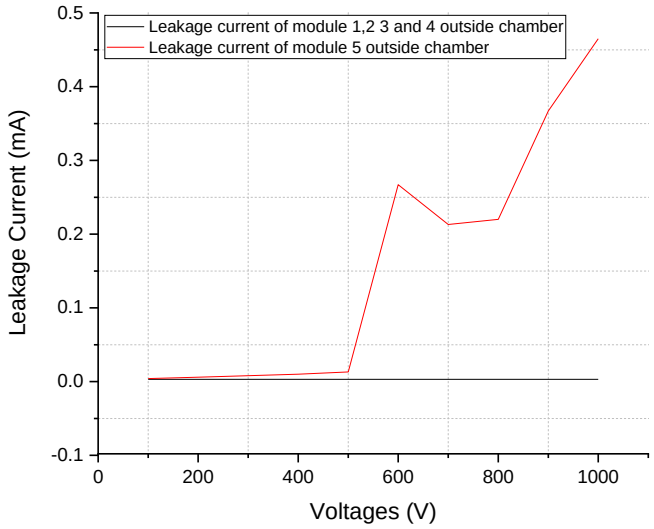


Figure 4.1 Leakage current plotted against voltage applied outside the chamber.

For all modules except module no 5, the leakage current remains constant starting from 100V up to 1000V, revealing that the modules are firmly laminated with no variation in currents while applying voltages in ambient environment. The results of leakage current show that all the modules have leakage current within safe limits when voltage is applied outside the chamber.

### 4.2.2 Leakage current behaviour inside environmental chamber

Before conducting the actual PID test on the modules inside the chamber, all modules are tested once by applying voltages on each module inside the chamber, when the chamber is at 60°C and 85% RH. The voltages are applied starting from 100V up to 1000V with an increment of 100V. The leakage current was recorded, and graph was plotted against voltage as shown in the following figure. The modules 1, 2, 3 and 4 showed variations in leakage currents w.r.t voltage, temperature, and humidity in a manner that the currents remained in safe limits for all the four modules to be tested for the main PID test. As the increase in leakage w.r.t voltage, temperature and humidity of modules has already been

studied in numerous papers, the modules showed similar variation [1]. The four modules titled as modules 1, 2, 3 and 4 had different leakage current behaviour under the same environmental conditions because of basically two main reasons. One reason is that all the modules differ from each other on basis of encapsulation sheet and front glass material. The volume resistivity, rate of water vapor transmission rate (WVTR) and the adhesion property of the materials used plays an important role in effecting the leakage current flow within the module [2][3][4][5].

And the second reason for varying leakage current behaviour of all modules is that the environmental conditions inside the chamber may vary for each module, because the modules may have moisture on its surface in form of droplets causing higher leakage currents than usual. Reason for accumulated moisture on modules is that all the modules were set up on the insulated stand inside the chamber for hours prior to the experiment to be performed. Because of being inside the chamber for longer hours, moisture accumulates on the surface of modules in the closed environment. But the leakage currents remained within safe limits, qualifying the four modules for the PID test. Among these four modules, the module no 2 (Poly+Quartz+EVA) showed lowest leakage current variations during the entire voltage stress at accelerated environmental conditions, while the module no 4 showed the highest variation in leakage currents (Poly+Quartz+PVB) as shown in figure 4.2.

But the module no 5 (Poly+EVA+Soda lime glass) showed large variation in leakage currents w.r.t high voltage. The leakage currents were as high as 5mA at 1000V inside the chamber as shown in figure 4.2. Higher leakage currents are mostly associated to frame, junction box and back sheet defects i.e., frame cracking, frame corrosion, loose junction box, broken junction, backsheet delamination etc. There were no visible defects in module no 5, so it can be concluded that the high leakage currents may be because of mishandling during lamination of the module or during frame and junction box connections. Because of such high leakage currents the module could not be further tested for PID. Ultimately, the main PID test was performed on modules 1, 2, 3 and 4.

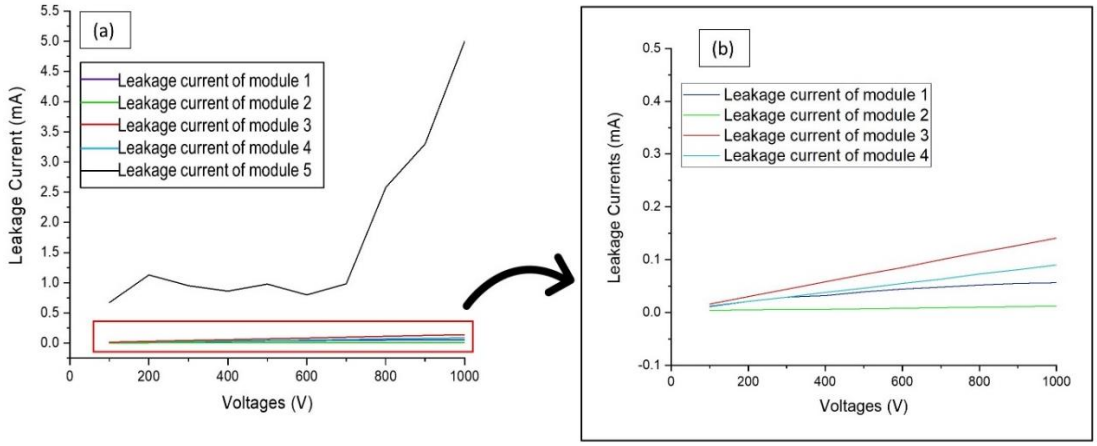


Figure 4.2 (a). Leakage current behaviour of module 1, 2, 3, 4 and 5 under voltage stress and accelerated environmental conditions inside chamber. (b) Zoom in graph of leakage current of module 1,2,3 and 4 under same conditions.

### 4.2.3 Leakage current behaviour during PID test

The PID test was performed on module 1, 2, 3 and 4 for 5 hours inside the environmental chamber under voltage stress of 1000V at 60°C temperature and 85% RH. The leakage current was recorded every 5 minutes during the test and was plotted against time in a graph for each module as shown in figure 4.3.

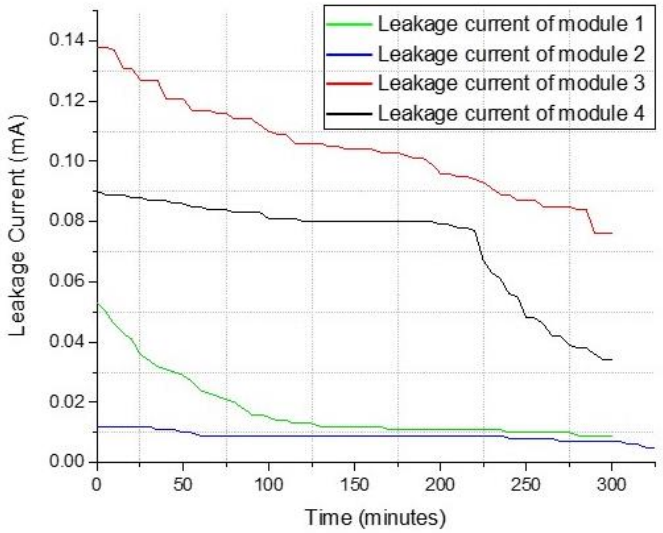


Figure 4.3 Leakage current of the four modules during PID test at 1000V, 60°C and 85% RH for 5 hours.

There are various factors effecting the leakage current flow, one dominant factor is that all the modules were set up inside the chamber prior to the PID test. This was done in order to save time on the day of performing the PID test. Because the module is placed inside the chamber (when off) for hours, moisture is accumulated which may be one of the causes of large leakage current. The other factors include encapsulation's volume resistivity, WVTR, adhesion property and glass sheet's strength. It can be clearly seen in the graph that other than the accumulated moisture the major reason for greater leakage currents in module no 3 and 4 is that both of the modules have PVB as the encapsulation material and the PVB sheet used in this case is a new formula encapsulation film that has good adhesion property and impact resistance, also its volume resistivity is close enough to that of standard EVA but the WVTR is slightly greater than the EVA sheet used in the other two modules. Because PVB has greater WVTR rate it is more prone to moisture ingression and transmission as compared to EVA [6]. The module no 2 showed lowest leakage current rate during the entire PID test. The quartz glass could be the reason of lower leakage current flow accompanied by EVA sheet as encapsulation. Quartz glass used has high resistivity as compared to soda lime glass and provides better electrical isolation reducing the leakage currents [7][5]. This can be counter proved by observing the leakage current behaviour of module 3 and 4. Module 3 has PVB sheet accompanied by soda lime glass, while module 4 has the same PVB encapsulation sheet accompanied by quartz glass. And it can be clearly observed that the leakage current in case of module 4 is less than that of module 3 owing to greater resistivity of quartz glass. Also, there was no correlation observed between leakage current and power loss of modules.

## 4.3 Maximum Power determination test results before and after PID

Maximum power determination test was performed before and after PID test on the four modules, IV and power curves were obtained. All modules showed degradation, dominantly effecting the $P_{max}$ and $V_{OC}$ of modules as shown in table 4.1. The degree of depression in $V_{OC}$ is larger than that in the $I_{SC}$ owing to the decrease in shunt resistance [8][9]. Results revealed that the module no 1 procured from China showed the highest degradation because of PID while the manufacturers claimed that the module is PID resistant since it was fabricated using PID resistant poly-crystalline solar cells. The % power degradation showed by the module 1 was 32%. The second highest degradation

was observed by the module no 2 that was laminated using c-Si solar cells, quartz glass and EVA film. The module showed 17% degradation in power which is less compared to the module 1 owing to the quartz glass that was used in fabrication of module 2. The quartz glass used in the module is has higher fatigue exponent and less alkali content. The higher fatigue exponent increases the overall strength of glass and its lifetime durability [7]. While lower alkali content means the glass has lower content of sodium ions, which are considered responsible for the potential induced degradation phenomenon [1][10][11]. Likewise, lower alkali content represents higher resistivity. The quartz glass volume resistivity ranges between $10^{16}$ to $10^{18}$ which is much superior to that of the conventional soda-lime glass ($10^{10}$-$10^{11}$) commonly used in manufacturing of PV modules [7]. Soda lime glass has lower volume resistivity and strength but is being commonly used in manufacturing of PV modules because it is cheap and easy to produce. Quartz glass is comparatively expensive to soda lime glass due to which it is not used widely in commercial PV modules but comparing the results of modules 1 and 2 clearly indicate a major difference in power degradation. Module 2 incorporating quartz glass as superstrate showed 15% less degradation in power compared to module 1 incorporating conventional soda-lime glass as superstrate revealing that quartz glass incorporated PV modules could be a favourable tradeoff between price and power degradation. The quartz glass used in these modules was relatively reasonable in price as it was manufactured in a local glass industry, making it a far better candidate against PID. Furthermore, polycrystalline solar modules have pretty much achieved the affordability feature after years of research in making the technology affordable but are still lagging in achieving reliability and our approach focuses on improving reliability for a longer module life and performance against the PID phenomenon.

Module no 3 showed less degradation in power compared to module 1 and 2 after PID test. The module 3 was fabricated using highly resistant PVB film and standard soda lime glass. The manufactures of the PVB film (procured from China) claimed that the film was made using a new formula and had higher resistivity and durability compared to the standard EVA film being widely used in the country for locally fabricating PV modules. The module 3 showed only 10% of degradation in power revealing that the PVB film showed greater resistance towards PID owing to its higher volume resistivity compared to

EVA film laminated modules (module 1 and 2). Although the film showed higher resistivity towards PID phenomenon, but the WVTR rate of the film was slightly less than the standard EVA film due to which the leakage current values during the PID test were higher as compared to modules having EVA as encapsulant. PVB film is also well known for its good adhesion properties due to which it shows high impact resistance [12]. The hydroxyl group in PVB are responsible for its good adhesion properties with majority of substrates specifically with glass. Because of good adhesion the PVB film shows good resistance against PID phenomenon [13]. The reason why EVA film despite of having high volume resistivity shows higher degradation due to PID is because of its higher vinyl acetate (VA) content. At higher temperatures the VA content in the EVA film converts into acetic acid. At elevated temperatures and higher rate of UV illumination, the acetic acid splits off from the EVA film. Additionally, in the presence of moisture and acetic acid the ionic concentration increases and resulting in accelerating PID. Another reason that EVA sheet is not a suitable encapsulation against PID because the volume resistivity of EVA drops two orders in magnitude from temperatures 23°C to 75°C. And PID phenomenon is majorly observed at higher temperatures between 60°C to 85°C, so the volume resistivity of the EVA sheet reduces at higher temperatures leading to higher leakage current and greater susceptibility to PID [14]. Due to this phenomenon, the PVB film shows less PID as compared to EVA [12][15][16]. Trade names for PVB films like Butacite, Trosifol, and Everlam have been tested and reported to show good resistance in stress testing owing to their strong physical and chemical properties [17].

Countless studies reveal that the most dominant path for PID to occur is from the surface of the front glass, through the bulk of the superstrate and encapsulation [1], [5]. And it has been documented in many studies that the adhesion of PVB film with glass is stronger than that of the standard EVA film [6], [13], [18]. So PID is less likely to occur following the aforementioned path owing to strong adhesion of PVB film with glass sheet. Moreover, one common reason linked with PVB film is its comparatively lower adhesion to plastics (backsheet) as compared to other encapsulations leading to a potential leakage current pathway resulting in PID. But studies also reveal that the leakage current pathway that is least likely to be the cause of PID is the one in which the current passes along the surface of the backsheet, and from the bulk of the back-sheet and encapsulant, and is often ignored for two main causes; (i) the high electrical

resistance of the plastic/polymer back-sheet and (ii) complete metallic covering offered by the aluminium back field over the semiconductive layering on the back side of the crystalline silicon photovoltaic cells [5]. Owing to this hypothesis, the weak adhesion of PVB with plastics (backsheet) can be ruled out as a potential reason for PID as the resistance of the backsheet will prevent the flow of leakage current through itself and the encapsulant in the first place.

The module 4 showed best results by being highly resistant to PID. The % loss in maximum power was negligible i.e 1% only. The module 4 showed impecible resistant to PID owing to the PVB encapsulation film and Quartz glass. Both the glass and encapsulant had better volume resistivity and impact resistance as compared to their standard substitutes i.e. Quartz glass and EVA sheet. The results of module 4 revealed that by replacing both the encapsulant sheet and front glass with materials that are having better electrical resistance , adhesion and rigidity could reduce the PID phenomenon to as little as being negligible.

Finally, it can be concluded that selecting a suitable glass sheet and encapsulant type could help reduce the PID effect significantly. Alternatives to the soda-lime glass like quartz glass proved to be a promising candidate in reducing PID, owing to the lower sodium ion concentration and higher volume resistivity. The price of quartz glass is comparatively a little higher than the soda-lime glass but is the best option if the reliability of modules is the major concern as in this case.

PVB encapsulation film seemed to be a better alternative to the locally available EVA film used in module fabrication. As most of the local market manufactured PV modules use low-quality EVA film in lamination that results in greater PID susceptibility. The local manufactures should import encapsulants, solar cells, and glass sheets by considering electrical and physical parameters following the datasheets for better reliability and performance of modules. Since the eventual selection of suitable superstrate and encapsulant depends on the cost of the materials and on the reliability of the modules under other environmental stresses such as UV, it is important to further evaluate the PID-investigated materials from long-term field reliability perspectives.

Table 4.1 Electrical Parameters of all modules before and after PID test.

| Panel No | Panel Customization | PID Stress | VOC (V) | ISC (A) | Vmax | Imax | Pmax (W) | FF (%) | % Pmax Degradation |
|---|---|---|---|---|---|---|---|---|---|
| 1 | **Standard Poly-crystalline module** | Pre | 2.525 | 8.833 | 1.579 | 7.434 | 11.7 | 52.7 | 32% |
| | | Post | 2.337 | 9.164 | 1.233 | 6.456 | 8.0 | 37.2 | |
| 2 | **Quartz glass+EVA film** | Pre | 2.590 | 8.192 | 2.040 | 7.632 | 15.6 | 76.2 | 17% |
| | | Post | 2.535 | 6.727 | 2.008 | 6.470 | 13.0 | 73.4 | |
| 3 | **Soda lime glass+PVB film** | Pre | 2.538 | 8.256 | 1.898 | 7.598 | 14.4 | 68.8 | 10% |
| | | Post | 2.225 | 8.937 | 1.599 | 8.115 | 13.0 | 65.3 | |
| 4 | **Quartz glass +PVB film** | Pre | 2.352 | 7.787 | 1.676 | 7.129 | 11.9 | 65.3 | 1% |
| | | Post | 2.324 | 7.930 | 1.636 | 7.234 | 11.8 | 64.2 | |

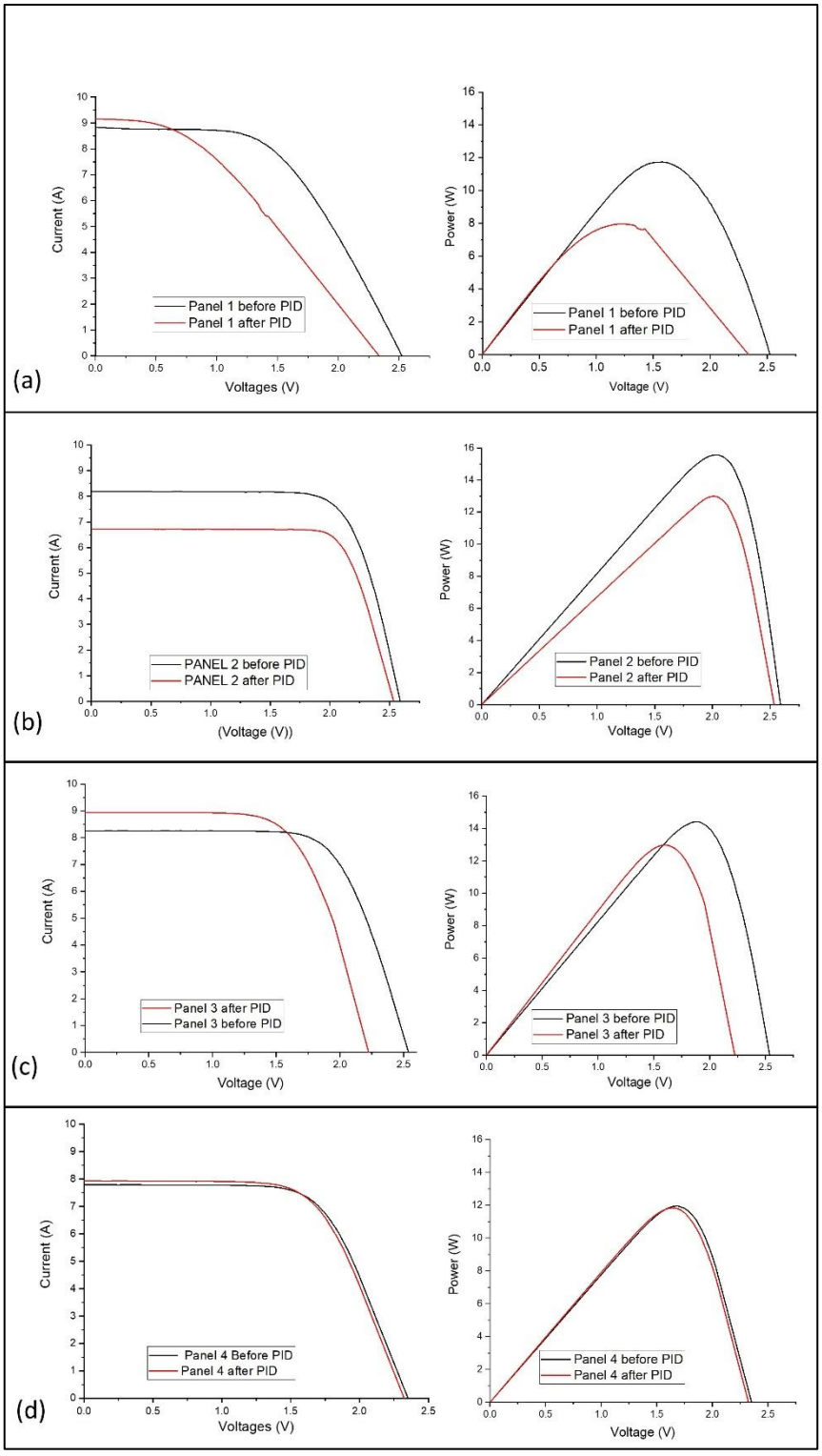


Figure 4.4 IV (Left) and Power (Right) curves of modules before and after PID. a) of module 1, (b) of module 2, (c) of module 3, (d) of module 4.

## 4.4 Dry Insulation test results

The dry insulation test was performed on modules before and after PID test, to determine whether the module's insulation is within safe limits. This is done by calculating the insulation resistance of the module through module's leakage current as shown on the insulation tester and module's area. Results of insulation test reveal that the modules 1, 2, 3 and 4 in spite of having losses in power after PID test qualified the insulation resistance test showing that modules have leakage current and insulation resistance within safe limits. According to standards, the modules must have resistivity greater than 40 MΩ-$m^2$ for modules having area greater than 0.1$m^2$. The modules 1, 2,3 and 4 passed the dry insulation test by having resistivity equal to 1156 MΩ-$m^2$ both before and after PID test making the modules safe for future usage. The results are shown in the table as follows

## 4.5 Wet leakage current results

The results of wet leakage current test performed before and after PID test revealed that modules had resistivity greater than the 40 MΩ-$m^2$ which is referred as a standard in IEC 61215. Modules 1, 2 and 4 had resistivity equal to 1156 MΩ-$m^2$ before and after PID test as shown in the table. While the module 3 had slight lower resistivity equal to 385 MΩ-$m^2$ during the wet leakage current test before PID. But the same module showed high resistivity after PID test. This difference in resistivity may have occurred due to water entering the junction box by mistake or because of excess spray of water on the module or on module contacts. The variation in resistivity of module 3 has nothing to do with any defect in module because if that would be the case the module would have showed similar resistivity after PID test, but it showed higher resistivity equal to 1156 MΩ-$m^2$. Nevertheless, the modules showed resistivity within safe limits passing all the modules in the wet leakage current test after PID.

Table 4.2 Dry leakage current test results of modules before and after PID test.

| Test Parameters | | | Panel 1 | Panel 2 | Panel 3 | Panel 4 |
|---|---|---|---|---|---|---|
| **Total Module Area ($m^2$)** | | | 0.1156 | 0.1156 | 0.1156 | 0.1156 |
| **Leakage Current (µA)** | | | 0.1 | 0.1 | 0.1 | 0.1 |
| **Test Voltage Applied** | | | 1000 | 1000 | 1000 | 1000 |
| **DRY INSULATION TEST** | **Leakage Current (µA)** | | 0.1 | 0.1 | 0.1 | 0.1 |
| | **Insulation Resistivity ($M\Omega$-$m^2$)** | **Before PID** | 1156 | 1156 | 1156 | 1156 |
| | | **After PID** | 1156 | 1156 | 1156 | 1156 |
| **WET INSULATION TEST** | **Leakage Current (µA)** | | 0.1 | 0.1 | 0.3 | 0.1 |
| | **Insulation Resistivity ($M\Omega$-$m^2$)** | **Before PID** | 1156 | 1156 | 356 | 1156 |
| | | **After PID** | 1156 | 1156 | 356 | 1156 |
| **PASS/FAIL** | | | PASS | PASS | PASS | PASS |

## 4.6 EL imaging test results

EL imaging was performed on modules before and after PID test as shown in the figure. The cells that are affected because of PID phenomenon turn darker revealing module degradation. The EL imaging of all the four modules support the IV curve results. Cells of module 1 appeared to be the darkest suggesting severe PID with large shunts on the module's cells, while the cells of module 2 and 3 showed lower degradation compared to module 1 owing to the quartz glass and resistant PVB film. The EL image of module 4 showed no dark areas and was identical to the EL image taken before the PID test. Module

4 showed no degradation and the module's before and after EL images were quite alike, showing no dark areas. The results from EL image reveal that the modules 1 and 2 show severe degradation while module 3 showed slight degradation and lastly module 4 showed no degradation.

EL images before the PID test were performed at current corresponding to the $I_{SC}$. However, EL images taken after the PID test at current equal to $I_{SC}$ did not show the presence of PID affected cells clearly. Hence, the EL imaging of PID stressed modules was performed at a current corresponding to 10% of $I_{SC}$. The EL images obtained at 10% of $I_{SC}$ exhibited lower luminescent intensity, the cells appeared darker and made it easier to identify cells that had degraded due to PID [19], [20], [21]. EL images before the PID test were performed at current corresponding to the $I_{SC}$. Finally, the EL study of the modules supported the IV curve results before and after the PID stress test.

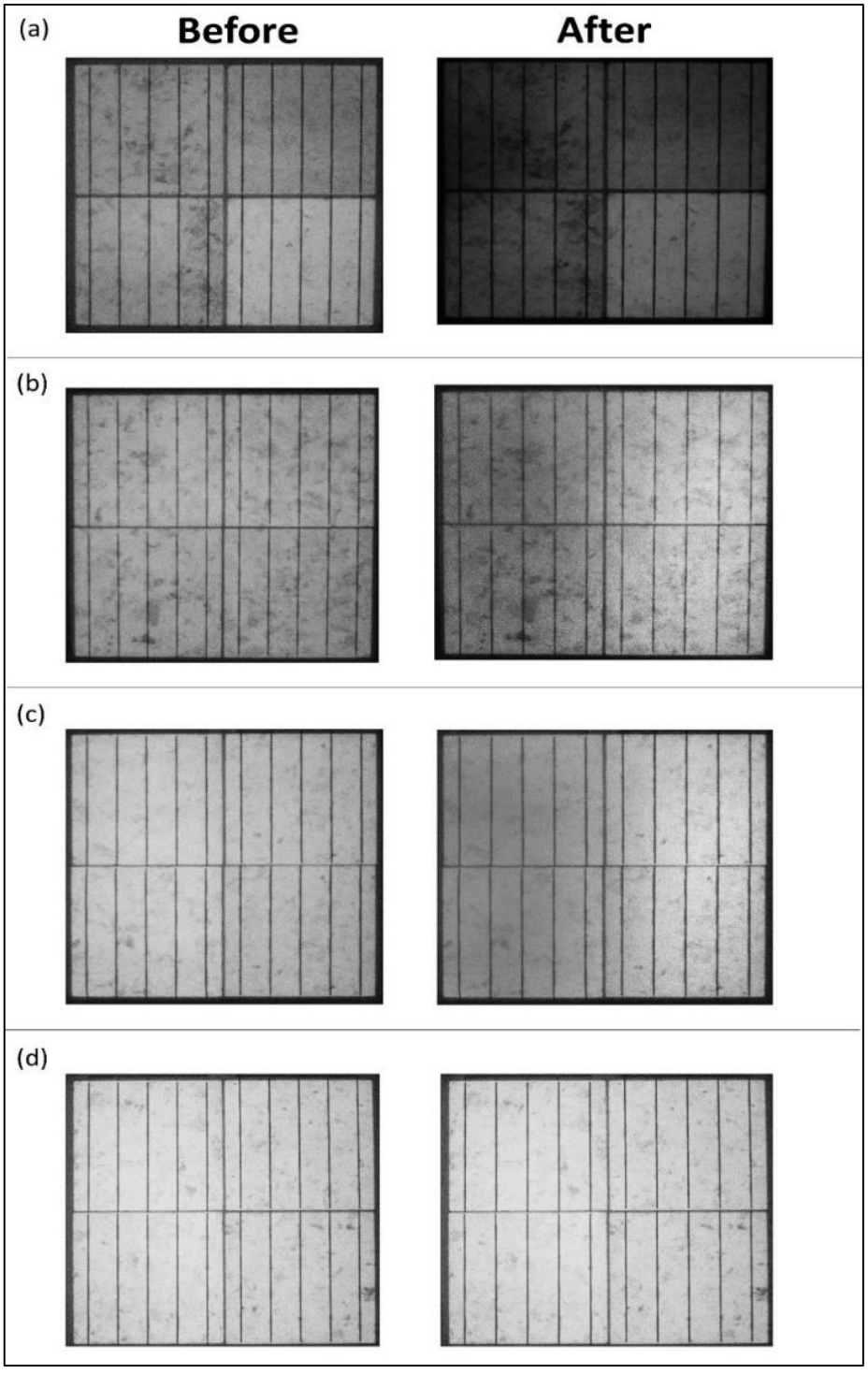


Figure 4.5 EL imaging of Modules before (left) and after (right) PID. (a) EL imaging of module 1 before and after PID. (b) EL imaging of module 2 before and after PID. (c) EL imaging of module 3 before and after PID. (d) EL imaging of module 4 before and after PID.

## Summary

This chapter discusses the results of Potential induced degradation test on different modules. The tests include dry insulation test, wet leakage current test, maximum power determination, EL imaging and the PID test. Leakage current graphs were obtained for all the modules outside the chamber, in the start of PID test inside the chamber and during the entire PID test by applying DC voltage on the modules through a DC power supply. The results of all the tests were discussed in detail revealing that changing the material of glass and encapsulation of the module with a material with greater volume resistivity and adhesion properties can help in reducing the PID. Results of maximum power determination revealed that modules incorporating quartz glass instead of soda lime glass and high-volume resistivity PVB encapsulation instead of EVA helped in reducing PID to as much as only 1% degradation in power after PID test. Dry and wet insulation test results revealed that all the module's leakage current was within safe limits before and after PID test. The resistivity was greater than 40MΩ-$m^2$ as specified as the minimum resistivity in standard. EL imaging was performed on all the modules before and after PID test. The EL images revealed darker areas on modules representing degradation due to PID effect. The chapter summed up the results of all the tests with real time pictures and graphs revealing that modules with electrically resistant glass and encapsulation can help reduce PID to a prominent level.

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# Chapter 5

## Conclusions and Future Recommendations

### 5.1 Conclusions

In the dissertation, potential induced degradation was studied in detail including basic phenomenon behind the process, effects of PID on cell level, module level and system level and methods on how minimize or mitigate the PID phenomenon. The major emphasis was on how PID occurs on module level, what are its causes, how it effects the module's electrical parameters and methods on how PID can be reduced effectively. Module components like solar cells, front glass and encapsulation were studied and how PID could be potentially reduced by changing the material of the components was also discussed in detail. Front glass and encapsulation sheet were replaced with materials having greater volume resistivity and better physical properties that helped in reducing PID effect to a noticeable extent [1][2]. PID tests were performed on modules, and it was concluded that higher volume resistivity materials can reduce PID. The standard front glass i.e., Soda lime glass and standard encapsulation film i.e., EVA film was replaced with higher resistivity Quartz glass and PVB film respectively. And experiments were performed that revealed that PID effect was reduced up to extent that only 1% losses in maximum power was observed in the module that incorporated both PVB film and quartz glass instead of the standard materials. It was concluded from the experiments that the EVA sheet used in majority of the locally manufactured PV modules is not PID resistant and may have lower volume resistivity due to which it showed high PID susceptibility. Also, the local PV module manufacturers didn't provide the details of the EVA film used in lamination leaving an uncertainty of what quality EVA sheets are being used in module manufacturing locally. Whether the EVA sheets used have high volume resistivity to prevent PID phenomenon or not. Along with this, PID tests are not being performed in local PV industries as a standard performance and reliability test leaving an ambiguity whether the manufactured modules and materials used in manufacturing are PID resistant or not. Also, at commercial level there are variety of EVA films available, each having their own chemical and physical properties. As a result of which majority of the local PV

module manufacturers are unaware of the quality, physical, chemical, and electrical properties of the EVA film and glass sheet used in manufacturing leading to production of PID susceptible modules. It can also be concluded from the experiments that quartz glass shows better resistance against PID phenomenon than soda lime glass owing to its lower sodium composition, higher volume resistivity and higher rigidity. And that soda lime glass can be replaced by quartz glass at commercial level PV module manufacturing [3][4][5].

In the experiments performed the standard encapsulation film was replaced by PVB film and modules incorporating the film showed resistance against PID. Unlike most of the PVB film that showed lower resistivity against PID [6], the PVB film used in these experiments showed higher resistance against PID owing to its higher volume resistivity and rigidity. Also, there are variety of PVB films available worldwide each having different physical, chemical, and electrical properties. The PVB film used in this research was procured from China and had high volume resistivity, rigidity, and adhesion properties. So, it can be concluded from this research that not all PVB films have lower volume resistivity, but the new technology PVB films have higher volume resistivity which could be a better option for encapsulation against the standard EVA film [7][8].

Finally, it can be concluded that by replacing the glass sheet, the encapsulation film or both, the effect of PID can be reduced. By selecting materials having higher volume resistivity, rigidity, durability and adhesion properties, the leakage current flowing through module as a result of PID can be reduced. Eventually decrease in leakage current causes increase in the resistance of modules against PID and prevents power losses in modules up to a negligible level.

## 5.2 Future Recommendations

The future recommendations are stated as follows:

- In this dissertation modules were tested at laboratory level. The effect of PID was investigated on newly manufactured modules that had not been used on site. Testing pre-installed on-site modules for PID involves demounting, shipping and laboratory testing and remounting of the site which requires both finances and

manpower. Because of the following challenges, PID was investigated on smaller modules at laboratory level in this research. So, further research can be performed on pre-installed modules onsite.

- The front glass and encapsulant can be substituted with different commercially available material options and each can be tested for PID phenomenon showing severity based on material changes.
- In this research, module's front glass and encapsulation film was substituted to reduce the PID phenomenon. Similarly, changes can be made on cell level as well as system level to mitigate effects of PID.
- After performing PID test on modules, each component of the module including front glass, encapsulation film and solar cells can be delaminated from the module and individually tested for faults/failures through different micro-analysing tests.

## Summary

In this chapter, the entire research process is concluded in a systematic manner. Apart from that, some recommendations regarding future research implications are also suggested.

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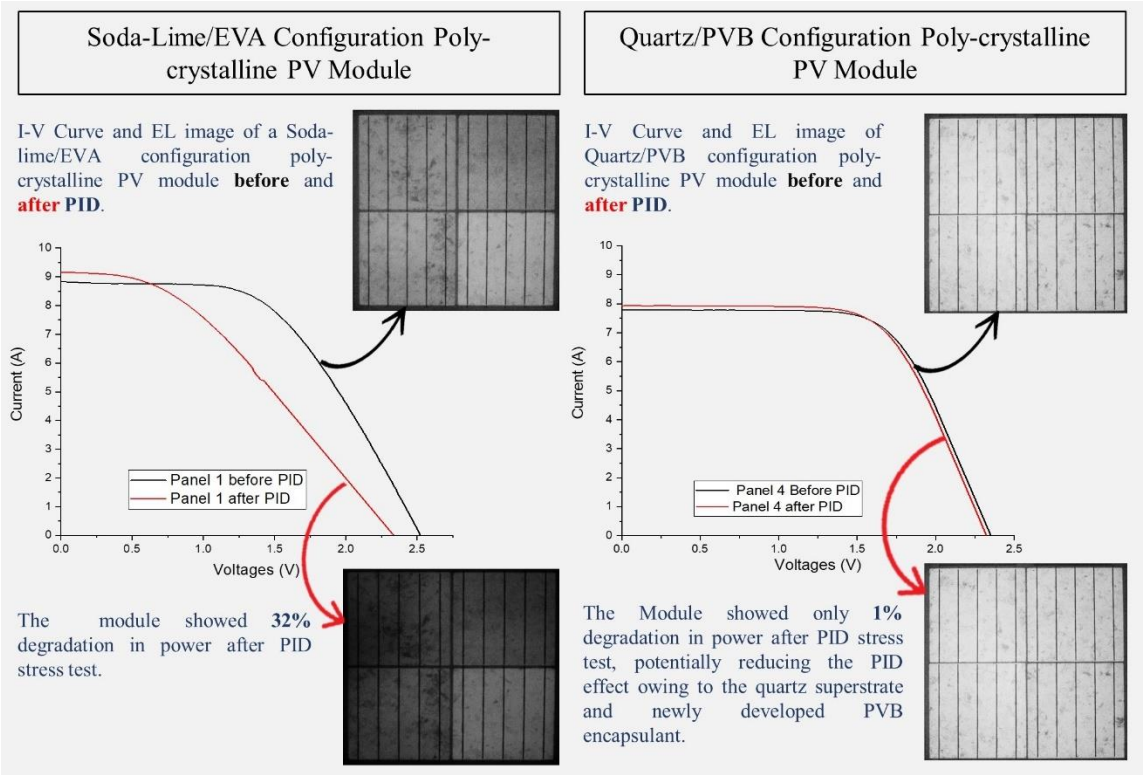
# Appendix-1 Research Article

## Graphical Representation



# Experimental Investigation of Potential Induced Degradation of Poly-crystalline Photovoltaic Modules: Influence of Superstrate and Encapsulant Types

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## Abstract

Potential induced degradation (PID) is amongst the most critical degradation phenomena affecting the reliability of photovoltaic solar modules by causing power losses up to 30% on the system level. In this research, PID is induced on poly-crystalline modules in an environmental chamber in accelerated temperature and humidity conditions under the application of high voltage stress to investigate the degradation phenomenon. The primary focus of this paper is to quantify the degradation extent of photovoltaic (PV) modules with different encapsulant and superstrate/glass types. The encapsulant types investigated in this work are Ethylene-vinyl acetate (EVA) and newly developed Polyvinyl butyral (PVB). The superstrate/front glass types investigated are Soda-lime glass and Quartz. The progression and severity of degradation were determined through Current-Voltage measurements and Electroluminescence imaging, revealing losses in Maximum power and Fill-factor. The leakage current was measured during the entire PID test and no correlation between leakage current and power was observed. It was demonstrated that the PID loss is strongly depending on the electrical and physical properties of the superstrate and encapsulant types. The module with Quartz/EVA configuration experienced lower (17%) PID losses compared to the Soda-lime/EVA module (32%). Similarly, the module with Soda-lime /PVB configuration experienced lower (10%) PID losses compared to the Soda-lime/EVA module (32%). While the module having both the quartz superstrate and PVB encapsulant, experienced the lowest PID with % degradation in power up to only 1%. The extent of degradation is explained based on the electrical and ionic conductivities of the superstrate and the encapsulant.

### *Keywords*

Electroluminescence (EL) Imaging, Encapsulation, Maximum Power Determination, Poly-crystalline Silicon Solar Modules, Potential Induced Degradation (PID).