# PHASE LOCKED LOOP

## Project Report

National University of Sciences and Technology (NUST), Islamabad, Pakistan

Muhammad Khubaib-ul-Hassan Khan 2009-NUST-BE-EL-62
Ahmed Waheed 2009-NUST-BE-BICSE- 143

*Project Title: "Analog Phase Locked Loop"*

*Name of group members:*

*Khubaib Khan* *2009-NUST-BE-EL-62*
*Signature:* _____

*Ahmed Waheed* *2009-NUST-BE-BICSE-143*
*Signature:* _____

*Project Co-advisor: Dr. Arsalan Javaid*

*Signature:* _____

*Project Advisor: Dr. AwaisKamboh*

*Signature:* _____

National University of Sciences and Technology

## *Acknowledgements*

*It is essential to remember the contributions of following persons and entities which helped us throughout the year. Sir Waseem for helping a great deal us in the project. Sir Sami for helping us out in the layout process. Last but not least to Open Silicon Pakistan now Silicon Design Solutions for providing us with the opportunity to work with industry experts.*


***Dedicated to our families…..***

# Table of Contents

# List of Figures

# INTRODUCTION:

A phase locked loop is a control system that generates an output signal whose phase is related to the phase of an input "reference" signal. It's circuit consists of a variable frequency oscillator and a phase detector primarily. This circuit compares the phase of the input signal with the phase of the signal derived from its output oscillator to keep the phase matched. This signal from the phase detector is used to control the oscillator in a feedback loop.

Phase locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to recover a signal from a noisy communication channel, generate stable frequencies at a multiple of an input frequency (frequency synthesis), or distribute clock timing pulses in digital logic designs such as microprocessors.

# Initial Literature review:

Before the start of practical application of any device, method or technique it is necessary that you have a strong back ground about each and every root of your project. The importance of literature review that our group did in the initial stages is evident and obvious and this stage forms an inevitable foundation for this project. Our Literature Review can be broken down into two sub parts:

- **PROJECT DOMAIN DOWNSIZING**
- **REALIZATION OF PLL**

## PROJECT DOMAIN DOWNSIZING:

In the start we searched for viable and feasible options to implement. A few things were clear that our project has to be the implementation of an ASIC device or any sub-part performing a specific function in that device. Among the vast field of Analog CMOS Designing we shortlisted two potential projects for ourselves. They were:

- Design of High Speed Mixed Signal Input Output Circuit for Chips (I/O BUFFERS)
- Design of a Phase Locked Loop Circuit.

Both of these circuits are extensively used as sub parts of a lot of ASIC devices. Mixed Signal I/Os are a part of every chip. During our familiarization with IOs we looked superficially over different techniques used to build IOs like Current Mode IOs, Voltage Mode IOs, Differential Mode IOs and Pseudo-Differential IOs. Also we reviewed techniques used for prevention of ESD, and reviewed Latch Up problems also to gain a deep insight about the subject.

Along with IOs, we in parallel gained the knowledge about the devices and methods used to remove skew (phase difference b/w two signals) or the devices which are used to synchronize two signals. In this venture we came across devices like PLL and DLL. Both of these techniques are the subject of intense research and have a vast range of applications.

Also in project domain downsizing we finalized the technology file we would be using and that is 500nm. We opted for 500nm because there are less second order effects to deal with and it is easily available at the labs in our institution.

## REALIZATION OF PLL:

After detail discussion and a series of presentations we along with our advisors and mentors decided to take PLL as the title of our Final Year Project. Now the next step was to gain a brief insight about the working and types of devices used for this particular function (i.e. to reduce skew and phase locking). The first question that we asked to ourselves was WHY should we implement PLL?, what applications can such devices offer us. In the pursuit of it's answer we came across issues such as unwanted delay which a signal encounters during inter and intra chip transmission. Devices used to implement Phase Locking offer us a wide range of applications such as Frequency Synthesizing, Clock Generation, De-Skewing, Clock Distribution (with a particular phase difference).

Now the next question was how many ways are there to implement phase locking?. There are mainly two methods:

- Analog Phase Locked Loops.
- All Digital Phase Locked Loops.
- Delay Locked Loops.

An Analog Phase Locked Loop is called so because of the nature of the frequency generating block inside it which is purely based on analog parts. In an All-Digital Phase Locked Loop the Frequency generating block is totally digital, also other blocks are formed on the basis of interpreting digital logic. A Delay Locked Loop is different in the

nature that it doesn't possess a frequency generating block at all and performs de-skewing with a delay line.

We downsized our project to a much greater extent and choose to implement an Analog Phase Locked Loop. Our choice was purely dictated by our interest in dealing and learning more about analog designing. The next step was to develop block level and intuitive understanding of the device. An analog PLL is composed of following parts:

- Phase Frequency Detector.
- Charge Pump.
- Loop Filter.
- Analog Voltage Controlled Oscillator.
- Fractional N (Frequency Divider).

## ANALOG CONCEPTS:

In order to implement something like a phase locked loop it is essential that you are fully armed with the all the technical basics and knowledge. So it was necessary to initiate a thread of Analog Concepts under the umbrella of which we were to revise certain concepts which were form a fundamental of our project. The concepts that we revisited and some that we learned freshly were:

- Current Mirror.
- Small Signal Models.
- Inverter.
- Wiring Concepts.

The Current Mirror is a very fundamental concept. This technique is extensively used as a biasing circuitry and is preferred because of its resilience against certain parameters which can vary with temperature like Threshold voltage because the current only depends on Width to Length ratio and input current, not on threshold voltage and mobility. Small Signal Models were also revised of basic elementary amplifier stages of MOS, which include Common Drain, Common Source and Common Gate.

Inverters are a very basic part of many Analog Integrated Circuits. This concept was also revised, topics like Noise Margin, threshold Voltage, Power Dissipation in Static and Dynamic Modes were studied in detail. Wiring Concepts were also necessary to give a review, because they introduce delays due to their capacitances. Different models which are used to estimate the Resistance and capacitance introduced by interconnecting wires were studied.

Books like Behzad Razavi and Johan Rabaey were usually used as touch stones while gaining insight of these concepts.

## ARCHITECTURE REVIEW OF PLL:

After building the necessary concepts required for designing and completing the intuitive level understanding of the PLL system, we moved our literature review towards the sub blocks of PLL. As explained above PLL consists of four blocks namely Phase Frequency Detector, Charge Pump with low pass filter, Voltage Controlled Oscillators and a Frequency Divider.

## PHASE FREQUENCY DETECTOR:

A phase frequency detector (PFD), in electronics, is a device which compares the phase of two input signals. It has two inputs which correspond to two different input signals, usually one from a voltage-controlled oscillator (VCO) and another from some external source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase.

To form a Phase-locked loop (PLL) the PFD phase error output is fed to a loop filter which integrates the signal to smooth it. This smoothed signal is fed to a voltage-controlled oscillator which generates an output signal with a frequency that is proportional to the input voltage. The VCO output is also fed back to the PFD to form the PLL circuit.

The PFD is an improvement over the phase comparators of early PLLs in that it also provides a frequency error output as well as a phase error signal. Phase detectors for phase-locked loop circuits may be classified in two types Type I detector is designed to be driven by analog signals Type II detector is sensitive only to the relative timing of the edges of the input and reference pulses. The actual input signals to the phase detector, however are not $\alpha$ and $\beta$, but rather sinusoids such as $\sin(\alpha)$ and $\cos(\beta)$. There are 3 basic types of PFD's depending upon the type of PLL

1. Analog phase detector
2. Digital phase detector
3. Phase-frequency detector

At times a delay element whose duration is $\tau$ seconds is used to prevent dead zone. Dead zone is a main property in the PFD phase characteristics as it introduces jitter to the PLL system. The PFD doesn't detect the phase error when it is within the dead zone region, then PLL locks to a wrong phase

## CHARGE PUMP:

Charge Pump takes two inputs from the Phase Frequency Detector. It consists of two current sources connected in series with two voltage controlled switches. This combination of current sources and switches charges and discharges the capacitor for a time span decided by the PFD.

The charge pump is a very crucial part of PLL. The values of current and the capacitance of charge pump decides the locking or stability time of the Phase locked loop. The filter attached in front of the charge pump can be an active filter and a passive filter. In the passive filter domain the filter can be of order one, two,three and so on. To keep the things simple and keeping the fact in mind that stabilizing a higher order loop filter is dificult so we opted for a first order loop filter. There is also a resistor in between the charge pump and filter capacitor which along with the capacitor determines the loop bandwidth.

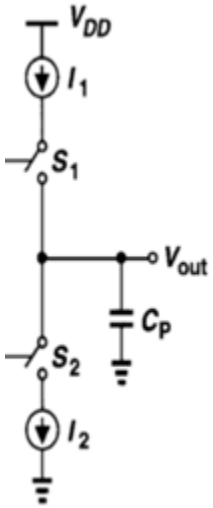



**Figure 1 Intuitive Understanding of Charge Pump**

## VOLTAGE CONTROLLED OSCILLATOR:

A VCO is the heart of any PLL because it generates the signal which is then brought in accordance with the incoming reference signal and then skew is reduced. A VCO can be of different types. Oscillators are basically of two types a) Harmonic Oscillators, b) Relaxation Oscillators. Harmonic Oscillators are mostly used in RF and antenna applications because of their temperature resistance and high power applications but are difficult to implement on integrated chips. While relaxation oscillators are based on CMOS technology and can be tuned over a wide range of frequency. One of the most famous types of relaxation oscillators is a ring oscillator in which a chain of inverters are connected back to itself to produce a complementing signal whose frequency is controlled by the delay of each delay element which is inverter.

There are many topologies of implementing a VCO. In some topologies designers exploit the fact that delay depends on Capacitance, some on the fact that it also depends on output resistance and some on the fact that it depends on the current that is used to fill the output capacitor. We decided to go with the topology which offers us control over the current flowing through each delay element. So we opted for a Current Starved VCO.

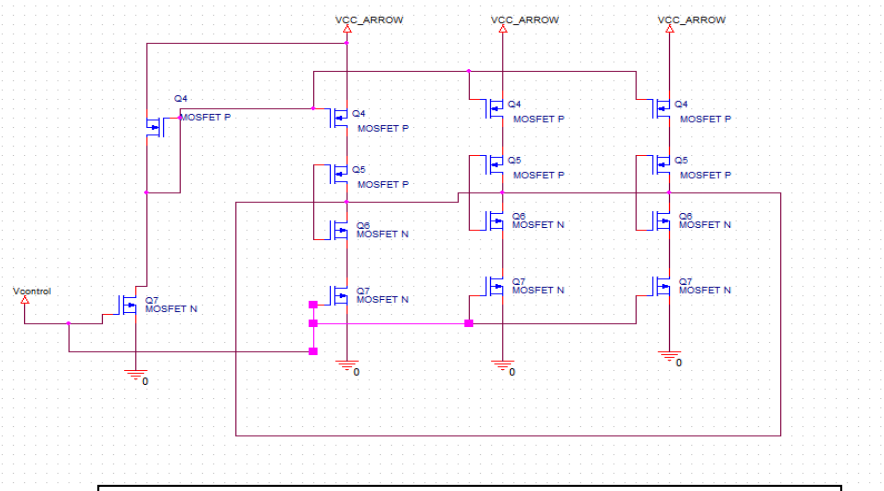



**Figure 2 Current Starved Voltage Controlled Oscillator**

The Vcontrol Voltage controls the current which is mirrored into every stage of the inverter and thus the current in every element is controlled through the voltage at the beginning. The current controlling MOSfets operate in the saturation region and plays a major part in the output resistance while the inverter MOSes operate in triode region which have negligible resistance.

## FREQUENCY DIVIDER:

A frequency divider's major function is to divide the frequency and its an essential part if you require your PLL to be used as a frequency synthesizer. A frequency Divider consists of a series of Flip Flops connected in different fashions. Mentioned in the figure is D flip flop when connected in such fashion divides the input signal frequency by 2 and gives the output. If a divide by four circuits is intentioned, then two flip flops manipulated in such a manner are connected in series, if divide by 8 is desired, three flip flops will be connected in series and so on. The divide by two functionality is implemented by exploiting the characteristic of D flip flop which is to pick the data up on the positive edge of the signal only.

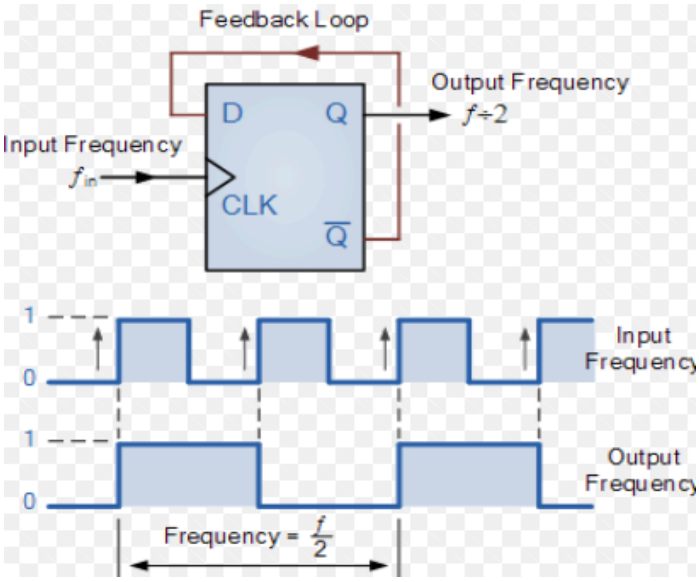



**Figure 3 Frequency Divider Basic Operation**

# DESIGN METHODOLOGY & DISCUSSION:

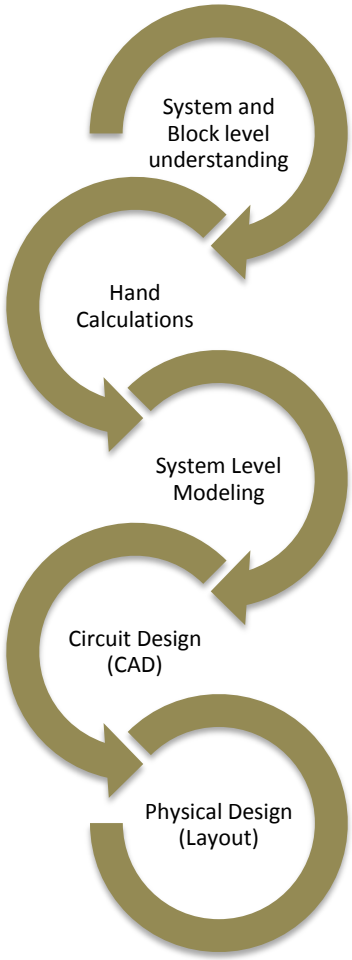



**Figure 4 Top Design Methodology Applied**

## SYSTEM LEVEL DESIGN:

After the detail understanding of what each part's function was it was now time to start the practical work and we started with system level modeling, which uses ideal models of the blocks, and gives us a superficial overview of how our system's outcomes would be for certain set of parameters. System level Modeling is not only there to be a formal part of Top-down design methodology, it offers us the flexibility to adjust certain parameters and view the outcomes, by doing so we can focus and come close in deciding the specifications of our system.

We performed system level modeling on the following two tools:

- Matlab.

- Cadence.

## MATLAB:

We started our system level modeling on Matlab Simulink. We used ideal function blocks like flip flops and nand gates to model PFD, a continuous time Ideal & linear Voltage Controlled Oscillator, a combination of resistance and a battery to produce our require current required to charge and discharge the filter. This is a snapshot of the system level modeling on Matlab.

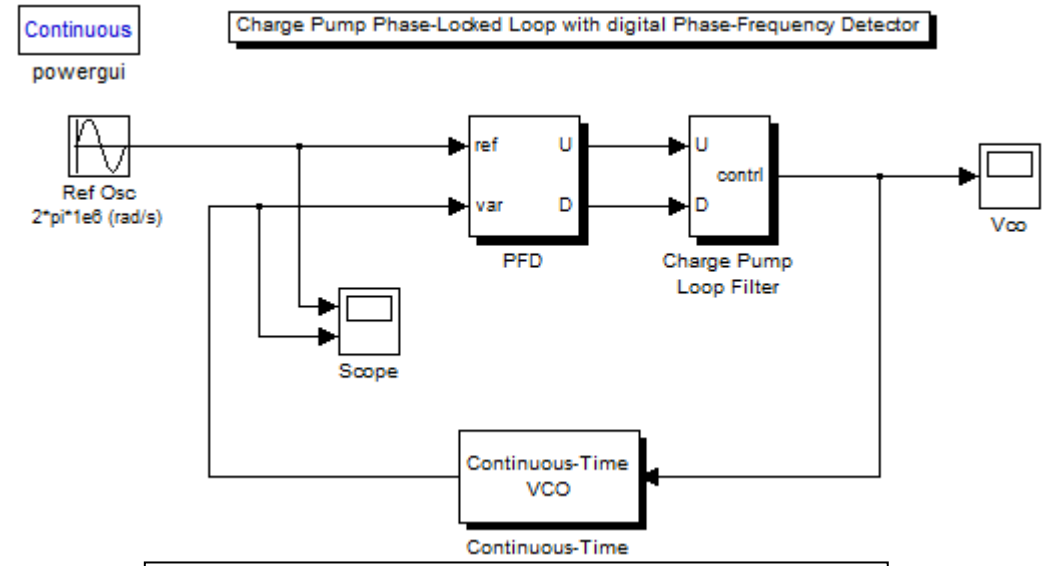



**Figure 5 Matlab Simulink Diagram**

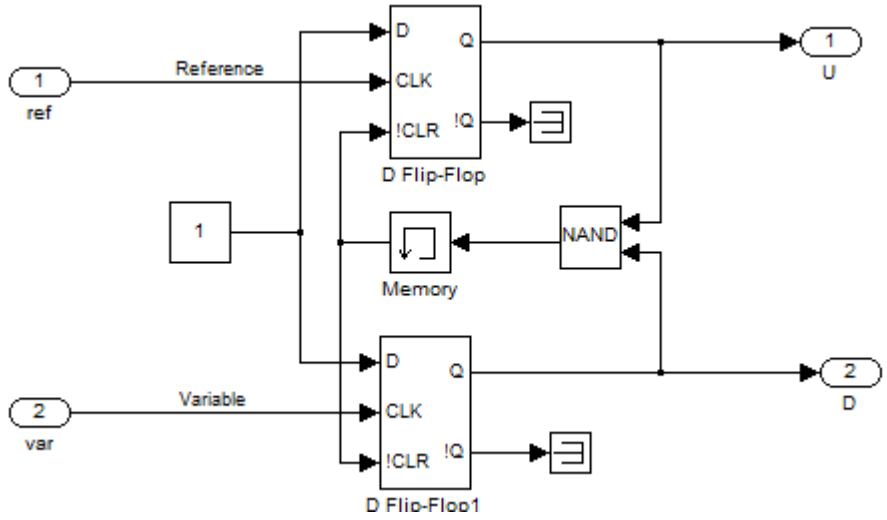



**Figure 6 Phase Frequency Detector in Matlab**

While using Simulink we faced different problems due to which it became difficult to model important parameters on Simulink. The first problem was that it was not possible to model a voltage controlled current source in Simulink because of the compatibility issues of blocks belonging to different sub libraries of Simulink. Due to this problem it was almost impossible for us to ensure a constant flow of current at any voltage.

The results from Simulink although were not very close to our assumptions that we made in our calculations, but still it gave us results and showed us that the system responds and converges to a single point and locks for the frequency at which we want it to run on. Also through this step a lot of issues such as system stability, loop dynamics, Gain of each block, and compatibility of filter with the VCO's Sensitivity were cleared.

### The Problem With Matlab Model:

a) The compatibility of blocks belonging to different libraries.

b) The ineffective model of charge pump.

Compatibility of different blocks with each other was a very critical issue. As most of the blocks belonged to Sim Library of MATLAB and some blocks like Continuos time VCO belonged to SimPower Library. So Matlab never allowed connections in between these two blocks.

Due to the above problem we were unable to connect a an ideal current source to a capacitor via switch because the ideal current source and switch will not connect. Due to which we had to take an alternative path to model the current source. Which was to connect a battery with a resistor and set their values so that according to the formula V=IR, that it releases our required current. Below shown in the figure is the diagram of the charge pump we modeled.

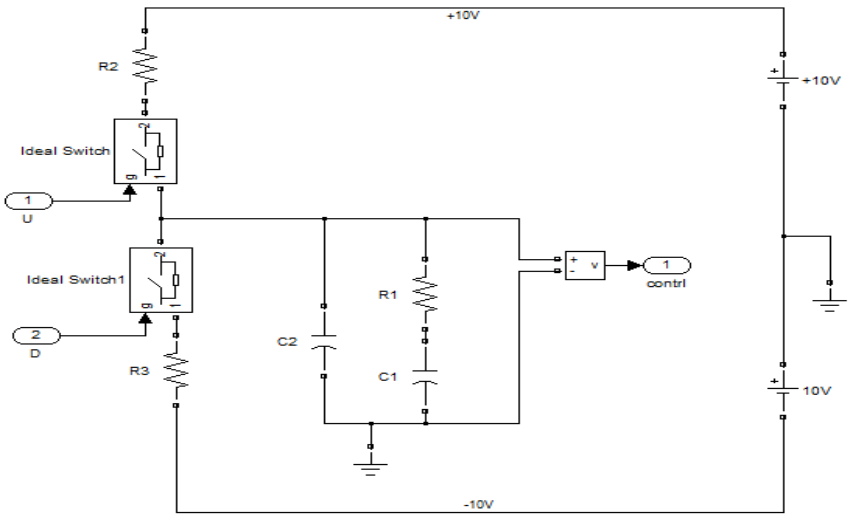



**Figure 7 Charge Pump in Matlab.**

This model was very ineffective because we weren't able to control our current of the charge pump, and it was controlled by the total impedance. The presence of an Ideal Current Source for this modeling was inevitable so that we could exactly formulate the value of our capacitance of charge pump. Such an ideal model could ensure us and give us the space to play and experiment with different value of of capacitor while we are sure and not worried by the fact that the current coming into the capacitor of the charge pump will also change with it.

## Learning Points:

Although the we weren't able to exactly define our specifications from the matlab model but it played an important part in giving us the understanding about the Loop dynamics of the system. We simulated the system for different values of capacitor and obtained the following results. The figure shown are that of two extremes, we swept the capacitor between 4pf and 400pf. The graphs of two extreme (ie 4pf and 400pf respectively) are shown and rest of the things will be mentioned in text. The graph shows Voltage at the input of the VCO wrt to time.

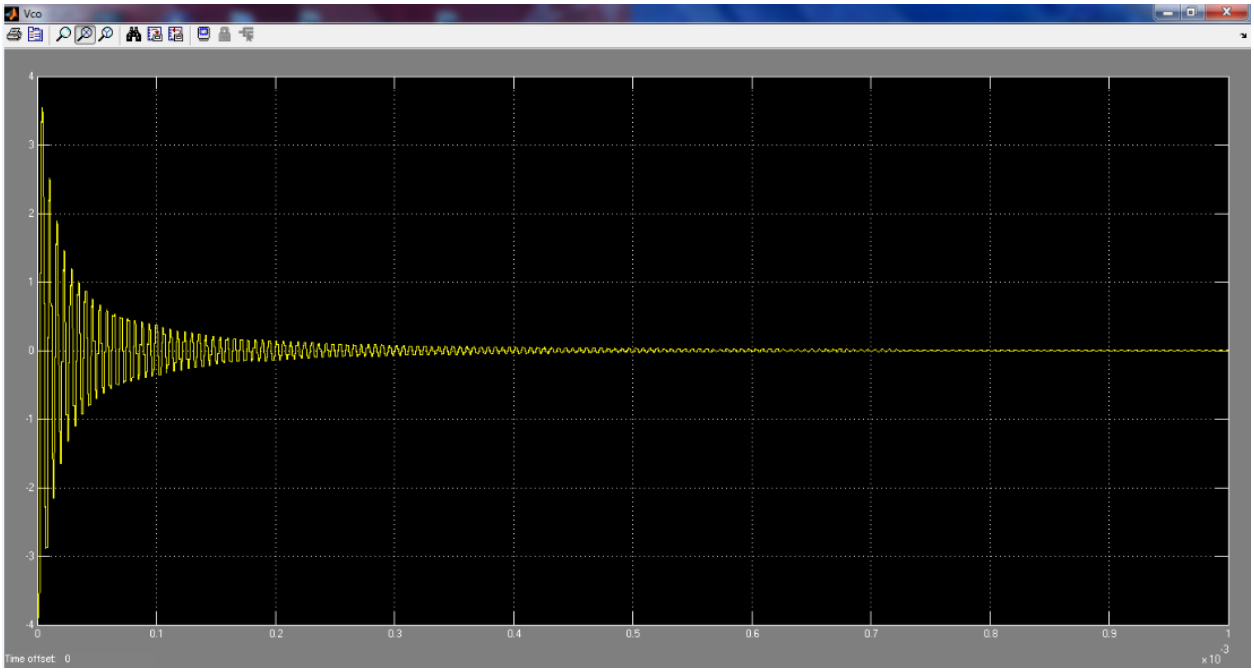



**Figure 8 System Responses with 4pf Capacitor.**

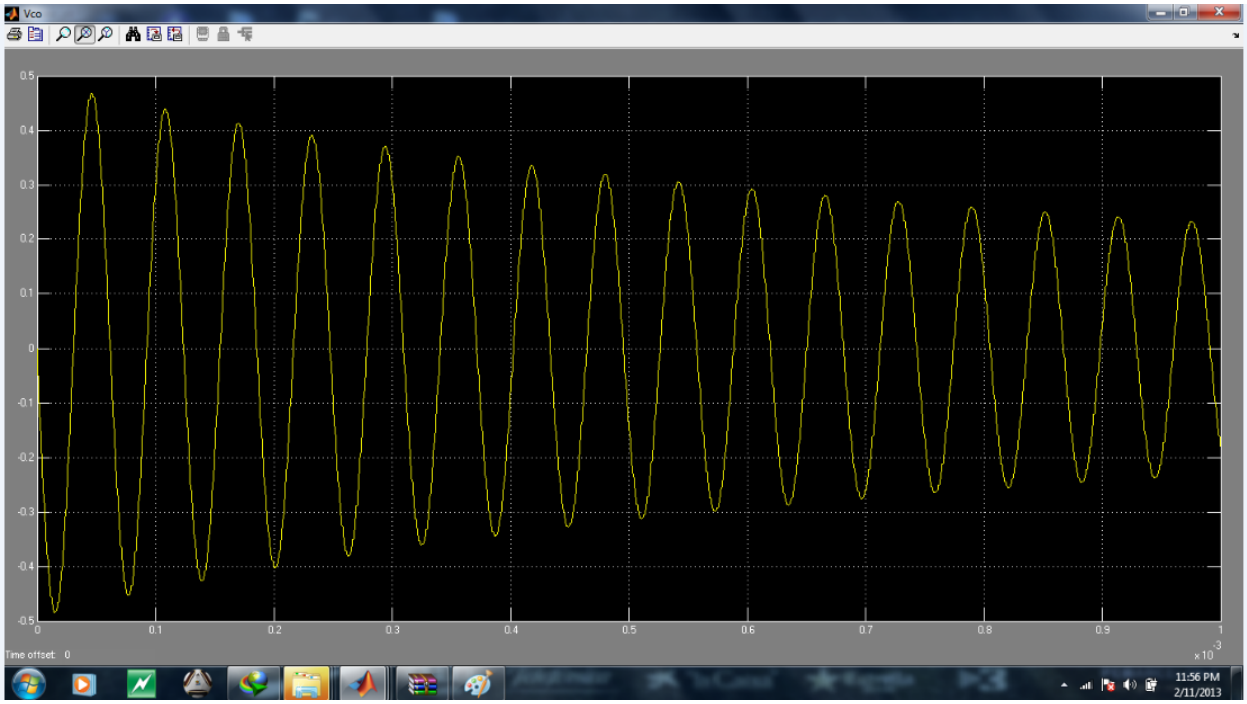



**Figure 9 System Response with 400pf capacitor.**

We can conclude this behavior by saying that if the capacitor's value is low loop stabilizes quickly, BW is high, settling time and lock time both are less but as we increase the value of capacitor the loop stabilizing time increases so as the lock time and BW decreases. The response for less capacitor values is highly under damped and that for high capacitor values it goes towards un-damped. There is a particular value in between this boundary for a critical damping which is our required value. For very low capacitor values the system goes to be in negative damping and sometimes never stabilizes.

## CADENCE:

In order to bring our system level modeling closer to our assumptions that we made in our hand calculations we decided to jump to cadence. In cadence we used the library of ahdlLib extensively in our system level modeling. PFD was modeled with a freq_phase_detector, VCO was modeled with a dig_vco both of them from the telecom section of ahdlLib of Cadence. Charge Pump was modeled through Voltage Controlled Current Sources. Fractional N block was modeled with D Flip Flops. A view of the schematic of system level model is as follows:

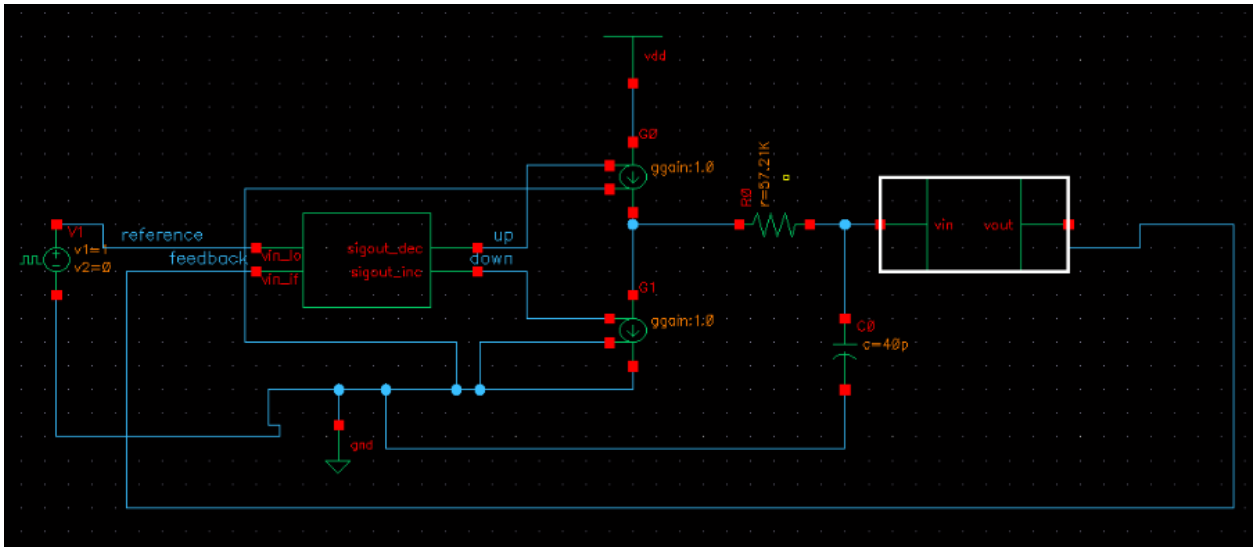



**Figure 10 System Diagram in Cadence.**

## VCO PROBLEM:

As shown in the figure the current and switch both were modeled by the use of a voltage controlled current source which give us a specified amount of current at high logic and 0 current at low logic. The modeling of VCO was a bit complex. A VCO has two crucial parameters at system level which are center frequency and VCO gain. We assumed while doing the hand calculations that VCO's gain is the the amount of frequency range a VCO can generate per volt and VCO center frequency will be the frequency of our reference frequency that is the frequency at which we want to lock our system. But the Dig VCO given in cadence had different interpretations of the latter term. The understanding of which was obtained by simulating VCO in an isolated environment. It gave us such a response:

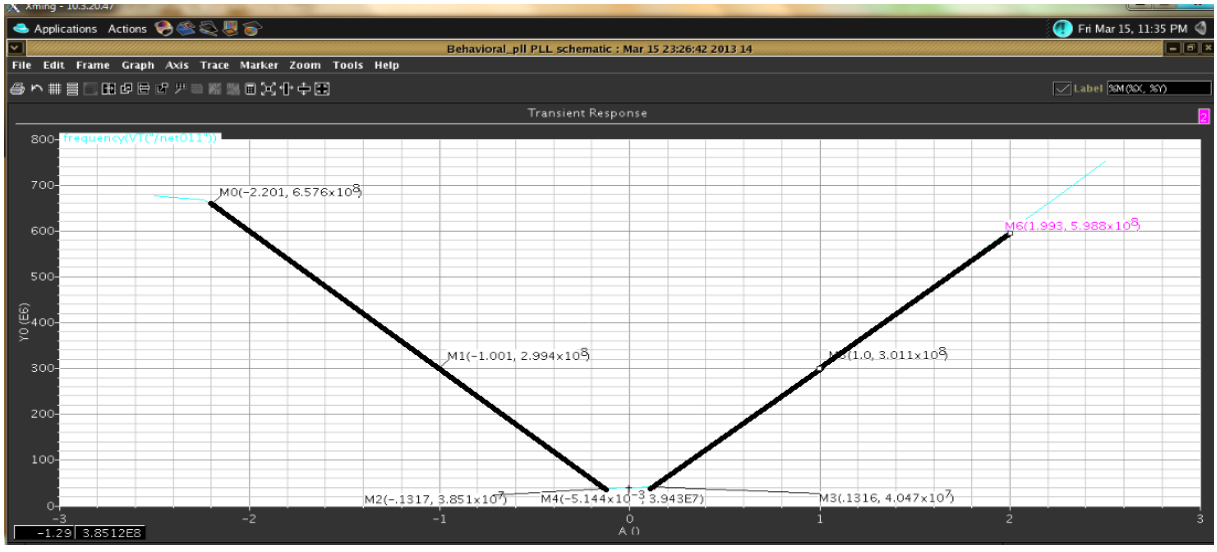



**Figure 11 Ideal VCO block response.**

As we can see from the model that the VCO is linear and the center frequency is just an amount of frequency which is added at every point. So in order to bring this VCO in accordance with the voltage range that we calculated a formula was developed:

Center Frequency = VCO GAIN – (VCO GAIN –(VCO GAIN*(1- center_voltage)))

Where center_voltage is the voltage at which we want our VCO to generate the frequency of reference signal or you can call it Locking Voltage.

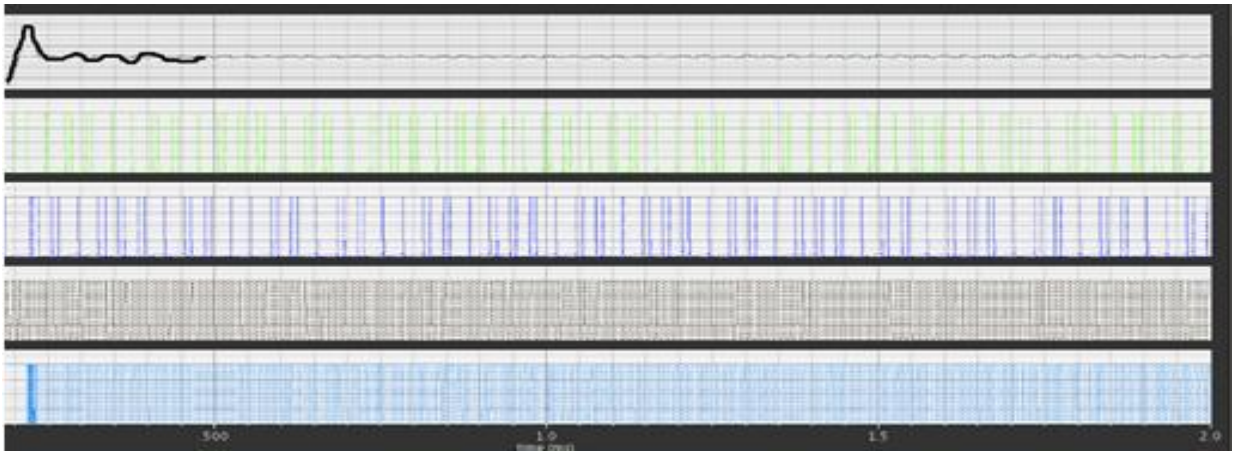


**Figure 12 Cadence Behavioral Modeling Response.**

## FREQUENCY DIVIDER PROBLEM:

The problem with this circuit is that it does divides the input frequency by 2 but it gives the output at neg edge due to which there is a constant phase difference of 90 degrees and the loop never stabilizes. So we used an alternative for that as shown in the figure. The divide by 4 circuit spec was chosen because the technology VCO has its limitations in stability. If we create a divide by 8 circuit the circuit stabilizes but the glitches are very large as in milli volts. And if circuits above than divide by 8 the VCO doesn't generate the frequency in a square waveform shape but does that in a saw tooth or triangular manner. The frequency divider circuit that we followed first is given in the figure:

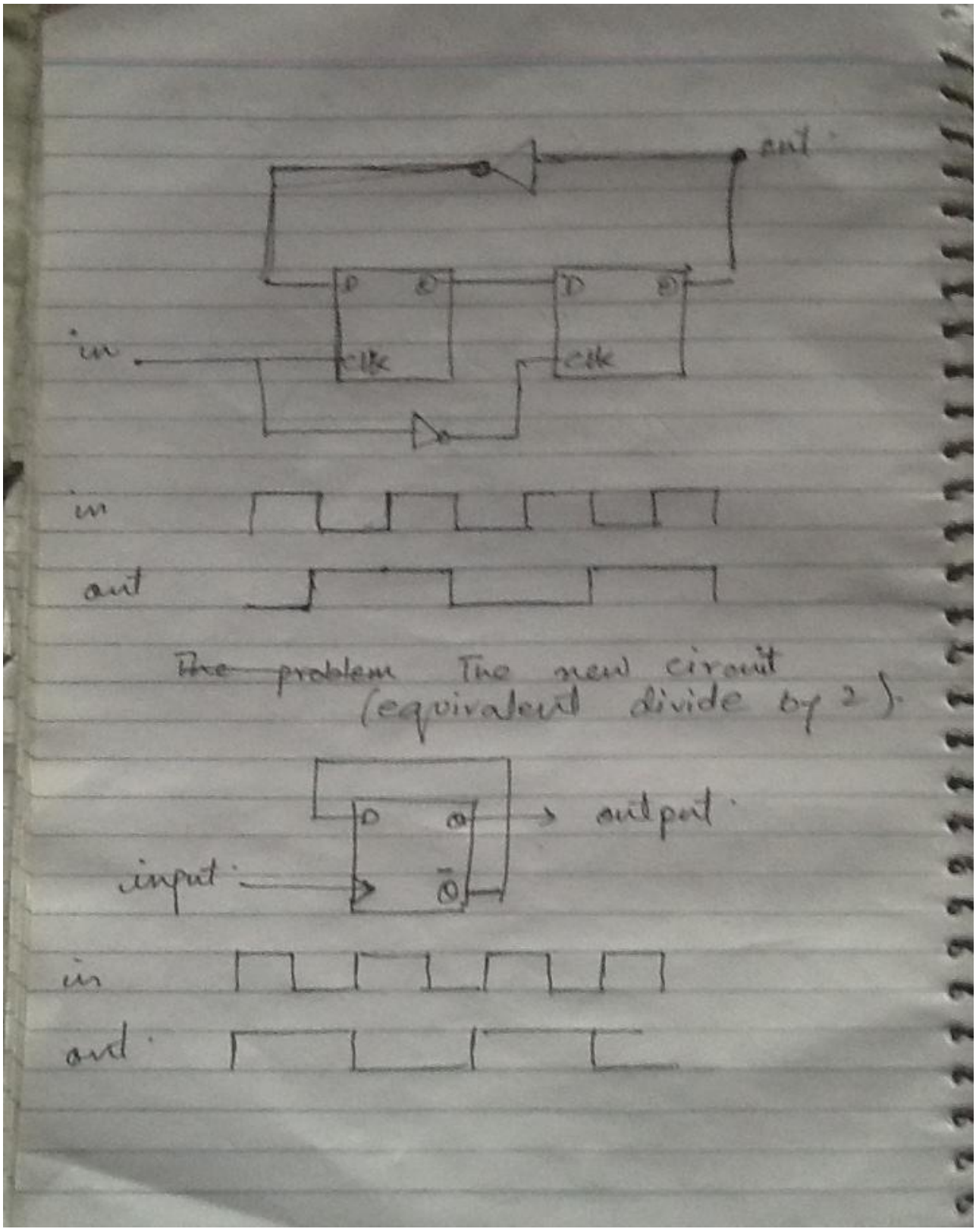



**Figure 13 Frequency Divider Problem.**

## OPTIMIZING GAP B/W HAND CALCULATIONS & SYSTEM MODEL:

Hand Calculations were performed in detail to sort out the W/Ls of each and every Mosfet in the VCO and also to calculate the Charge Pump value of Capacitor and resistor. The technology file that we used was that of ami06 BSIM3V1 Level-49 HSpice which is shown in the figure below:

Some Assumptions were made before doing hand calculations they were:

- Our VDD is 2.5V and while sizing the current sources of our VCO architecture in order to make sure that they are in the saturation region always we have to keep their Vov=0.25V.
- While sizing the mosfets of inverters we have to make sure they act in triode region so we will force their Vds to be 10mV.
- Frequency range is 1Mhz to 15Mhz with System locking at 8Mhz, current rage will be derived from this frequency demand which will indirectly determine our voltage range of the VCO.
- For charge pumps we assumed our current to be 2uA and the capacitor's value will be calculated by I=CV/t. And the value of resistor will be dictated by the cut off frequency of our filter which in this case should be 8Mhz.
- The PFD can detect at max 62.5ns that is the half of 8Mhz inverse.

The hand Calculations done are as follows the conclusions are these details are given in the APPENDIX A:

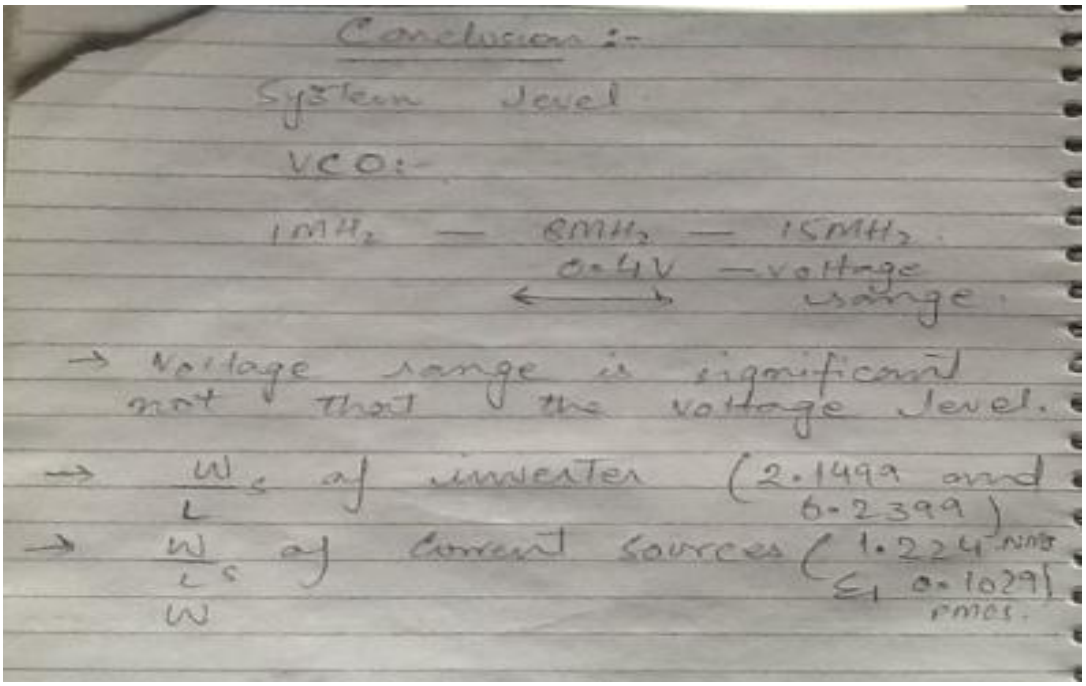



**Figure 14 Hand Calculation Results.**

When our calculations were done the next step was to bring the calculations and system level modeling in accordance. But at the start the system level model was stable and locking and working properly but the readings were differing from what we anticipated. Mainly there were two reasons:

- The model of VCO in CADENCE is a linear one which means that relation b/w Voltage and Frequency is linear but in actual it should be square law.
- The current source used here is purely ideal due to which no matter how large the resistance of Loop Filter, the dynamics of loop filters will remain unaffected and independent of the value of resistance.
- The value of capacitor calculated by us using a technique which involves Q=CV/t has some drawbacks.

To the answer of our first question we decided to approximate our voltage range in such a manner that it abides square law. So we decided the voltage range should be 0.x Volts if the frequency range is x^2Mhz. Moreover as described above the VCO was settled such that it generates frequencies at voltages we anticipate.

Now addressing the second point. The value of resistor when changed it never affected the readings that much for one main reason that is because eof the presence of an ideal source the value of current is not limited or affected by high value of resistors. So thus we have to leave the tuning of resistor value to circuit level stage.

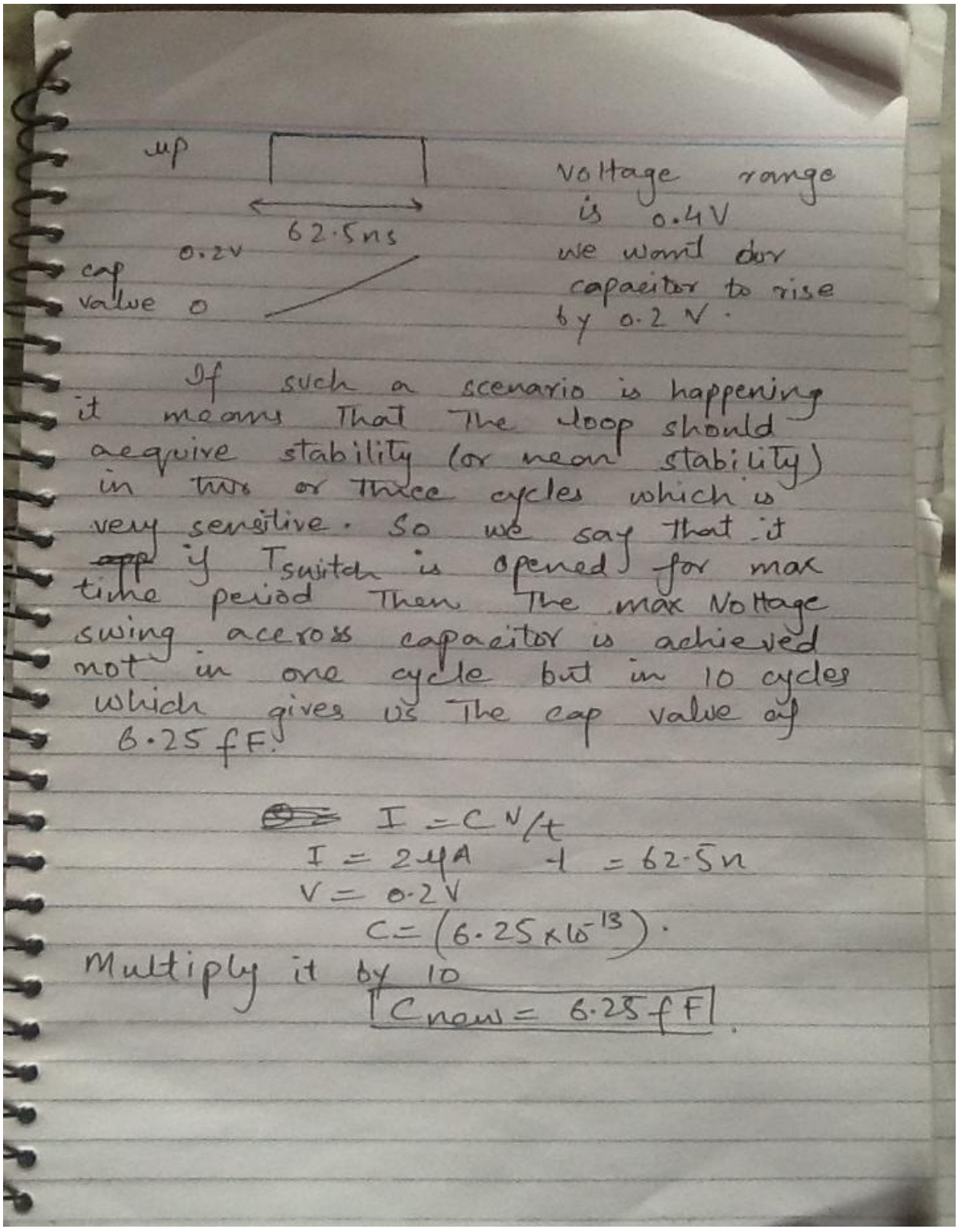


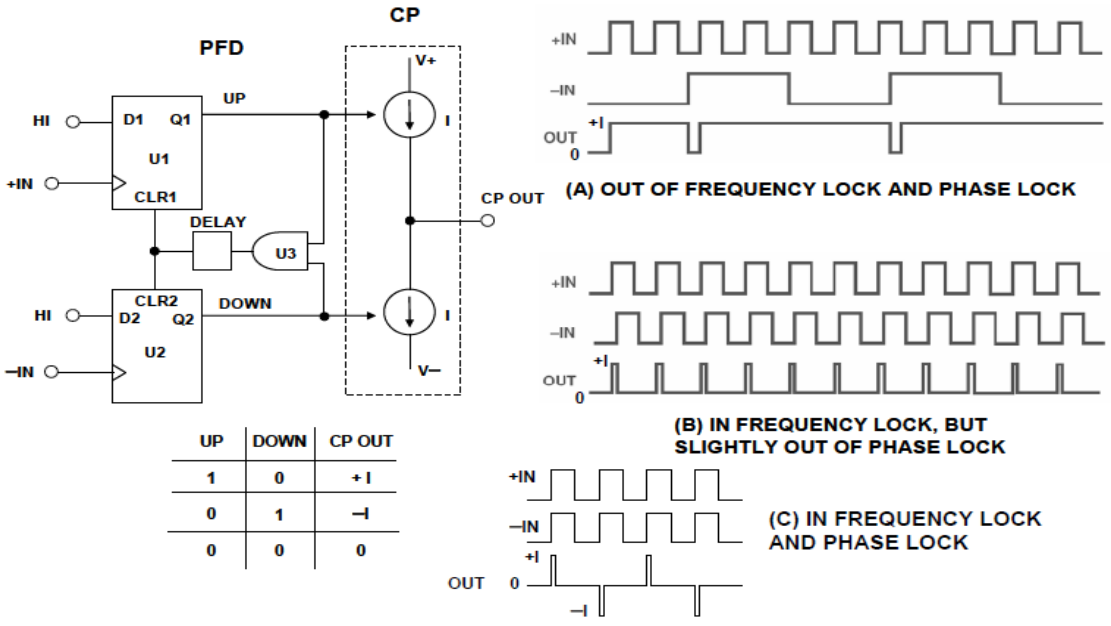

**Figure 15 Hand Calculations for Loop Filter.**

So we cannot exactly define the value of capacitor's value by this because this is making our system very sensitive. What we expected was that such a voltage range is not acquired in one cycle but in several cycles lets say in 10 steps. This assumption is more formidable and makes our system able to work when we incorporate the divider, because when we incorporate the divider our circuit will work on higher voltages and lesser value of capacitance at that point will create difficulties for us.

## CIRCUIT DESIGN:

### PHASE FREQUENCY DETECTOR:

The figure below shows a popular implementation of a phase frequency detector. It consists of 2 d flip flops and 1 and gate. 1 output of the flip flop enables the positive current source while the other output enables the negative current source. The D flip flops are positive edge triggered in the below design and their corresponding possible states are also shown.

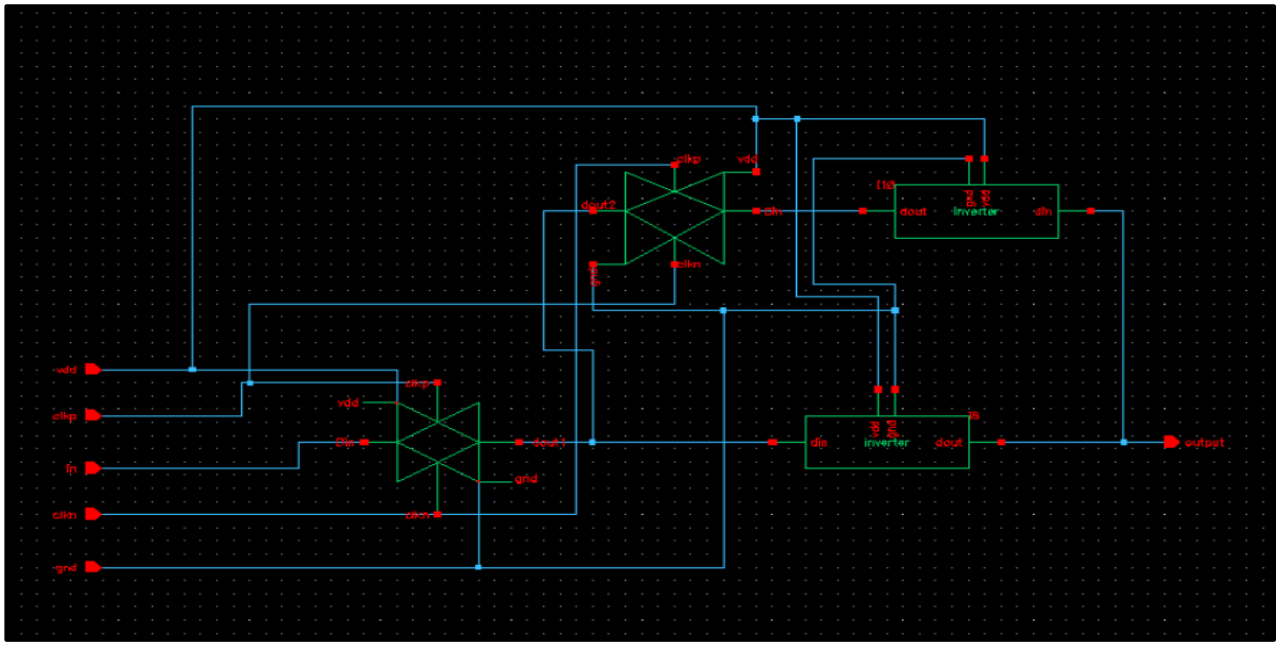



| UP | DOWN | CP OUT |
|---|---|---|
| 1 | 0 | +I |
| 0 | 1 | –I |
| 0 | 0 | 0 |

**Figure 16 Phase Frequency Detector Working.**

The approach used was bottom up in designing the PFD in cadence simulating environment. Starting from on paper hand calculation and later transferring it onto the tool. It all started from the basic building blocks of the flip flop, transmission gate and inverter.

The flip flops were chosen to be transmission gate based because of their smaller size and high speed over other designs. The first step was to build a latch using 2 transmission gates and 2 inverters. Later 2 latches were combined together to make 1 edge triggered D flip flop. A major error faced during this phase was the clock feed through and charge injunction. This was later eliminated by correctly sizing the MOSFETs at each stage.




The table below shows the sizes and other designing parameters of the MOSFETs used

### TXT GATE

| | PMOS | NMOS |
|---|---|---|
| **Width** | 9u | 3u |
| **Length** | 600n | 600n |
| **Cgs** | 6.85f | 1.95f |
| **Cgd** | 475a | 2.37f |
| **Ron** | 1.4k | 2k |
| **RC** | 9.6p | 3.9p |

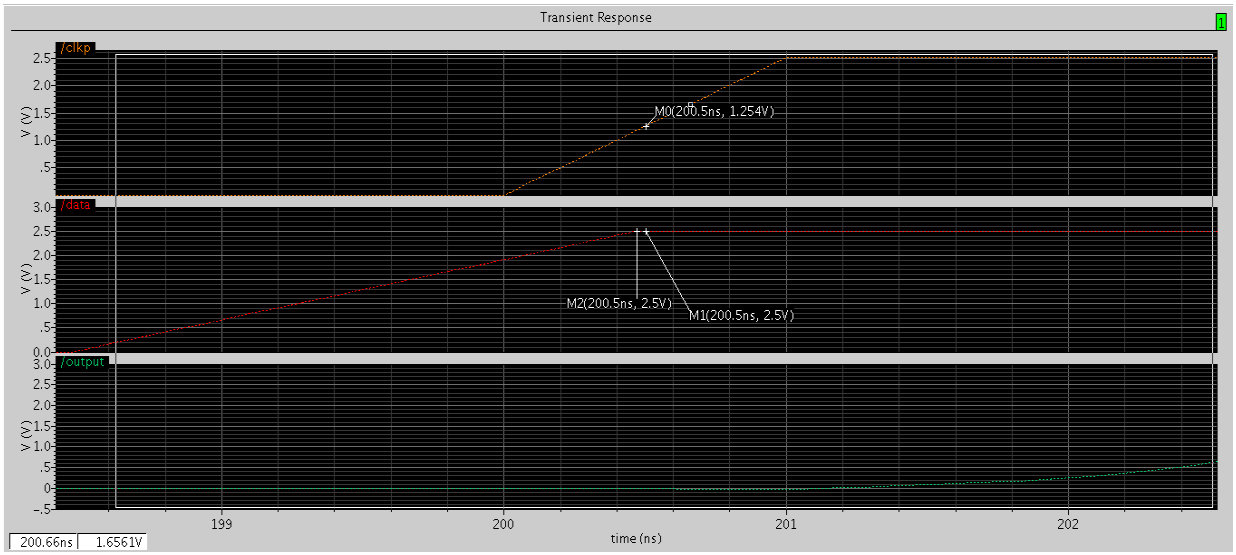
### Inverter

| | PMOS | NMOS |
|---|---|---|
| **Width** | 3u | 1.5u |
| **Length** | 600n | 600n |
| **Cgs** | 2f | 921a |
| **Cgd** | 2.2f | 997a |
| **Ron** | 4.7k | 4.9k |
| **RC** | 9.4p | 4.5k |

After the flip flop was designed and successfully run the next step was to find setup time and clock to q delay. This was found by using a number of iterations and the results were as under

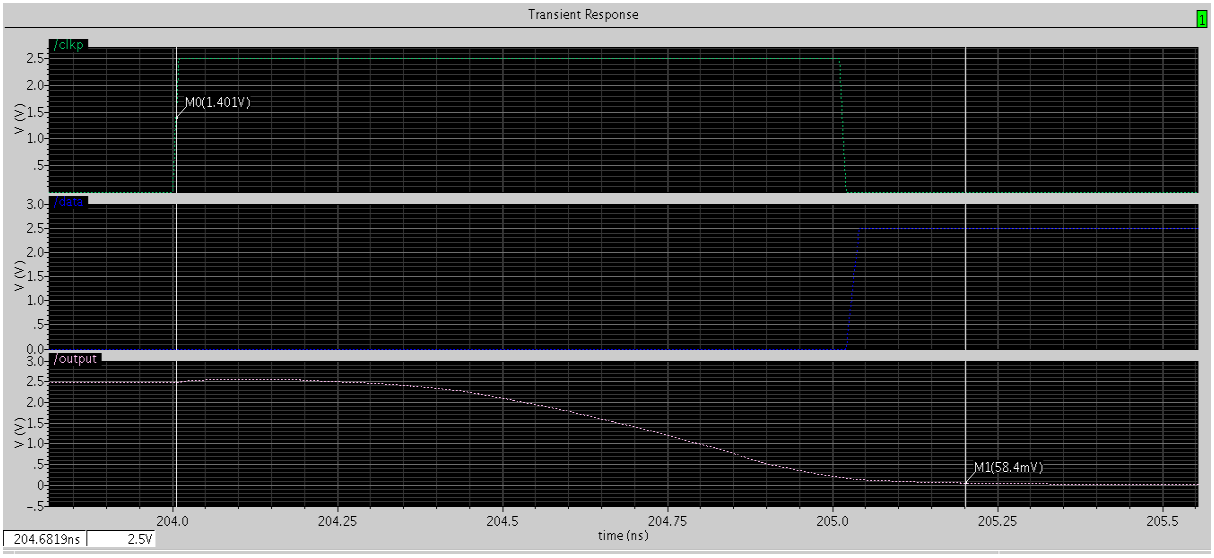
## Setup time

31.6p sec



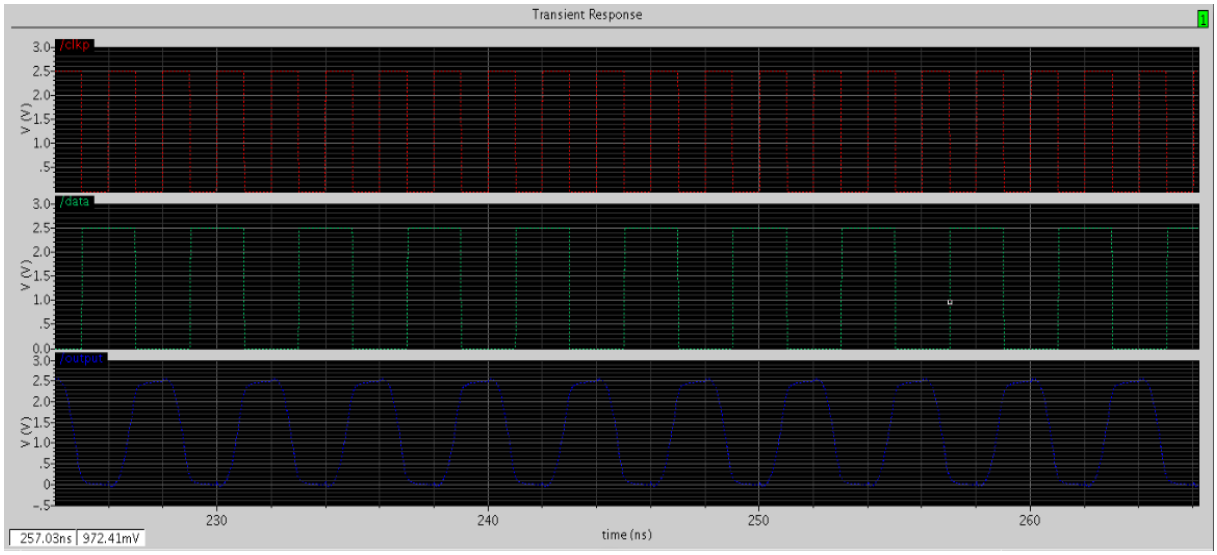

## Clk to q

1n sec

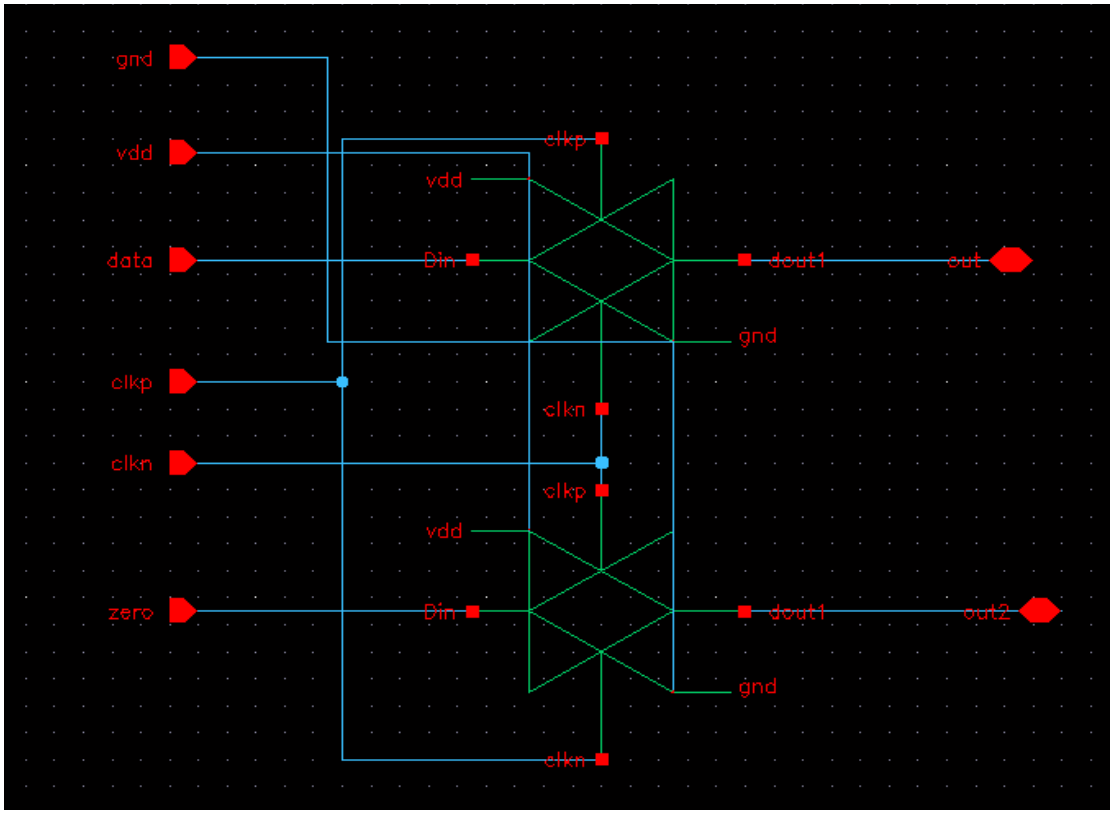



Another important conclusion reached from here was the maximum frequency for which this the flip flop will work. As the clk to q delay was 1 ns we found out the max freq as: 1/2ns = 500 Mhz.

This was also later verified by the simulation results.

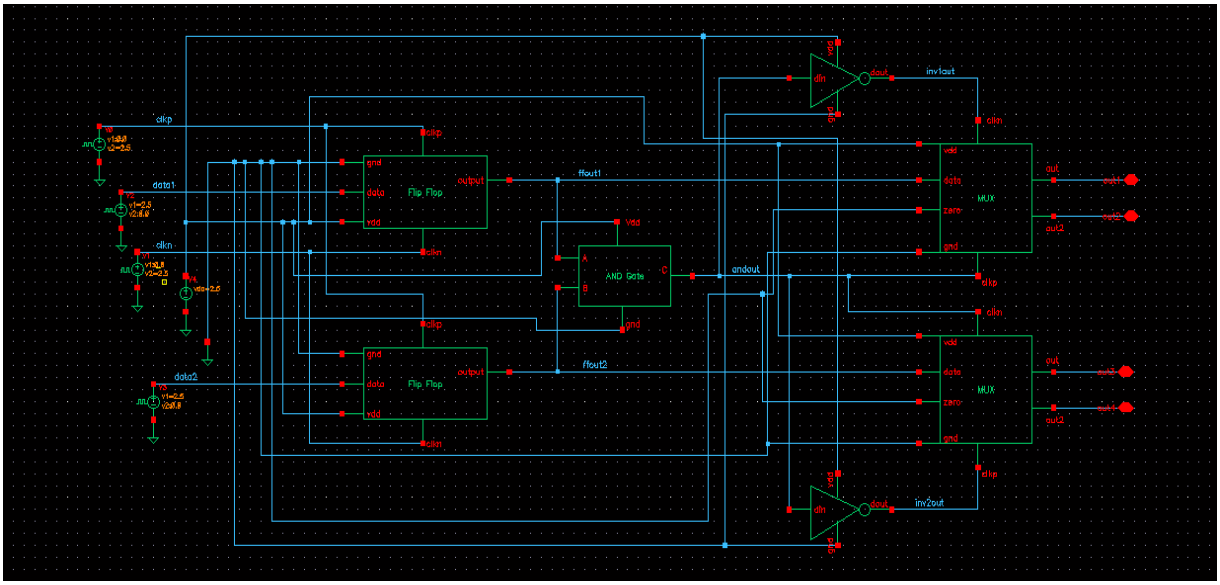



The next step was to implement the reset function in the 2 flip flops. This was done by using 1 AND gate and ! MUX. The MUX had 2 inputs one was zero and other was the flip flop's output. The clock to the MUX was provided by the AND gate.




The idea is, whenever there will be level high at the on both flip flop outputs the AND gate will deliver a logic high which will turn on the transmission gate having input zero and

thus we will get a logic low at the final output i-e reset. Else we will keep getting the flip flop output as our final output as the AND gate will be passing logic low and the transmission gate will the zero input would be off.




## CHARGEPUMP:

Charge pumps receives two input signal from the PFD and decides whether it has to raise or lower down the frequency produced by the system by raising or decreasing the voltage. It is important to note here that the charge pump we are considering is with the loop filter. The charge pump's initial review and physiology has been discussed above. The calculations involved in computing the value of capacitor of loop filter and the sizes of transistors involved in the design are presented below:

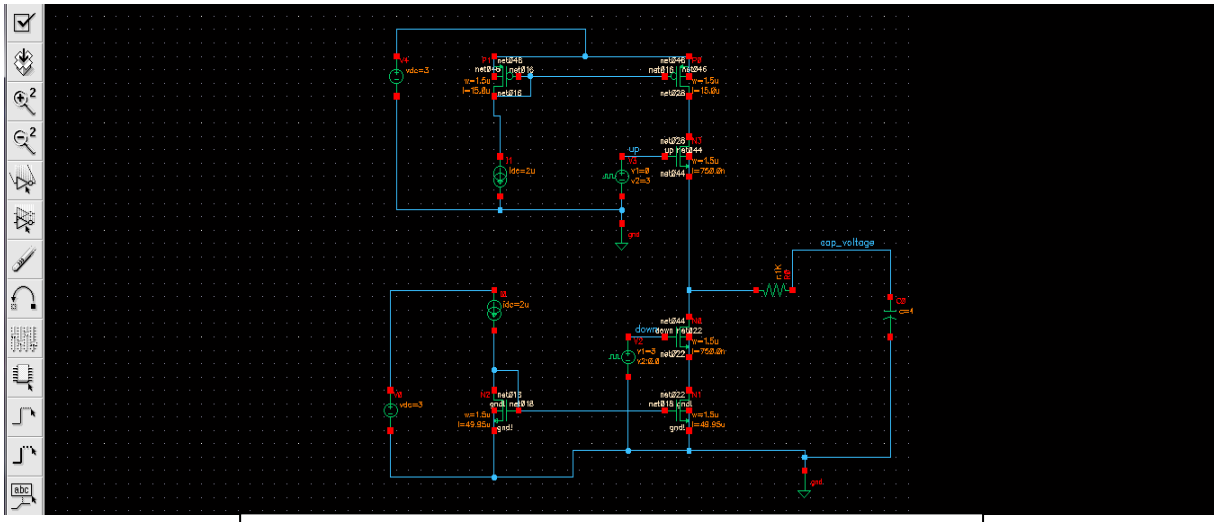



**Figure 17 Charge Pump Schematic.**

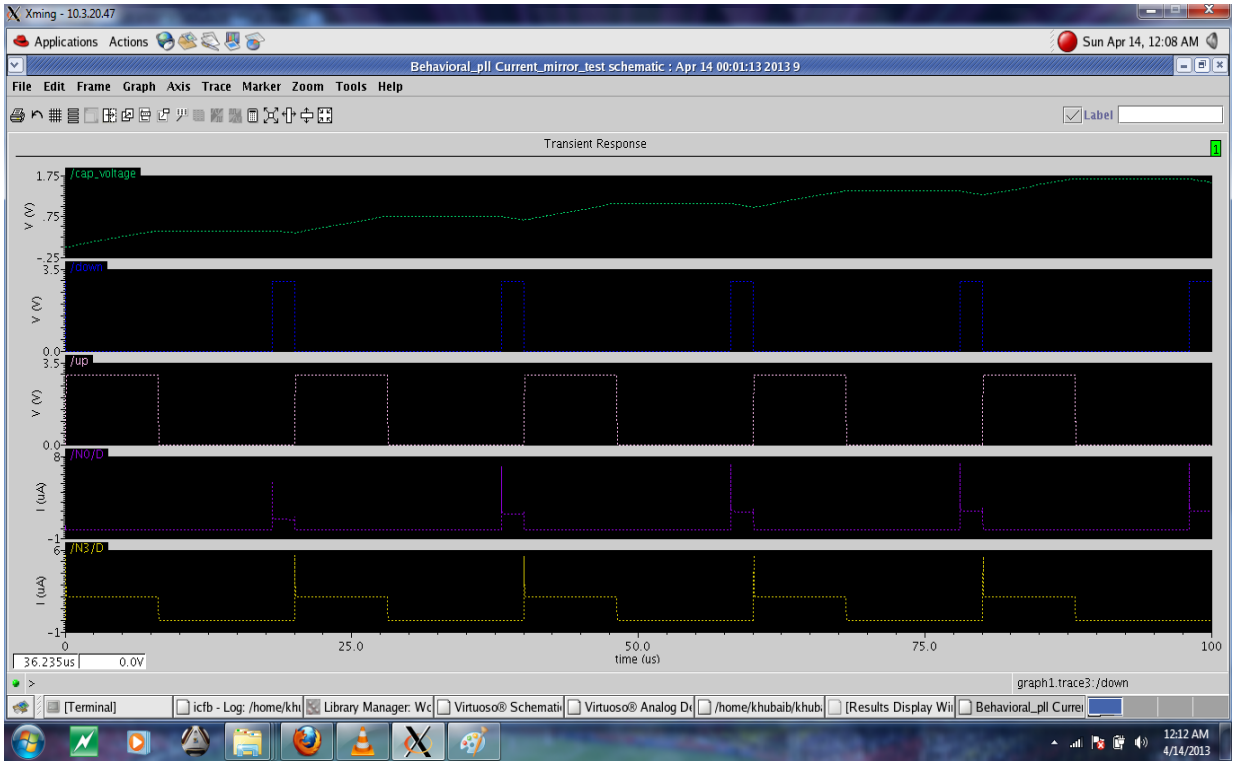



**Figure 18 Charge Pump Simulations.**

**IMPORTANT NOTE**: THE RESISTANCE OF BOTH THE CURRENT SOURCES IS VERY NEAR and in the order of 300K….. while that of switch is 5K. The glitches which you see in the current forms are because of the transition of switch. When Vgs of the switching mos increases from 0 volts to 3 volts at some point at 1.5 volts it acts as an amplifier so it extracts a maximum amount of current from the circuit that's we see a glitch at the output current. As you can see from the zoomed image also

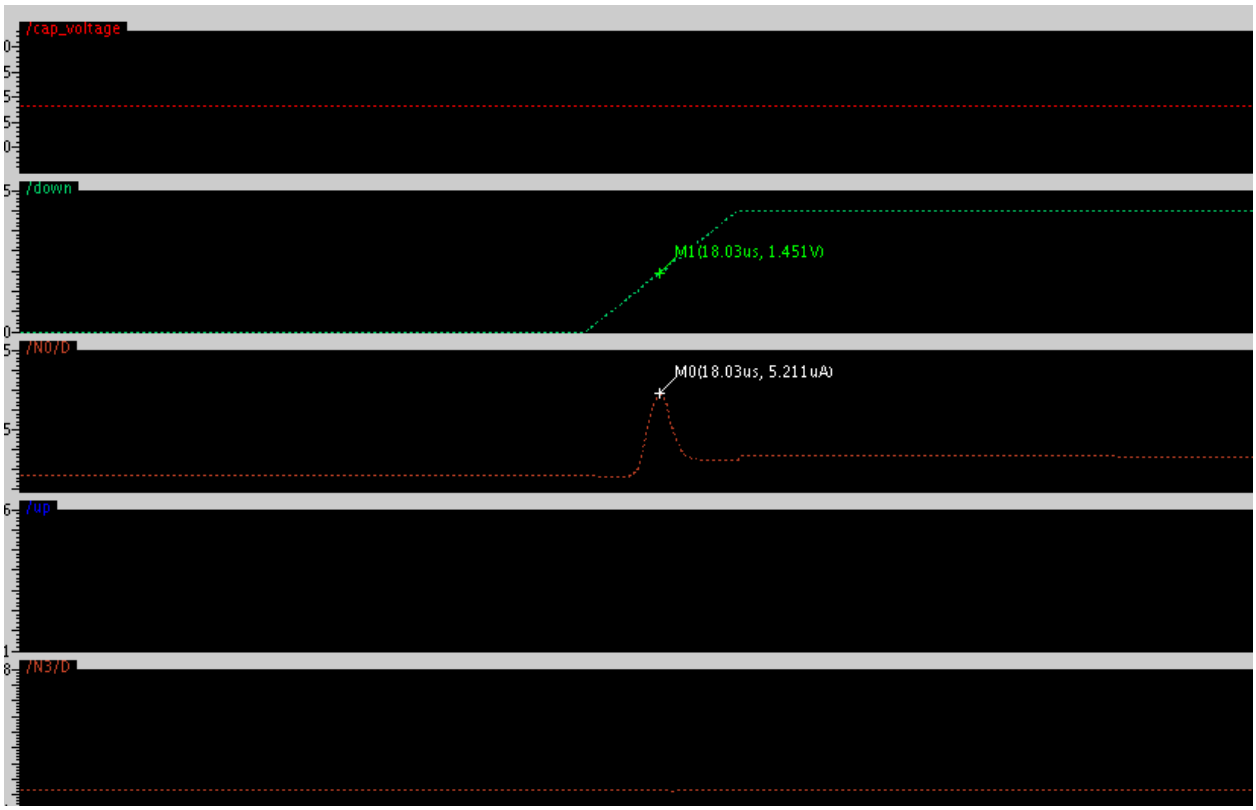



**Figure 19 Glitches in Charge Pump.**

## VOLTAGE CONTROLLED OSCILLATOR:

A voltage controlled oscillator detects voltage level on the capacitor of the charge pump and produces a signal whose frequency is according to this voltage. As discussed in the literature review the topology decided was a current starved ring oscillator because of the flexible speed range it offers and the square law correspondence between input voltage and output frequency. The hand calculations for the sizing of the voltage controlled oscillator is given in appendix A. The schematic of the device is shown below

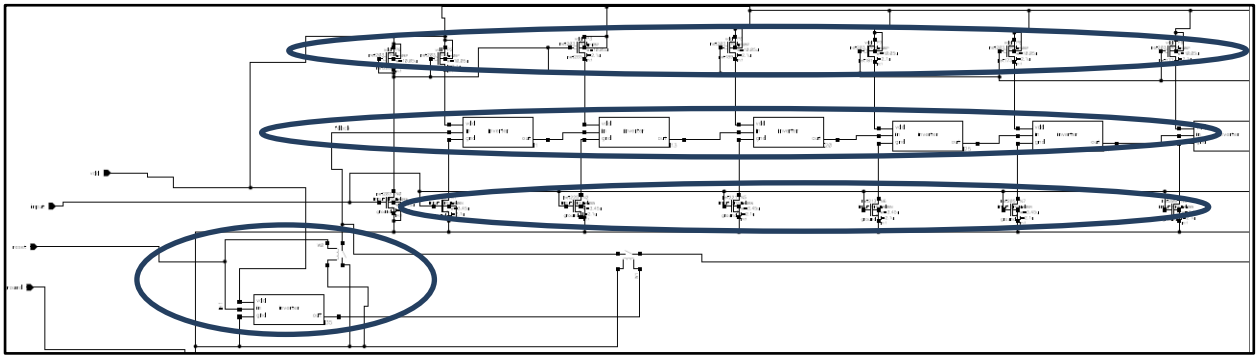
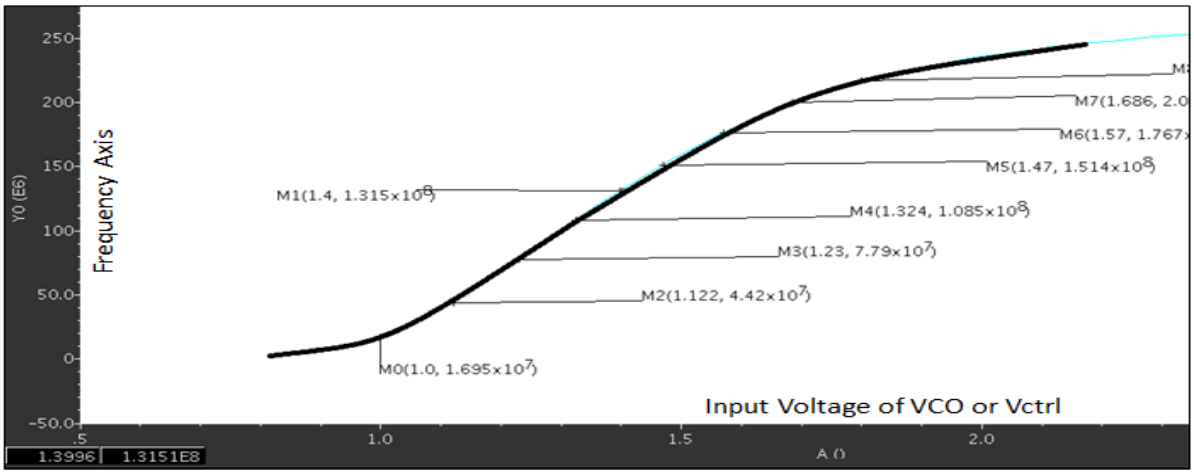


**Figure 20 Voltage Controlled Oscillator Schematic**

In the above schematic block 1 and 3 are current starving mosfets. The voltage vctrl is provided to the very first mosfet in the block 3. It generates a current proportional to that voltage and this current is mirrored to the next seven stages by the diode connected mosfet which appears first from left side in block 1. Thus these current sources and sinks control the flow of current through the inverter and hence the rise and fall time, which can be alternatively explained as the time required to charge and discharge the intrinsic capacitances at each junction. The more the voltage the more is the current and the rapidly the capacitance charges and discharges and hence the output signal has more frequency. Now the block which is not numbered and appears in the left bottom side is the reset block. Its function is to provide an initial reference to the inverter chain from where it should start oscillating. If we don't implement this block the VCO will generate a signal which is not rail to rail.

The sensitivity graph of our VCO is as follows:




**Response of our VCO block** $\text{Gain} = \Delta F_{out} / \Delta V_{in}$

**Figure 21 Response of VCO Block**

## VOLTAGE BUFFER:

A voltage buffer is a block which buffers and soothes the output. It is not a conventional PLL block but its need arose because of the fact that the VCO was producing a signal which was not matching the proper shape of a clock. So in order to bring our signal in the shape of square wave a voltage buffer was to be applied. A voltage buffer drives it output no from its input but from Vdd and ground. An exponential horn technique was implied for the generation of this block. Its schematic is given as follows:

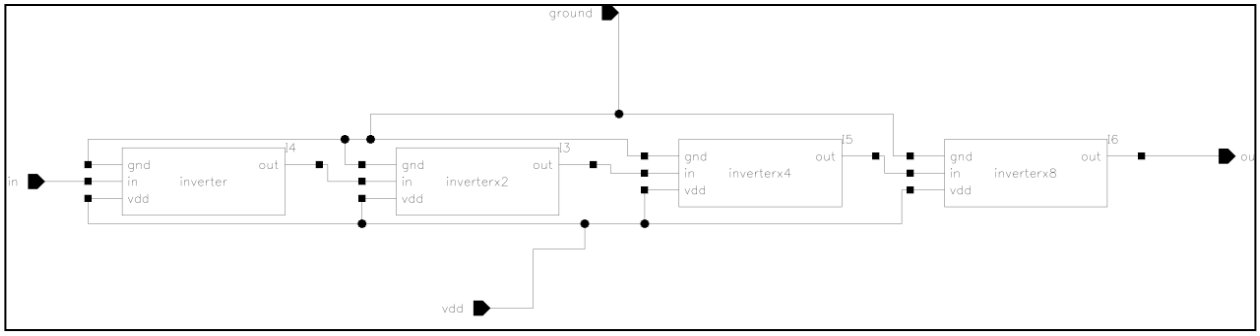



**Figure 22 Buffer Schematic.**

The buffer consisted of four inverters and the inverters were sized in such a way that the W/L ratio of the next inverter was α times larger than the last one. The effect of W/L ratio on an inverter's VTC is such that if W/L of an inverter is large its noise margins are high.

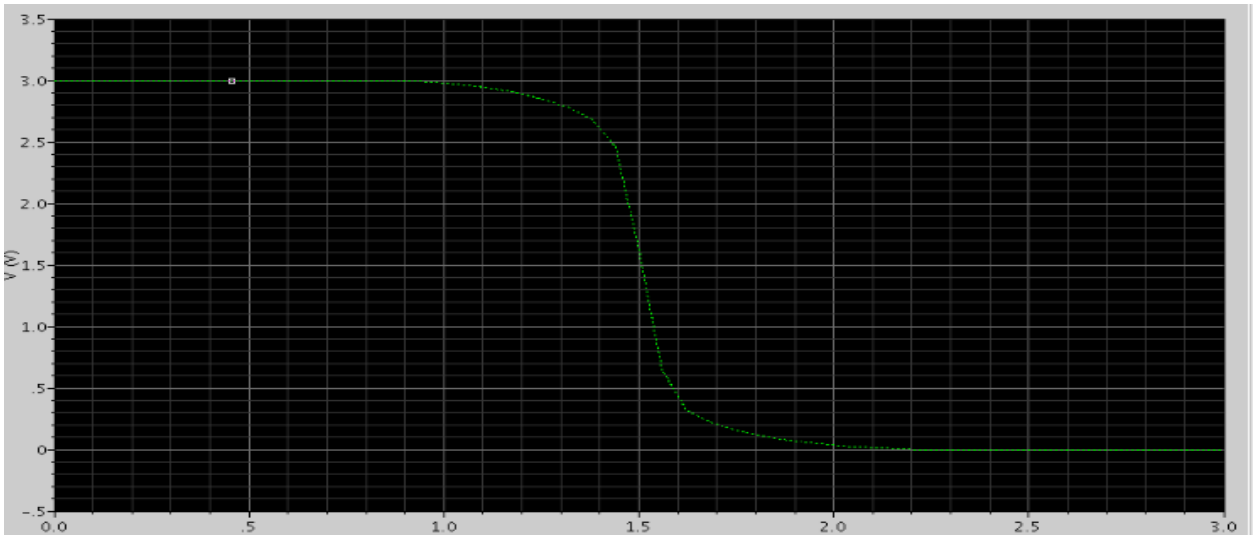



**Figure 23 Voltage Transfer Characteristics of an inverter.**

So when a signal is given to the input of the first inverter of the buffer it takes a relatively low voltage as high and a relatively high voltage as low. When this signal is given to the next inverter the voltage at which the inverter considers a signal high and low touches the ideal limit that is Vdd and ground respectively. And thus a near perfect square wave is constructed.

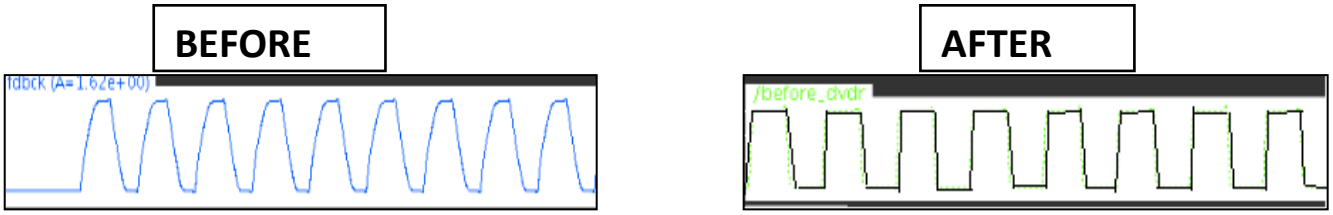



**Figure 24 Effect of buffer on output.**

## FRACTIONAL DIVIDER:

A frequency divider's main function is to misguide the PFD in thinking that exact same frequency is produced by the VCO, instead of which a much higher frequency signal is produced by the VCO and the divider lowers it down before it is feedback to the PFD. If we want our PLL to synthesize some frequency, frequency divider or fractional divider is a necessary part.

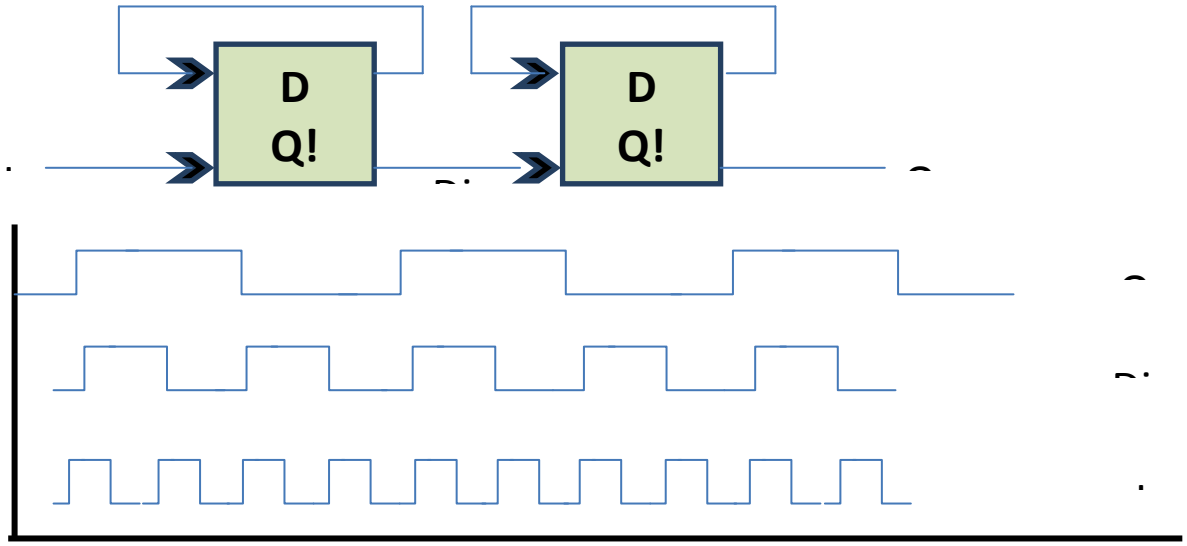



**Figure 25 Operation of a Frequency Divider.**

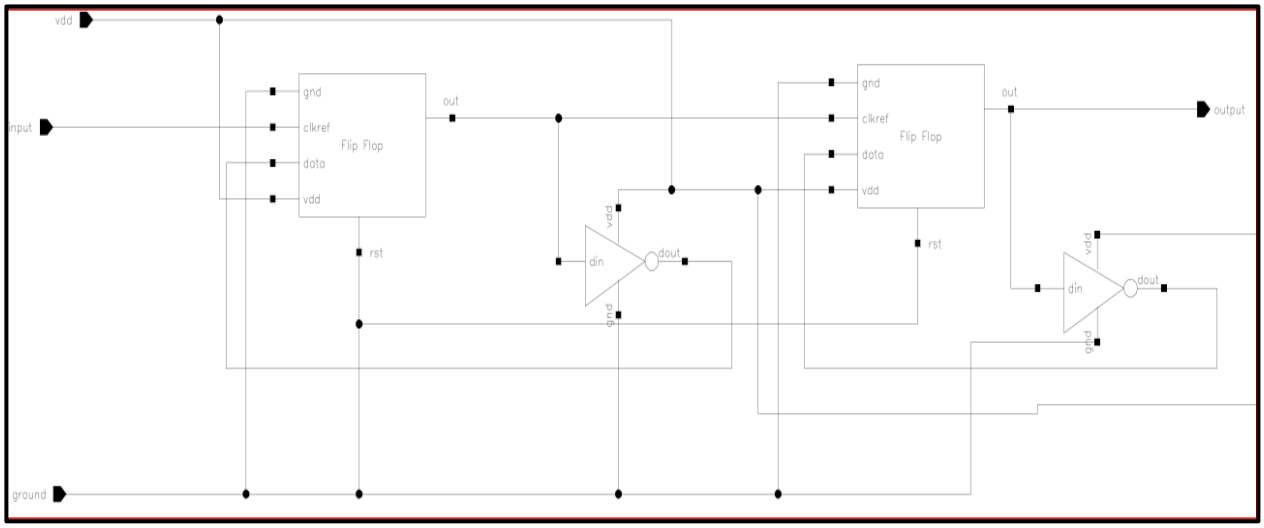



**Figure 26 Divider Schematic.**

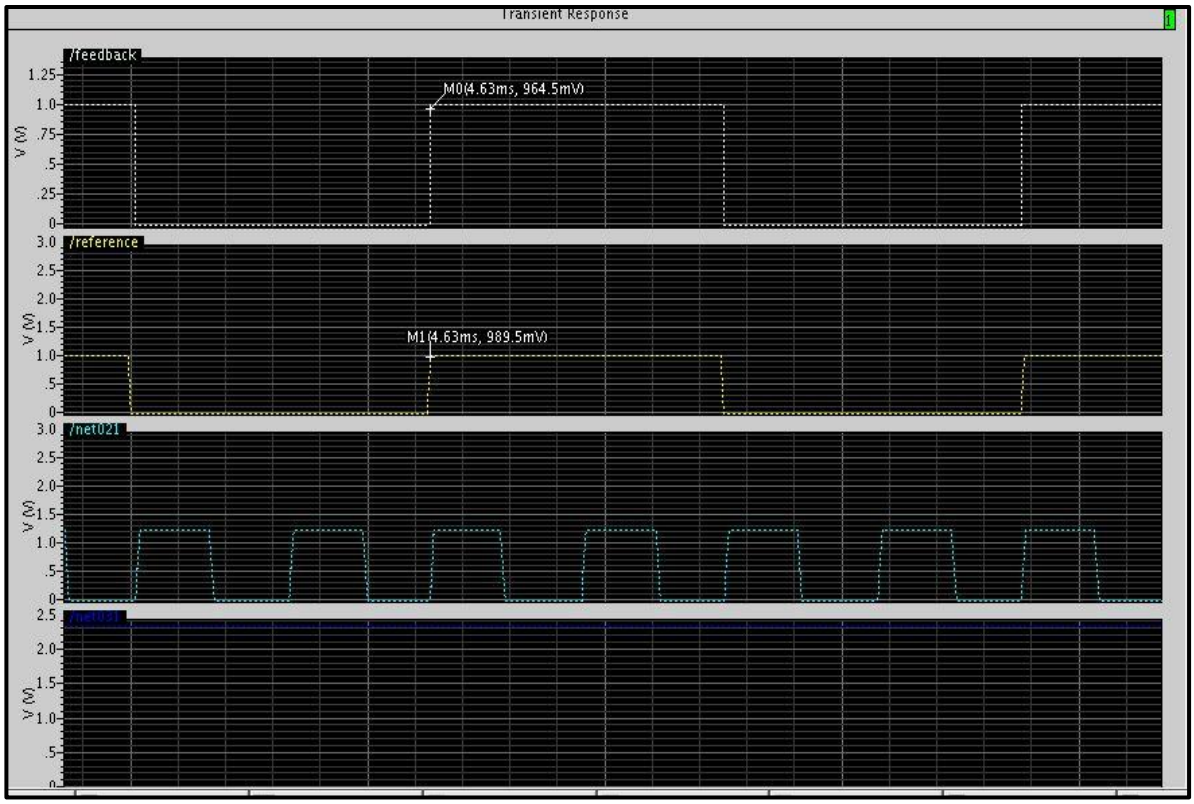



**Figure 27 Frequency Divider Response.**

## THE LAYOUT:

The next step was to draw and check the layout of our PLL schematic. 4 major steps were taken during the whole layout cycle:

1. Create Layout Cellview
2. Design Rule Checking
3. Layout Parameter Extraction
4. Layout vs. Schematic Comparison

This was started by first drawing the layout xl of the inverter and transmission gates and then moving up the hierarchy block by block. Only Metal 1 and metal 2 was used throughout the whole layout.

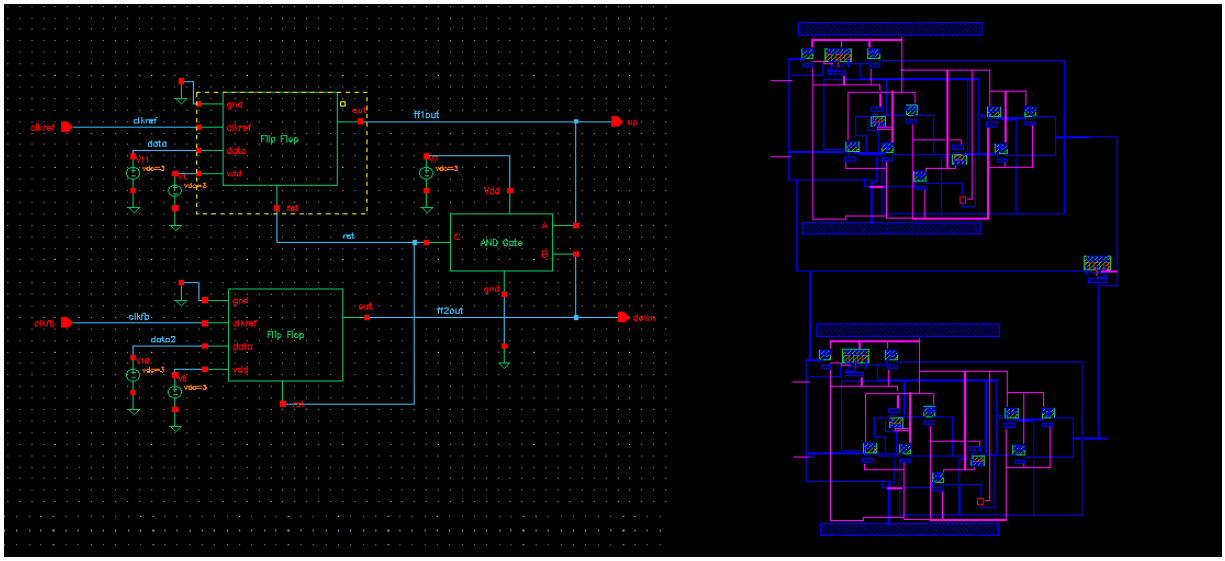



**Figure 28 Phase Frequency Detector Layout XL**

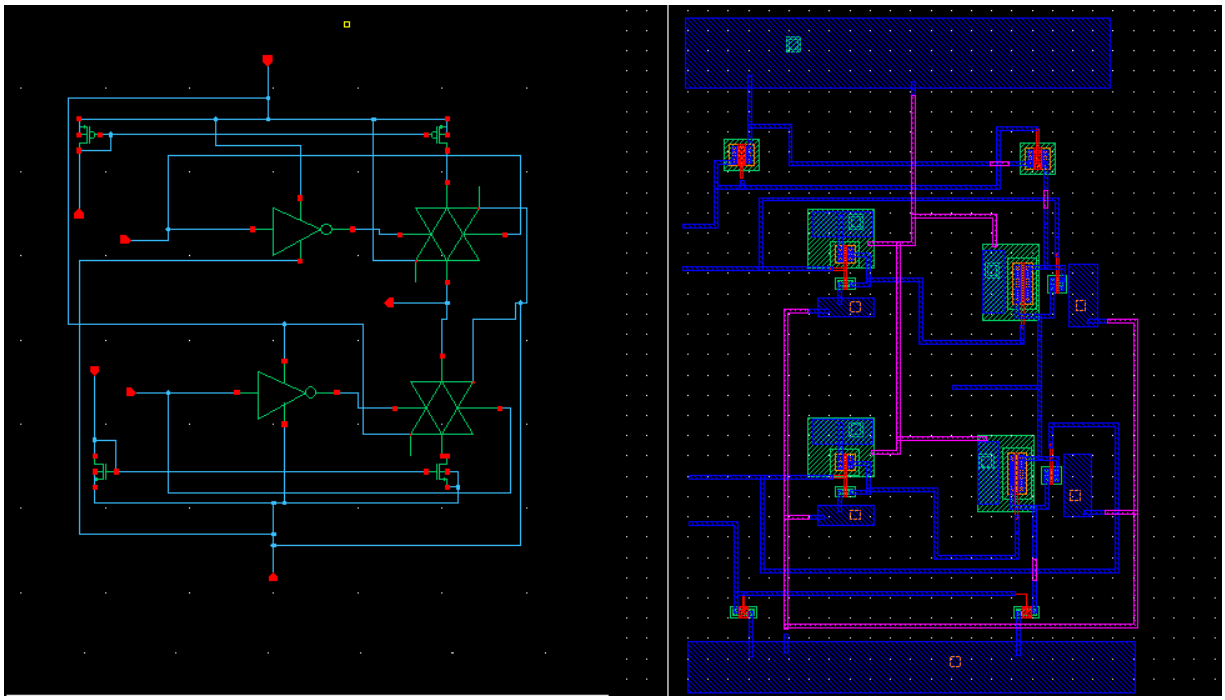


**Figure 29 Charge Pump Layout XL**

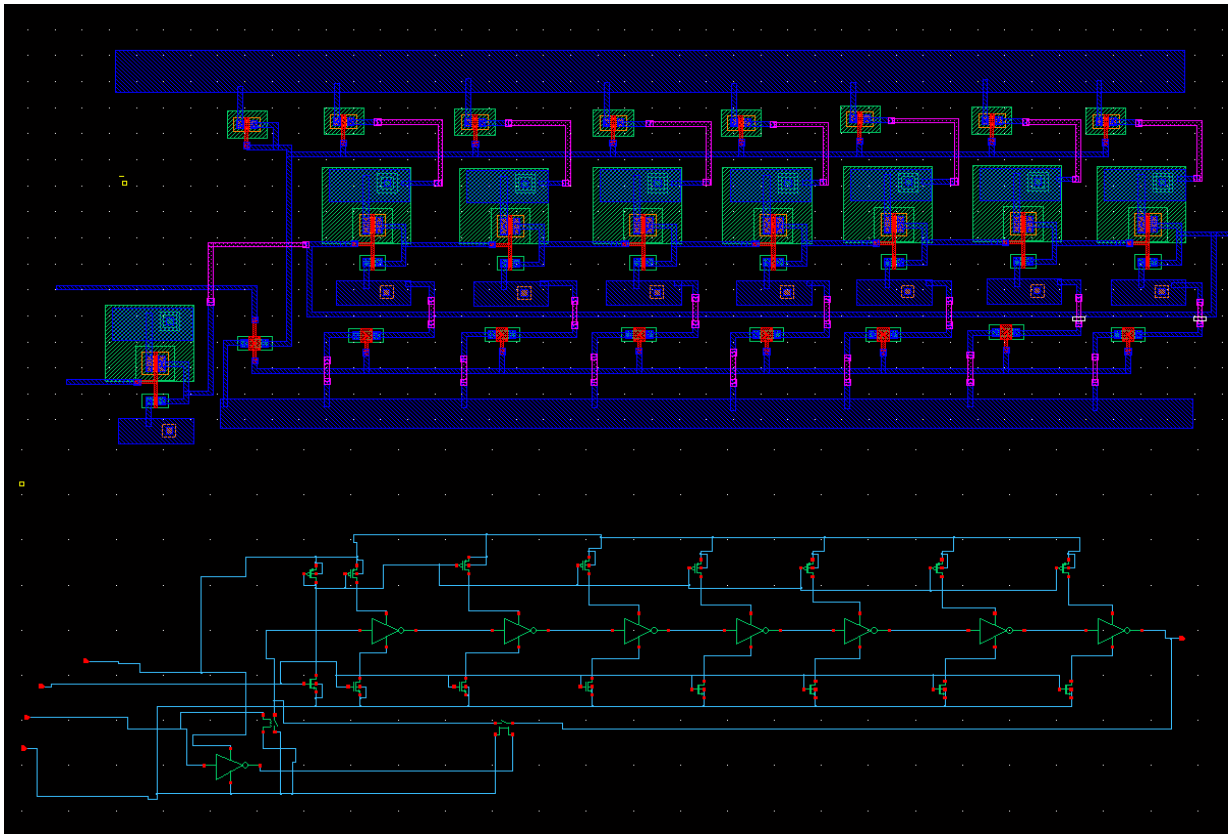


**Figure 30 Voltage Controlled Oscillator Layout XL.**

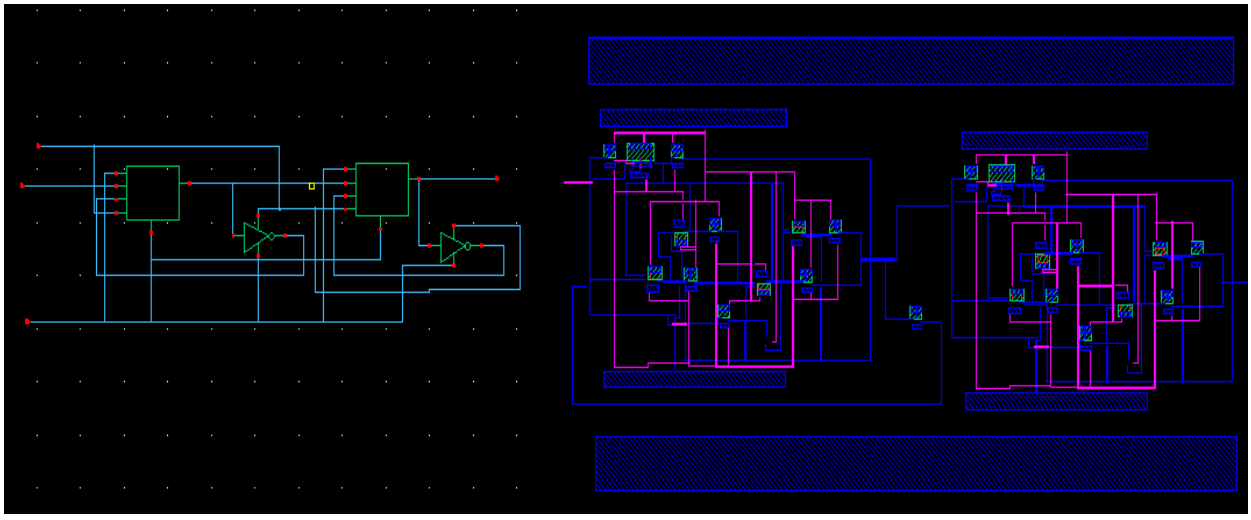


**Figure 31 Fractional Divider Layout XL**

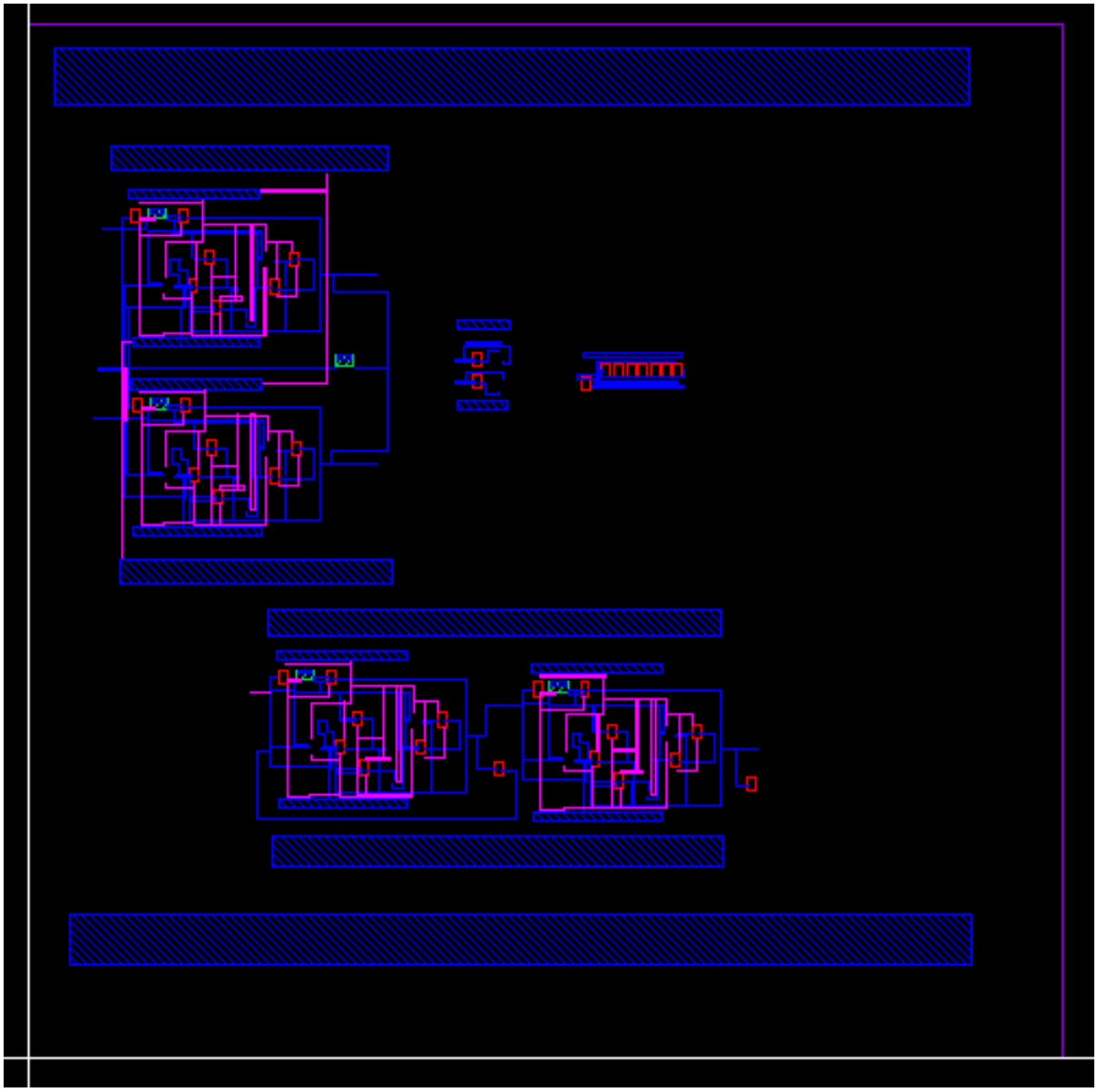
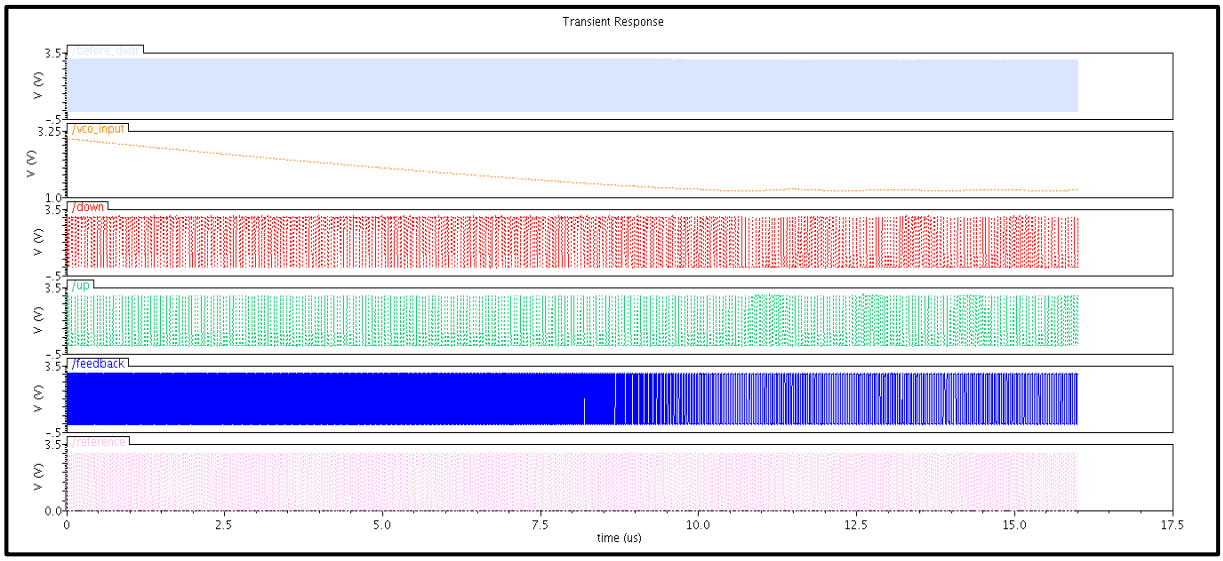


**Figure 32 Phase Lock Loop Complete Layout**

# RESULTS



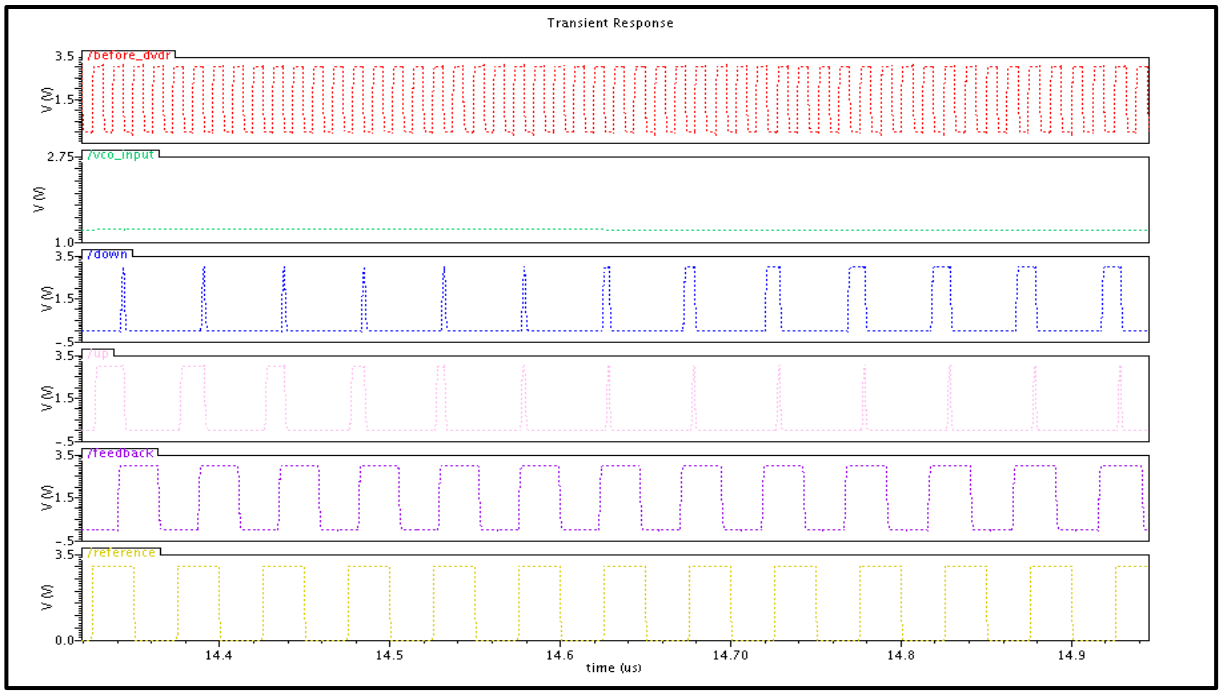




**Figure 33 System Responses at 10MHz Signal at reference.**

# CONCLUSION:

The phase locked loop made by the group works can be characterized in a lot of different ways. Before defining our PLL we have to define the terms in which the system will be elaborated.

LOCK-RANGE: the range of frequency which can be provided at the reference pin of the system, and for the range the system remain stable.

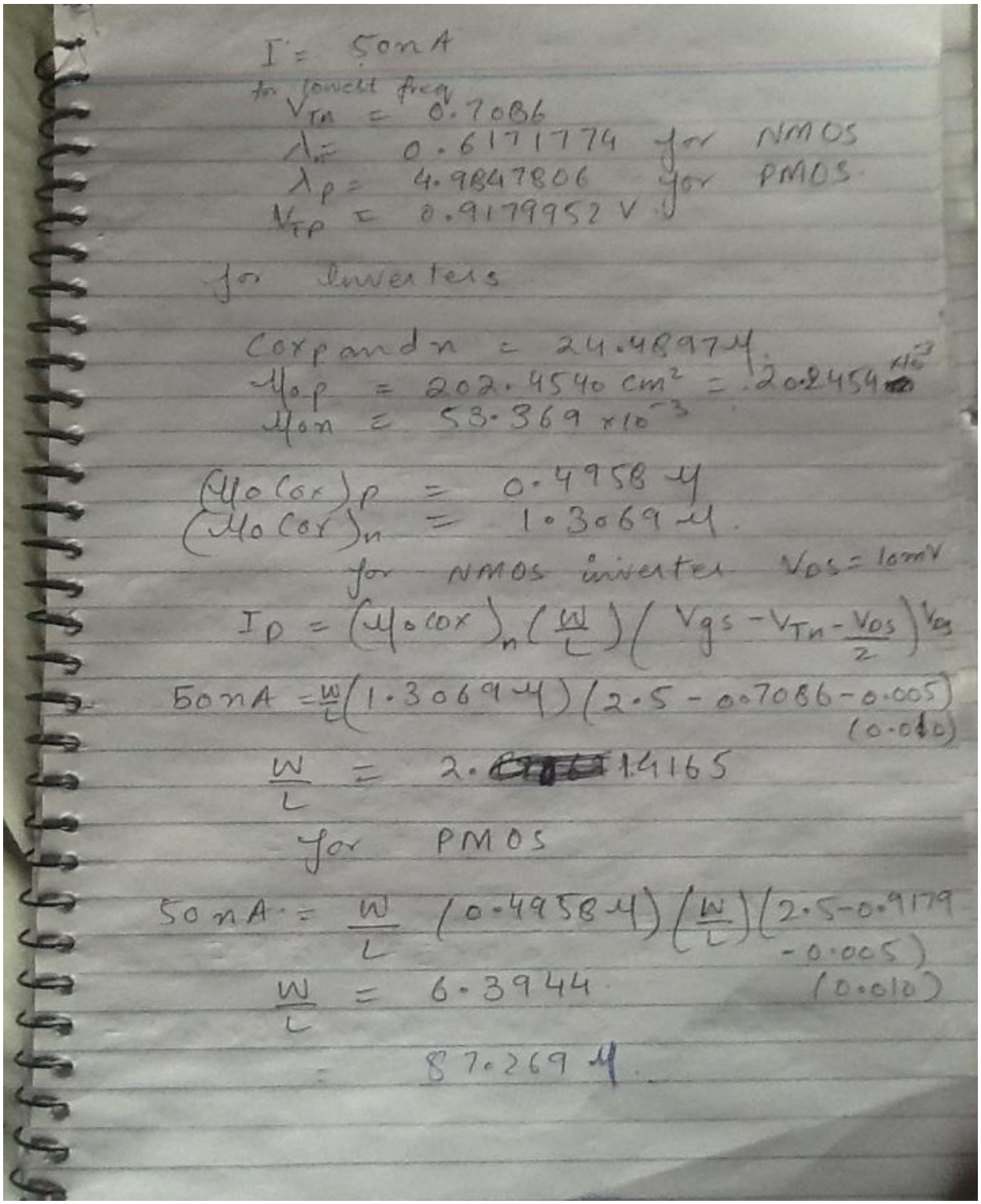
LOCKING TIME: the time required for the system to reduce the skew or to synchronize the reference to the feedback signal.

FREQUECNY SYNTHESIS RANGE: The frequency synthesis range is the range which our PLL can be produced. As our PLL incorporates a fractional divider so it will synthesize frequency.

POWER DISSSIPATION: The power dissipation is mostly dominated by the VCO as it is a current starved one. It is to be measured on the extreme case when the frequency is maximum so the current drawn from the power supply by the VCO is maximum.

The phase locked loop made by the group has a frequency range from 1MHz to 50MHz and it can synthesize rom 4MHz to 200MHz signal as the fractional N divider has the N=4. The system requires 100us to settle. The power dissipation of the system goes upto 500uW.

# APPENDIX A:



$I = 50nA$

for lowest freq

$V_{Tn} = 0.7086$

$\lambda_n = 0.6171774$ for NMOS

$\lambda_p = 4.9847806$ for PMOS

$V_{TP} = 0.9179952\ V$

for Inverters

$Coxp and n = 24.48974$

$\mu_{op} = 202.4540\ cm^2 = .20.2454$

$\mu_{on} = 53.369 \times 10^{-3}$

$(\mu_o C_{ox})_p = 0.4958\ \mu$

$(\mu_o C_{ox})_n = 1.3069\ \mu$

for NMOS inverter $V_{os} = 10mV$

$$I_D = (\mu_o C_{ox})_n \left(\frac{W}{L}\right)\left(V_{gs} - V_{Tn} - \frac{V_{os}}{2}\right)^{1/2}$$

$$50nA = \frac{W}{L}(1.3069\mu)(2.5 - 0.7086 - 0.005)\ (0.010)$$

$$\frac{W}{L} = 2.[redacted]1.4165$$

for PMOS

$$50nA = \frac{W}{L}(0.4958\mu)\left(\frac{W}{L}\right)(2.5 - 0.9179 - 0.005)\ (0.010)$$

$$\frac{W}{L} = 6.3944$$

$$= 87.269\ \mu$$

$C_{JSW} = 3.8256 \times 10^{-10}$ $C_{gate} = 3.1147 \times 10^{-10}$

Capacitance of Inverter

Model:

$$C_{gate} = C_{ox}(W_p L_p + W_n L_n)$$
$$= 24.4897 \times (1.5986 \times 10^{-17} + 5.354 \times 10^{-17})$$

$$C_{gate} = 52.26 \times 10^{-18} F$$

$$C_{Bottom} = C_{Jn}(W_n L_n) + C_{Jp}(W_p L_p)$$
$$= 6.762 \times 10^{-16} + 1.1627417 \times 10^{-15} + 2.26742 \times 10^{-16}$$
$$= 1.8538 \times 10^{-15} F$$

$$C_{SW} = (W_n + 2L_n) C_{JSWn} + (W_p + 2L_p) C_{JSWp}$$
$$= 500 \times 10^{-9} (4.14165) C_{JSWn} + 500 \times 10^{-9} (8.3944) C_{JSWp}$$
$$= 7.92214 \times 10^{-16} + 1.3073 \times 10^{-15}$$
$$C_{SW} = 2.0995 \times 10^{-15} F$$

$$C_{DB} = C_{Bottom} + C_{SW}$$
$$= 3.9533 \times 10^{-15} F$$

~~TOTAL~~ $C_{TOT} = 4.00526 \times 10^{-15} F$

a) 50nA = $I_D$

$r_{on_n} = \frac{1}{\lambda_n I_D} = 32.4\ M\Omega$

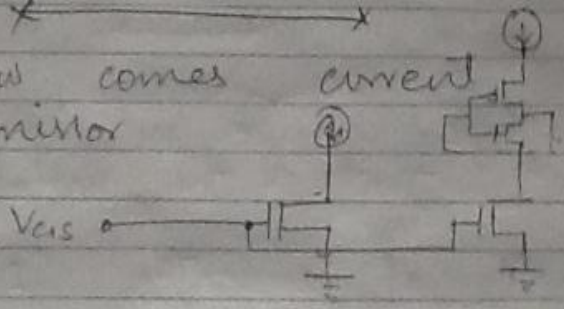
$R_{on_p} = \frac{1}{\lambda_p I_D} = 4\ M\Omega$

$f_{osc\ (low)} = \frac{1}{2 \times 7 \times C_{ox}(R_{on_n} + R_{on_p})}$

$= \frac{1}{5.607 \times 10^{-14}(R_{on_n} + R_{on_p})}$

$f_{osc\ low} = 0.5\ M\Omega$

Now comes current mirror




$V_{GS} = 0.7 + 0.25 = 0.95V$

~~50nA~~ $I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2$

~~50nA~~ $\frac{W}{L}_{nmos} = 1.2024$

$\frac{W}{L}_{pmos} = 0.1029.$

# APPENDIX B:

Design of current mirrors & sources.

~~NMOS~~

points to remember.

for NMOS as we go from weak to strong inv region. $\mu_n C_{ox}$ decreases.

Tentative range ~~80u~~ 100u - 55u.

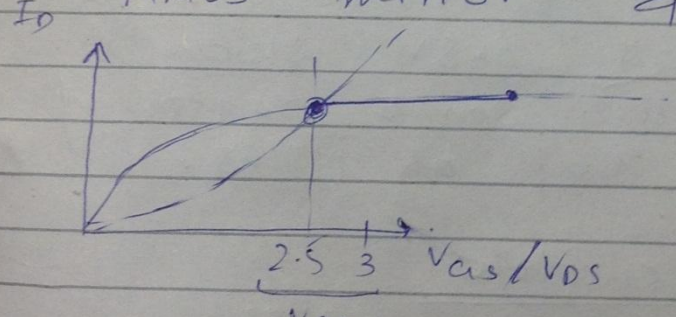
for PMOS same case

Tentative range

50u - 22u.

$V_{TH}$ is inversely proportional to $W/L$.

NMOS mirror & source




$V_{TH} = 0.98\ V.$

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2.$$

$$2u = \frac{1}{2}(56u)\frac{W}{L}(2.517 - 0.98)^2.$$

If was simulated at $I_D - V_{DS}$ curve that @ $V_G = 2.517$ we obtain 2uA current

$$\frac{W}{L} = 0.03$$

$W = 1.5u$ (minimum)

$L = 50u$

~~Values given~~

For PMOS

as

$$\frac{(\mu_n C_{ox})_n \text{ @ saturation}}{(\mu_n C_{ox})_p \text{ @ saturation}} = \frac{56\mu}{20\mu} = 2.8$$

$$\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n * 2.8 = 2.8 \; 0.084.$$

so $\boxed{\begin{aligned} W_p &= 1.5\mu \\ L_p &= 18\mu \end{aligned}}$

Eq for This

a PMOS $I_D - V_{GS}$ was simulated ~~2.5V~~ 2μA current was obtained at 0.5V which is correspondingly the same region of inversion as that of NMOS.

Now switch.

That would be NMOS.

$V_{DS} = 10mV$ $V_{GS} = 3V$

$I_D = 2\mu$ $V_T = 0.88V$

for greater W/L.

$$I_D = \mu_n C_{ox} p \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$\therefore \mu_n C_{ox} = 43\mu$.

$$\frac{W}{L} = 2.2.$$

*

point $V_{TH}$ & $\mu_n C_{ox}$ remain constant over $V_{DS} - I_D$ — curve.

* for this $\frac{W}{L} = 2.2$ NMOS

$R_{on} = 5.017 k\Omega$

$W = 1.354$
$L = 600nM$

* point $V_{TH}$ is not affected by $V_{DS}$ or $V_{GS}$ but only by $\frac{W}{L}$.

# REFERENCES

- **Inverters (Johan Rabaey Chapter#5)**
    - Concepts like Noise Margin.
    - Delay Controlling Knobs.
    - Threshold Voltage.
    - Power Dissipation(static & dynamic).
- **Wiring (Johan Rabaey Chapter#4)**
    - Concepts like Capacitance of wire broken into parallel and fringe capacitances.
    - Resistance including skin effect(frequency dependent parameter).
    - Models for estimation of delay due to wire.
    - Lumped, Lumped RC, Distributed RC.
    - Termination, Lattice Diagram.
- **Basic Know How of ESD Pads.**
- **Phase locked loop. (Behzaad Razavi Chapter#15)**
    - Purpose of PLL.
    - Intuitive Understanding and recognition of all sub blocks.
    - Comparisons b/w DLL and PLL and Digital PLL. (what parts are different like difference

    In charge pump and time to digital converter and VCO replaced by delay line),

    reference: (All Digital Phase Locked Loop Design and Implementation by Anitha Babu, Bhavya Daya, Banu Nagasundaram, Nivetha Veluchamy University of Florida, Gainesville, FL, 32608, USA )

- ***Phase locked loop. (Behzaad Razavi Chapter#15)***
    - *Difference in terms of applications DLL & PLL (clock synthesis etc.)*
- ***Voltage Controlled Oscillators (Behzaad Razavi Chapter#14)***
    - *Types of Ring Oscillators (differential & Single Ended).*
    - *Single Ended RO architectures in terms of delay elements.*
        - *A Variable Delay Line PLL for CPU-Coprocessor Synchronization By Mark G Johnson Section IV.*
        - *Linear Current Starved Delay Element by Goran S. Jovanovic Section II.*
        - *A 1.2um CMOS Current Controlled Oscillator Micheal P Fynn.*
- ***Miscellaneous Architectures Visited During The Literature Survey.***

- *To prevent False locking Problem.*
    - *A Low-Jitter Delay-Locked Loop with Harmonic-Lock Prevention Sungkyung PARK, Changsik YOO,and Sin-Chong PARK.*
- *High frequency Clock Generation Through A Delay Line*
    - *Low-Jitter Clock Multiplication: A Comparison Between PLLs and DLLs. Remco C. H. van de Beek, Eric A. M. Klumperink,Cicero S. Vaucher.*
    - *Design of PLL Based Clock Generation Circuits.*

- ***Miscellaneous Architectures Visited During The Literature Survey.***
    - *High Speed Topologies.*
        - *Negatively Skewed Topology (A Novel High-Speed Ring Oscillator for Multiphase. Clock Generation Using Negative Skewed Delay Scheme Seog-Jun Lee, Beomsup Kim, and Kwyro Lee)*
        - *Multiple Feedback Loops Topology (A 1.25-GHz 0.35-□m Monolithic CMOS PLL, Based on a Multiphase Ring Oscillator Lizhong Sun and Tadeusz A. Kwasniewski)*
        - *Coupled Oscillators (Precise Delay Generation Using Coupled Oscillators, John G. Maneatis and Mark A. Horowitz).*

- ***Hand Calculations Of VCO.***
    - *Capacitance Modeling at the edge of each delay element. (Johan Rabaey Chapter#3&5)*
    - *Ring Oscillators Characteristics and Applications By M.K Mandal & B.C Sarkar*
    - *A Method To Drive An Equation For the Oscillation Frequency of a RO by Stephen, Docking & Manoj Sachdev.*
    - *Current Mirror Understanding as the biasing circuitry.*
    - *Making Of suitable Assumptions For Designing.*