INTRODUCTION

The efficient and reliable performance of solid-state devices that are building blocks of integrated circuits have become critically important in an era of microprocessors. In order to ensure durable working conditions during operations, scaling these devices to the nanometer scale creates a challenging situation for designing and modeling. However, the presence of localized impurities and size miniaturization to the nanoscale regime has become significant, rendering traditional approaches to nanometer scale manufacturing and cooling inadequate. The influence of ever-more powerful technology on our culture is growing. To avoid premature component breakdown, the enormous heat generated by today's electronics must be drained.

For engineers, thermal design has become a great challenge. Cellphones, data centers, home electronics, telecommunications and other electronic devices need thermal management for their safe working. In order to meet the demand of users to have efficient gadgets, there must be an increase of power of critical electronic components.

1.1. **Joule heating**

In electronics, Joule heating, which is also known as resistive or Ohmic heating, is an unavoidable phenomenon because it is caused by the inelastic collision of the charge carriers due to applied electric field. That collision produces a conversion in the electrical energy to the thermal energy by the material lattice vibration. Many devices such as electric heaters, iron and toasters function on this principle, but with the passage of time, this heat generation poses barriers to the safe operation of many devices. For instance, motherboard processors normally need temperatures below ~ 85 ° C for their safe operation.

This phenomenon becomes more critical when miniaturization of electronic devices take place by following Moore’s law [3], which is presented by Gordon Moore who is Intel co-founder. In 1965, he predicted that the number of transistors on a dense integrated circuit would quadruple every year, and he was correct. In 1975, this forecast was updated to a doubling of chip density every two years, implying that the size of transistors will be cut in half every two years. The 10 nm chip lithography node has been achieved, with the industry now shifting toward 7 nm and 5 nm fabrication technologies.

Dennard scaling; is another theory about number of transistors on chip. That theory had scaled the number of transistors on a chip and its states that even as transistors get smaller, their power density remains constant. A microprocessor of the same geometric size with a higher transistor count would therefore still consume the same power as one with a lower count of larger transistors [1]. This was made possible by a reduction in the voltage required to sustain a constant electric field across smaller transistors, in turn reducing the power requirements. As shown in Figure 1.2, together with Moore's law,

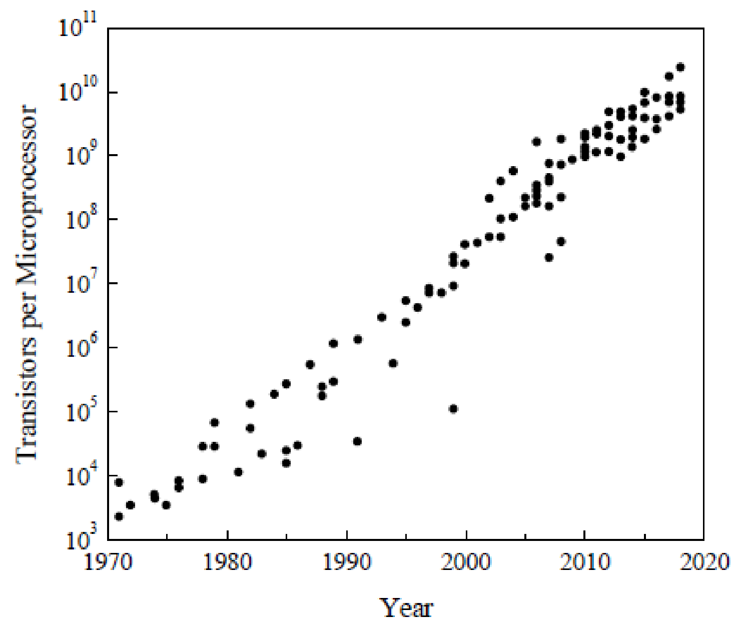

Figure 1.1: F. Labonte and K. Rupp [2] also collected data that shows 46 years of microprocessor data count.

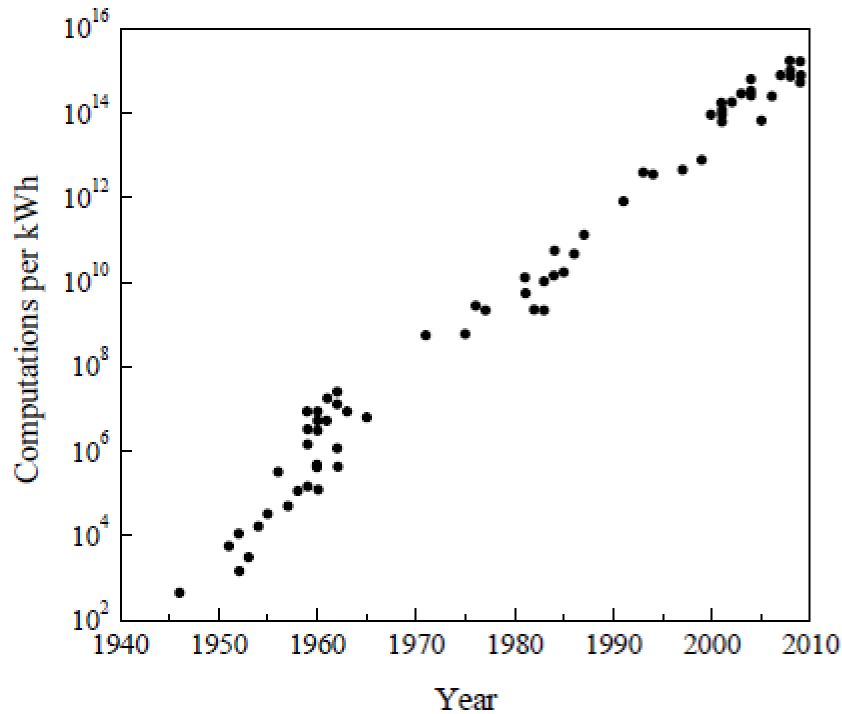

Figure 1.2: Data from Koomey et al. [3] shows the improvement in computations per kilowatt hour from 1946 to 2009.

Transistor count on chip had increased in past half century due to intensive work on microprocessor by the industry's leading companies.

Although transistor count has continued to increase in recent years but there is also a significant change in device performance and material properties that cause a transition from continuum regime to the nanoscale, that resulted in the breakdown of Dennard scaling around 2006[4]. As a fraction of the total power supplied, static power losses increase rapidly due to short channel effects and a decrease in unit dimensions and voltages, the decrease in the thermal conductivity of the material and the temperature of the unit are also the features, thus being implicitly depending on dissipating total power [5]. Therefore, continued miniaturization creates significant problems in the thermal management and control of electronic devices due to a very high rise in high performance chip power density. A closer re-examination of technology growth since 2000 Koomey and Naffziger suggested that, due to the end of Dennard scaling and the slowing of Moore's Law output per watt has now doubled every 31 months [6], [7], [8]. Despite the industry shifting its attention to rising processor cores instead of clock frequency, the number of active switching elements per unit area has continued to increase. Conventional cooling methods are

increasingly failing to meet the high cooling demands of emerging electronic devices, and an enhanced understanding of the processes regulating heat generation and dissipation requires the development of more efficient cooling technologies.

1.2. Electrical Conductivity and Material Classifications

A characteristic feature of all crystalline solids is translational symmetry in geometry, which in turn includes a translationally symmetrical atomic electrostatic potential distribution. Electron energy levels are organized in bands that may be conducting or forbidden for such a system: electrons may spread in a conduction band, but cannot be put in a forbidden band, resulting in gaps in the permissible spectrum of energy [9]. Because the current flow requires electrons to travel from one state to another, carriers cannot flow by either fully empty or completely complete bands, the latter because of the Pauli exclusion principle, which prohibits the same quantum state comprises two or more electrons from the same quantum state.

The valence band is the highest occupied band in a material, while the conduction band is the next possible non-filled higher-energy band. All crystalline solids may be classified into one of three categories depending on their electrical properties: metals, semiconductors, and insulators (in order of decreasing electrical conductivity). Figure 1.3 is a simplified energy band diagram that represents a visual comparison of these classes. The conduction band of a metal is only partly filled at absolute zero temperature [9], meaning it contains both electrons and empty states. This helps electrons to cover the distance between states with the help of electric field, since the conduction and valence energy levels. Bands overlap, requiring very little energy to conduct carriers in metals, and therefore have very high electrical conductivity.

However, the conduction band is fully empty in semiconductors and the valence band at absolute zero temperature is completely full. The device reaches its minimum energy configuration at 0 K in which electron bands are gradually filled from lower to higher bands of energy. Because temperature is a measure of a system's internal energy. Temperature configurations are accomplished by advancing electrons from lower energy states to higher energy ones. The energy difference between valence and conduction, at room temperature, therefore, bands are small enough to make any observable conductive band population. For semimetals, at room temperature, the energy difference partially disappears so that the bands of conduction and valence converge. In an insulator, by comparison, even at room temperature, the prohibited energy difference

between the two bands remains very high, such that very little current flows after the application of an electric field.

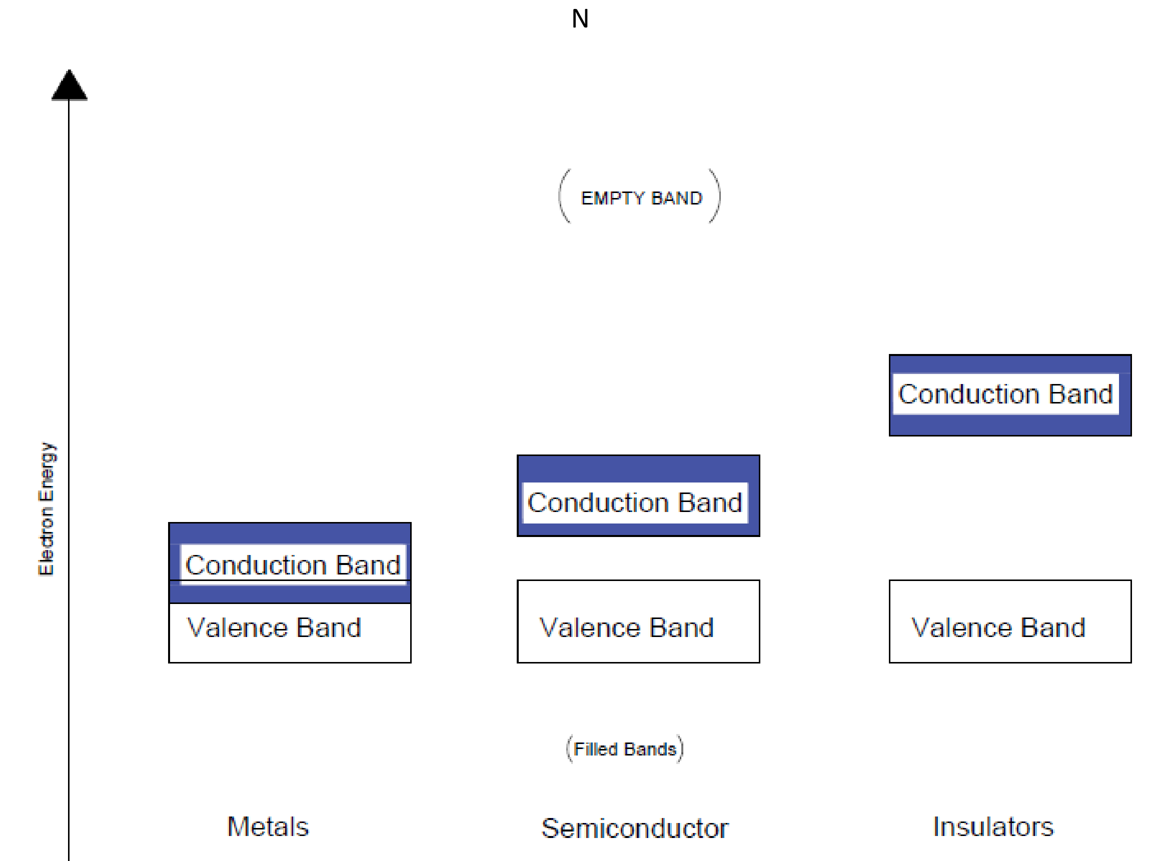

Figure 1.3: Energy band diagrams for crystalline solid classification

1.3.Semiconductors in Electronics

Semiconductors are essential in the design and functioning of electronic devices. Their limited but nonetheless existing band difference, unlike conductors and insulators, can be varied by temperature and, more importantly, impurity level [10], [11], thus enabling their electrical and thermal properties to be easily and significantly altered to meet specifications. In diodes, their sensitivity to these external variables enables their usage for, amplifiers and transistors applications that are basic components for modern electronics.

Single species of atoms consist of elemental semiconductors, such as germanium (Ge), silicon (Si), and selenium (Se). There are also binary, ternary and quaternary semiconductor compounds, consisting of two, three or four distinct components, the most common of which include elements

from the third III and V groups of the periodic table, such as arsenide gallium (GaAs) and indium phosphide (InP). Silicon is the most commonly used semiconductor in the electronics industry since, by silicate crystals found in the earth's crust, it is the second most readily available material on earth. Owing to the four valence electrons of each atom forming perfect covalent bonds, Si crystals have the ability to withstand high temperatures and have a lower cutoff (reverse bias) current than most other elemental semiconductors, but this comes with the downside of a higher potential barrier forward bias mode [12].

Whether by an increase in temperature or photoexcitation, the promotion of electrons from the valence band to the conduction band enables a semiconductor to conduct electricity. Furthermore, in the valence band, positive charged vacancies, called holes, are left behind, allowing the band to start conducting as it is no longer fully full. Therefore, semiconductors' electrical conductivity can be due to either electrons or holes, or both, unlike a metal in which electrical conduction only happens because of electrons.

The hole and electron concentrations at thermal equilibrium are equal in a semiconductor with no deliberately added impurities (intrinsic). The electrical conductivity of such a semiconductor increases with rising temperature [11] as more electrons are pushed from the valence band to the conduction band, a greater number of charge carriers are thus formed. An alternative way to adjust the conductivity at any given temperature by many orders of magnitude is to apply impurities to the semiconductor, a method called doping. An extrinsic semiconductor is often referred to as a doped semiconductor, whereas a degenerated semiconductor is so heavily doped that it behaves more like a metal than a semiconductor. The general relationship between carrier concentrations in any thermal equilibrium semiconductor is defined by the Law of Mass Action [10]:

$$n_0 . p_0 = n_i^2 \quad (1.1)$$

where n_0 and p_0 are the concentrations of the conducting electrons and holes respectively, and n_i is the intrinsic carrier concentration of the material. Note that for an intrinsic semiconductor at thermal equilibrium: $n_0 = p_0 = n_i$.

With either electron acceptor (p-type dopants) or electron donors, a semiconductor can be doped with (n-type dopants). As they replace host atoms in a silicon lattice, boron, aluminum, and

gallium act as p-type dopants because they have less valence electrons than Si, resulting in the formation of a hole in the valence band for each atom that has been replaced. Due to the addition of extra, chemically unbound electrons to the lattice, phosphorous and arsenic, which have more valence electrons than Si, act as n-type dopants, which can be readily transferred into the conduction band. In p-type semiconductors, holes are thus the main charge carriers, while the electrons in n-type semiconductors mainly contribute to electrical conduction.

1.4.Heat Conduction in Semiconductors

The migration of free conduction band electrons and interatomic collisions by lattice vibrational waves in crystalline solids together contribute to the transport of thermal energy by conduction. Applying the wave-particle principle of fundamental quantum mechanics. Each mode of lattice vibration is quantized as a phonon, according to which all types of energy and matter can be represented as either a particle or a wave [12], which can be viewed as a harmonic oscillator with a characteristic frequency ω and a wave vector **q** similar to the use of a photon as an electromagnetic quantization. Crystal momentum is similar but not equal to linear momentum: in a propagating lattice vibration, there is no net mass transport, so a phonon does not bear physical momentum.

At the continuum scale, Fourier's law is used as the conduction rate equation, which takes the general form [20]:

$$Q'' = -k\nabla T \tag{1.2}$$

where Q'' is the heat flux vector, k is the thermal conductivity of the material (a material property), ∇ is the three dimensional del operator and T is the scalar temperature field. The negative sign represents the flow of heat in the direction of decreasing temperature. The thermal conductivity may be calculated as the total of electron and phonon contributions: $k = k_e + k_p$. For pure metals, which have an abundance of free electrons present in the lattice, $k_e \gg k_p$, while the opposite is true for non-metallic solids (semiconductors and insulators) [21]. Kinetic theory provides the following expression for thermal conductivity [22].

$$k = 1/3C\bar{v}\lambda \tag{1.3}$$

where the electron specific heat per unit volume is $C = C_e$, the mean electron velocity is $\bar{v}$ and the electron mean free path is λ for conducting materials. For non-conducting materials, the phonon specific heat per unit volume is $C = C_P$, the average speed of sound is $\bar{v}$ and the phonon means free path is λ. The average free path is the average distance between the energy carrier and travels with discontinuities in the lattice and other electrons or phonons prior to collision. A longer mean free path means higher thermal conductivity, as collisions reorient the energy carrier's momentum and can cause energy dissipation to the lattice.

1.4.1 Phonon Modes

Phonons are defined on the basis of material's lattice vibrational modes, which can be in-plane or out-of-plane. Longitudinal and transverse phonon modes have in-plane modes. Atomic displacements along the path of wave propagation (compressive waves) correspond to the former, while the latter applies to in-plane displacements perpendicular to the direction of propagation (shear waves). Transverse modes may have two identical polarizations in standard three-dimensional solids, but out-of-plane atomic displacements, referred to as flexural phonons, manifest themselves in single or few-layered solids.

In addition, in-phase or out-of-phase, the displacements themselves can be coherent displacements of atoms result in lattice waves usually moving at the speed of sound from their equilibrium lattice locations, and are thus referred to as the acoustic mode. On the other hand, optical modes are excited by infrared radiation and require atomic displacements that are out-of-phase. Usually, they are found as a basis in the primitive cell in ionic crystals containing several atoms, in which the neighboring anions and cations shift in opposite directions when energized by the electric field of incident radiation. In addition to the orientation of these displacements relative to the direction of wave propagation, Phonon modes are thus characterized by the phase relationship of the atomic displacements.

For each vibrational mode, the relationship between the frequency (ω) and wave vector (q), expressed as $\omega = \omega(q)$ and called the dispersion relationship, allows the velocities of the phonon group to be calculated. The group velocity is the velocity with which a particular phonon classification transports the envelope of the lattice vibration amplitudes. The group velocity is the slope of the dispersion relation for that phonon group [13]. Thus, acoustic phonons are the major contributors to silicon heat conduction.

The energy of a phonon is measured as the product of the reduced Planck constant and the frequency of the phonon mode. A mode's collective energy E is [10], [12]:

$$E = (n + \frac{1}{2})\hbar\omega \tag{1.4}$$

where n is the number of phonons excited in that mode (also called the phonon occupation number) and $\hbar$ is the reduced Planck's constant.

1.4.2. Phonon Scattering Processes

Phonon contributes to thermal conductivity through the vibrational interactions of adjacent atoms, which are affected by impurities, crystal anharmonicities and geometric discontinuities. As they pass through a substance, phonons, electrons, and holes will scatter through multiple mechanisms, with each scattering mechanism having an associated relaxation time: the average time between two consecutive scattering events. The moments, paths and energies of the energy and charge carriers in the material are influenced by these activities and thus play a key role in deciding the thermal and electrical conductivity of a material by limiting the mobility of carriers [14].

Figure 1.4 illustrates a few different scattering types, which include scattering by stationary defects (impurities, device boundary, grain boundary etc.) and dynamic defects (electrons and phonons). Phonon-electron scattering induces lattice self-heating. These inelastic collision events transfer energy to the phonons from the charge carriers (electrons accelerated by an applied electric field), with the direction of particle motion being increasingly random with consecutive

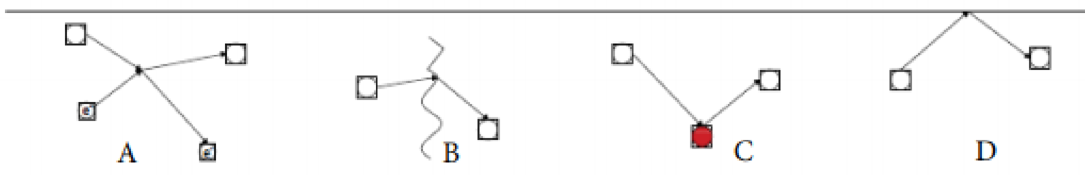

Figure 1.4 Illustrate scattering mechanisms of phonon-electron scattering, phonon-defect scattering, phonon-phonon/impurity scattering and phonon-boundary scattering respectively

collisions as opposed to aligning with the electric field, resulting in alignment with the electric field dissipating heat to lattice. This raises the lattice's local temperature and leads to sub-optimal efficiency of electronic devices. Owing to the higher concentration of charge carriers, the probability of this form of scattering is greater when the material is heavily doped. Then more heat dissipation from the energized phonons is induced by other scattering events not involving charge carriers. Boundary dispersion is dependent on surface roughness, and in low-dimensional nanostructures, it is especially important. Owing to the presence of grain boundaries, vacancies, or other deformities in the crystalline lattice, defect scattering occurs. Other phonons or impurity atoms of different sizes can also disperse phonons, especially in alloys and doped materials [9].

1.4.3. Energy Dissipation and Transport in Nanoscale Devices

The thermal conductivity of a particular material is heavily dependent on the mean free path of its energy carriers. For this reason, scattering mechanisms are extremely critical for thermal conductivity, restricting the mobility of the carrier. The thermal conductivity is called intrinsic, when constrained by the anharmonicity of the crystal lattice. When the crystal is perfect, without defects or impurities, the intrinsic limit is reached, and phonons can only be spread by other phonons [15]. The material would have an infinite thermal conductivity if no anharmonicity were present. When mainly restricted by external effects, such as phonon-boundary or phonon-defect scattering, thermal conductivity is extrinsic [16]. If there were no anharmonicity, the material would have an infinite thermal conductivity.

When mostly constrained by external effects, such as phonon-boundary or phonon-defect scattering [16], thermal conductivity is extrinsic. Thermal conductivity is significantly reduced by dispersion from borders in nanostructures that have a higher surface-to-volume ratio than microstructures or bulk materials, and the role of localized impurities and variations in sizes is also important, causing extrinsic effects to dominate. Phonon-boundary scattering, phonon-defect scattering, phonon-phonon scattering /impurity phonon-electron scattering, which is just a few times thicker than an atomic layer, often affects thermal conductivity interactions with the atmosphere for two-dimensional materials such as graphene or transition metal dichalcogenide (TMDC) [17]. When the device's characteristic length L is substantially larger than the mean free path, a considerable number of scattering events are encountered by phonons and a substantial amount of heat is dissipated to the lattice. If the size of the system is in the same order as the mean

free path (usually in tens of nanometers), there are less scattering events for phonons, with some traveling without scattering. In the quasi-ballistic transport, thermal conductivity is higher and local temperatures in the device are lower in this case given that the mean free path remains unchanged, since the phonons can transport energy away from the generation region more effectively without dissipating it to the lattice. In ballistic transport, $L \ll \lambda$ no major dispersion. As a consequence, without heating up itself, the substance tends to conduct electricity. Using a simplified 2D interface representation, Figure 1.5 shows the three distinct transport modes. Power dissipation in nanoscale circuits is calculated by two components: the dynamic power used for charging and discharging the load during switching and the static power consumption resulting from the current leakage. With the voltage overdrive, the leakage part scales exponentially, is very sensitive to changes in the threshold voltage, and is indirectly dependent on the total power dissipated as it is a strong temperature function [18], [19], [20]. Due to short channel effects such as drain induced barrier reduction, the downscaling of dimensions and voltage therefore allows sub-threshold leakage more significant (where the drain is close enough to gate the channel and turn on the transistor prematurely). In turn, the efficiency and demand-driven miniaturization trend that has led to a higher chip densities have resulted in unprecedented levels of dissipation of power and temperature.

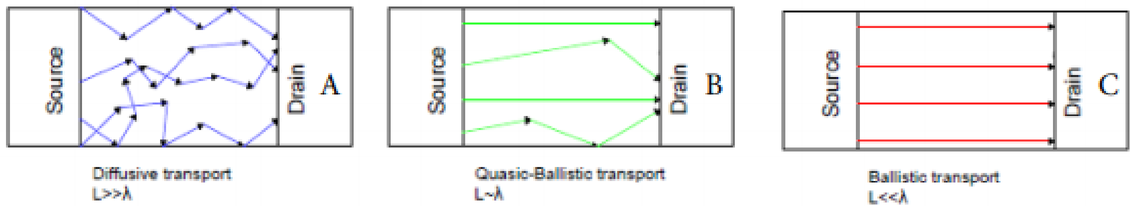

Figure 1.5: Illustration of transport mode classifications based on device size relative to mean free path.

In micro and nanoscale electronic devices, thermal conductivity is substantially lower than the bulk conductivity value of the material since increased boundary containment results in a decrease in the mean free path of the carrier [21]. In addition, the increased density of power associated with a smaller device dimensions contribute to higher local temperatures. With rising temperatures, the thermal conductivity of a semiconductor usually decreases (except at very low temperatures where an initial region of increasing thermal conductivity is observed) due to increased vibrational movement of the lattice atoms, which impedes the motion of the lattice atoms of energy carriers

[22]. The reduction in thermal conductivity and the rise in local temperatures contribute to each other in the cyclic chain in the absence of a correctly engineered cooling mechanism, resulting in a thermal runaway and breakdown.

1.5.Nanoscale Heat Conduction Models

Having identified the important role of Joule heating in hindering the efficient performance of electronic devices, the simple physical processes that regulate it, and how recent technical advances exacerbate the problem, it is now necessary to review the methods developed in literature that are used to research this phenomenon and help to develop solutions to the challenges presented by it.

1.5.1. Experimental Methods

With a decline in unit measurements, the difficulty inherent in the use of experimental methods for studying Joule heating increases. The deposition of thin films on substrates in modern electronic devices makes it impossible to reliably calculate the thermal conductivity of the cross-plane film [23], [24] and involves the use of methods that work on a thermal conductivity system. Time scale of picoseconds to perform surface-sensitive measurements and remove the effect of the substrate heat conduction [25]. Several experimental methods are able to reliably provide knowledge about the modes of the phonon and conductivity of the material. The benefit of experimental techniques is the absence of the need to simplify the assumptions associated with analytical and numerical models, but they are expensive and time consuming, particularly with the fine precision involved in the preparation of measuring methods. Raman spectroscopy is a non-destructive optical technique which determines the modes of vibration of a device by using the inelastic dispersion of photons with phonons. A change in the frequency of the incident photons released from a high intensity laser source [26] is caused by the vibration energy of the lattice atoms. Information on the intensities and wavelengths of the dispersed light is shown as several peaks in the Raman spectrum, each peak corresponding to a specific chemical bond and vibration mode [27]. The technique can provide information about the phonon dispersion, lattice anharmonicity, phonon population, phonon lifetime and temperature distribution of the sample [28]– [29]. The time-of-flight technique analyzes the present signal caused by the motion of ionizing radiation-generated charge carriers as a way of calculating the time taken by these charge carriers to cross a known thickness sample under the control of an electric field applied.

[30] [31]. The transit time and sample thickness together provide information on the carrier transport characteristics of the semiconductor sample, such as the speed of drift, the stability of the carrier and the trapping of the carrier, as well as their reliance on the electric field and temperature [32]- [33]. This, in essence, helps the electrical and thermal conductivity of the material being studied to be calculated.

Microscale thermometry techniques are capable of calculating longitudinal scales in the order of the mean free paths of energy carriers, enabling temperature mapping at a high spatial precision over the surfaces of micro and nanoscale devices [34]. Scanning thermal microscopy uses a sharp-tipped probe to calculate the local surface temperature, and calculating the difference in local temperature subject to a known heat flux will deduce the thermal properties of electronic equipment and recognize localized hotspots and defects [35]- [36]. By depending on optical reflectance, scanning optical thermometry tests the local temperature and uses lasers as sources of periodic heating [37]. It is best suited to quantify the propagation of temperatures resulting from electrical heating in micro and nanoscale devices because, unlike scanning thermal microscopy, it does not rely on the absorption of heat through a solid sensor and hence avoids the time delay associated with it [36]. Picosecond reflectance thermometry uses small laser light pulses separated into two paths of beams with a mechanical delay between them [31]. Energy from the first beam induces a temperature spike near the surface of the sample, with the energy of the second beam [36], [37]- [38] being determined by the decay of this temperature change.

1.5.2. Analytical Methods

A heat conduction model with an acceptable level of detail for the length scale and temperatures involved must be chosen in the Joule heating analytical and computational analysis, as well as for the theoretical understanding of experimental findings. Several separate models are commonly used in literature to measure Joule heating, with their own sets of assumptions, and are specific to a particular variety of conditions, with experimental findings acting as the accuracy benchmark. Provided the advances in computational technology, numerical simulations with a variety of visualization and post processing effects produce fast results and are capable of managing complex geometric structures with reasonable precision.

The typical heat diffusion equation, expressed as [20]:

$$C\frac{\partial T}{\partial t} = \nabla.(\varkappa \nabla \mathbf{T}) + \mathbf{Q}''' \quad (1.5)$$

Where $\mathbf{Q}'''$ is the volumetric heat generation rate, is based on Fourier's law. Thus, owing to its failure to account for carrier scattering events and to capture heat transfer processes at short time and length scales, it is only valid at the continuum scale. Similarly, the dissipated power measurement in a mesoscopic electronic system is measured as:

$$Q = IV = I^2R \quad (1.6)$$

(Where Q is the dissipated power, I is the current flowing through the device, is the V potential difference across its terminals and R is the electrical resistance of the device) will result in an overestimation. Unlike at larger length scales, the energized carriers do not undergo a sufficient number of scattering events to fully dissipate their energy to the lattice before exiting modern devices, which operate in the quasi-ballistic regime [39].

Due to the nanoscale measurements involved, the low number of carriers present in total in small devices makes the location of each carrier, dopant and impurity critical for the efficiency of the system and the use of average densities and statistics contributes to measurement inaccuracies [40]. One of the first to predict that the differences of dopant atom were Keyes [41]. Concentrations in the transistor channel area may lead to fluctuations in the threshold voltage of the system.

The phonon mean free direction, the phonon wavelength and the lattice spacing are important characteristic length scales that decide the applicability of different models to the analysis of Joule heating, as these help to define whether the phonons can be modeled as particles or waves [42]. The Debye temperature, which is the temperature at which the highest vibration mode of a crystal is excited, serves on the temperature scale as a similar characteristic measure [43]. For silicon, the Debye temperature is 645 K [44], the acoustic phonon means free path is around 300 nm [45] and the phonon wavelength is 1 nm at room temperature [46]. For indium arsenide Debye temperature is 270 K.

For $T < \theta_D$, the Fourier equation is no longer valid for length scales shorter than the acoustic phonon mean free path, and the phonon Boltzmann transport equation (BTE), which treats phonons as semi-classical particles, must be solved instead. To account for the granularity, the BTE for each phonon mode must be solved. The quantum mechanical behavior of phonons

becomes important at even shorter length scales, below the phonon wavelength, and/or with $T \ll \theta_D$,and lattice dynamics equations are used[47]-[48]. However, the measurements and temperatures involved in modern electronic devices are not so limited as to necessitate quantum mechanical modelling, and semi-classical methods suffice.

In its self-consistent formulation of phonon and electron transport, the Boltzmann transport equation integrates the effects of external electric fields, electron-phonon interactions, phonon decay, and multiple scattering events [49]. Based on the fundamental assumption that an ensemble of carriers has a statistical distribution function $f(\mathbf{r}, \omega, t)$ that depends on time t, position vector r, and phonon frequency ω, and is a measure of the average particle (electron or phonon) occupation in the vicinity of the location described by position vector **r,** at time t, and that each carrier has a spatial and momentum coordinate. In order to model carrier transport to a desired degree of precision, the Boltzmann transport equation (BTE) applies the principle of charge conservation by equating the cumulative rate of change in time of the distribution function to the change due to different scattering mechanisms. [4], [50].

Since phonons have no charge, they do not interfere with any applied potentials and are only susceptible to anharmonic decay by interactions with the atomic potential [51]. As a result, in the phonon BTE, which can be articulated as [49], [50], [51].

$$\frac{\partial f}{\partial t} + \upsilon \cdot \nabla f = \left(\frac{\partial f}{\partial t}\right)_s + \left(\frac{\partial f}{\partial t}\right)_g \quad (1.7)$$

The only change in the distribution function is due to the motion of phonons in real space, in which υ is the phonon velocity vector. The rate of change in phonon occupation due to scattering events is described by the first word on the right-hand side (which include anharmonic phonon decay). Furthermore, depending on the energy transfer involved, a phonon is released or consumed every time an electron transfers between two states, which is accounted for by the second word on the right-hand side. The BTE needs the evaluation of the scattering term, and while there are methods for doing so by applying an integral in wave vector space to all scattering processes, solving this integral-differential form is a difficult task [52], [53]. As a result, the relaxation time approximation is frequently used in the literature to model the scattering term, with the rate of change of phonon occupation due to scattering expressed as [54], [55]:

$$\left(\frac{\partial f}{\partial t}\right)_s = \frac{f_0 - f}{\tau_{ph}} \quad (1.8)$$

Where f_0 is the equilibrium phonon distribution and τ_{ph} is the relaxation time : the time it takes for phonons to relax to equilibrium as a result of all scattering processes combined, as a function of position and momentum. The equilibrium phonon distribution can be calculated using Bose-Einstein statistics as [56]:

$$f_0 = [\exp\left(\frac{h\omega}{k_B T}\right) - 1]^{-1} \quad (1.9)$$

Where k_B is the Boltzmann constant, while the relaxation time is related to the phonon mean free path as $\lambda = \upsilon\tau_{ph}$. Substitution of Eq. 1.8 in Eq. 1.7 and integration over the phonon frequency and density of states allows for the BTE to be expressed in terms of the phonon energy density u as [56]:

$$\frac{\partial u}{\partial t} + \boldsymbol{v}.\nabla u = \frac{u_0 - u}{\tau_{ph}} + Q'' \quad (1.10)$$

As Eq. 1.10 shows, solving the BTE for the conduction problem also necessitates modelling of the device's phonon dispersion, electron energy bands, phonon transport, and volumetric heat production. The following section discusses how to evaluate the heat produced by electron-phonon scattering in an electronic system using existing methods.

1.6. Nanoscale thermal analysis models

The inaccuracy of using the expression of Eq. 1.6 to measure heat generation in a micro or nanoscale electronic system has been briefly discussed previously. The failure to forecast the non-uniform spatial distribution of heat generation and thereby recognize crucial design defects, the lack of knowledge regarding the contribution of individual phonon modes to heat generation, and the inability to account for hot energy carriers travelling into the unit contacts and dissipating heat there are all flaws in that model [54]. Meanwhile, solving the BTE directly is a time-consuming operation, and analytical solutions are only available for basic heat conduction problems [53]. The drift-diffusion, hydrodynamic, and Monte Carlo simulation methods, which are focused on the numerical solution of the BTE, are other well-established ways to calculate heat generation in electronic devices.

1.6.1. Hydrodynamic Method

The BTE is used to derive the hydrodynamic model, which was first used by Stratton [57] and Blotekjaer [58]. The basic equations of this model are the zeroth, first, and second moments, which represent the electron charge, momentum, and energy conservation, respectively [59]:

$$\frac{\partial \mathbf{n}}{\partial t} + \nabla . (n v_d) = \left(\frac{\partial n}{\partial t}\right)_c \quad (1.11)$$

$$\frac{\partial \mathbf{p}}{\partial t} + \nabla . (v_d\, p) = -enE - \nabla(n k_B\, T_e) + \left(\frac{\partial p}{\partial t}\right)_c \quad (1.12)$$

$$\frac{\partial w_e}{\partial t} + \nabla(w_e\, v_d) = -en v_d\, \mathbf{E} - \nabla(v_d\, n k_B\, T_e) - \nabla Q + \left(\frac{\partial w_e}{\partial t}\right)_c \quad (1.13)$$

Here, T_e is the electron temperature, $\boldsymbol{p}$ is the electron momentum density, w_e is the electron energy density, v_d is the electron drift velocity, and the subscript c indicates terms that change due to collisions, which can be rewritten using the relaxation time approximation. Furthermore, in the case where electrons are the majority charge carriers, the volumetric heat generation is evaluated as:

$$Q''' = \frac{3}{2} k_B \frac{n(T_e - T)}{\tau_e} + (R - G)\left[E_g + \frac{3}{2} k_B (T_e + T)\right] \quad (1.14)$$

Where T is the lattice temperature, and τ_e is the electron energy relaxation time. In this case, the holes are assumed to be in thermal equilibrium with the lattice.

While the drift-diffusion model has a similar mathematical framework to the hydrodynamic model and both are obtained by applying the formula of moments to the BTE, the latter is more detailed because it uses three moments rather than two in the former. The benefit of the hydrodynamic approach is that in this model, the majority carrier temperature is not presumed to be equal to the lattice temperature, allowing for more precise predictions of carrier concentration, velocity, and energy, particularly in the vicinity of strongly peaked electric fields

[60]. The added computing expense associated with the extra equation is compensated by the increased precision. Despite the enhanced carrier transport handling, this system is still unable to differentiate between the contributions of individual phonon modes to heat production, and the use of a single averaged carrier temperature T_e and relaxation time $\tilde{\iota}_e$ implies that the energy based scattering speeds in mesoscopic devices are not measured to a sufficient degree of precision [61]. Furthermore, during system simulation, the truncation of the model to a finite number of moment equations during derivation from the BTE causes spurious peaks in carrier velocity profiles in the vicinity of peaked electric fields, which are minimized when a larger number of equations is used [62]–[63].

1.6.2. Monte Carlo Simulations

The Monte Carlo (MC) method is a mathematical technique for predicting the probability of different potential results in a problem with random variables and risk evaluation. When allowing for the interdependence of such parameters, event outcomes are drawn separately and at random from a set weighted by pre-defined probabilities. The results of MC simulation are never exact due to the stochastic nature of the operation, but they do lie within defined intervals with assigned probabilities, and using a larger sample size raises confidence in the results. In addition to being used to solve purely statistical problems, the MC approach can also be used to solve a well-defined system of mathematical equations, or a combination of the two, as in the case of semiconductor device simulation [64].

The MC process, when used to perform carrier transport in semiconductor devices, utilizes a variety of super-particles to represent classes of mobile charge carriers inside the unit [64]. The motion of these particles under the control of externally applied electric and magnetic fields is studied after attributing energy and momentum information to each particle depending on the initial conditions. The pre-defined probabilities of the different scattering processes are used to calculate the length of each particle's initial free flight in the presence of an external force, after which it is subjected to a randomly chosen scattering phenomenon that reorients the particle momentum [65], [66].

The MC method offers precise details about phonon generation and the exchange of energy between electrons and phonons due to the individual particle-tracking aspect of the simulation and the deliberate integration of scattering phenomena, which is significant since various phonon modes with different group velocities have differing contributions to heat generation and present

confinement in an electronic device. The sum of the energies of all phonons released minus the energies of all phonons consumed per unit volume over a given simulation time t_{sim} can be used to measure the volumetric heat generation rate at steady state [67].

$$Q''' = \frac{1}{t_{sim}} \Sigma(h\omega_{emitted} - h\omega_{absorbed}) \tag{1.15}$$

1.6.3. Drift-Diffusion Method

The drift-diffusion method, which usually requires simultaneous solution of the current density, continuity, and Poisson equations, has been widely used in the literature to solve the BTE and predict carrier transport characteristics of electronic devices [1]. The current density equation – which relates electric current to carrier concentration – for electrons can be obtained from the BTE for a three-dimensional case using the formula of moments and a relaxation time approximation as [2].

$$J_n = q\mu_n \left(-n\nabla V + \frac{k_B T}{q} \nabla n \right) \tag{1.16}$$

Where q is the absolute value of the electronic charge, μ represents the field-dependent mobility, and k_B is the Boltzmann constant. Here current density $\boldsymbol{J}$ in an electronic device (contributed to by both electrons and holes) is also related to the applied electrical field $\boldsymbol{E}$ through the electrical conductivity σ (which is the reciprocal of resistivity ρ) as [3].

$$\boldsymbol{J} = \sigma \boldsymbol{E} \tag{1.17}$$

Electric current must also obey the continuity equation, which is expressed by the zeroth moment of the BTE, since electrical charge must be conserved. The continuity equation can be written as equation [2].

$$\nabla \cdot J_n = qU(n, p) + q\frac{\partial n}{\partial t} \tag{1.18}$$

Where $U(n, p)$ represents the net generation-recombination rate, which is a function of the local electron and hole concentrations (n and p, respectively). Since this continuity equation is used in the drift-diffusion model, the overall charge within the device, as well as the charge entering and exiting the device, is conserved. Furthermore, it guarantees that the numerical solution domain

maintains a positive carrier density. The hole current density is described by equations similar to equations 1.16 and 1.18.

It is necessary to solve the Poisson equation in combination with the transport model in order to reliably determine the time evolution of the spatial electric field distribution in an electronic system [4], [5]. The electrostatic potential is related to the net charge density by the Poisson equation [6]:

$$\nabla^2\phi = \frac{q}{\epsilon_s}(n - p - N_D^+ + N_A^-) \quad (1.19)$$

Where ϵ_s is the dielectric constant of the semiconductor, and N_D^+ and N_A^- are the concentrations of the ionized donors and acceptors respectively. Since all four charge carrier densities are functions of location, the distribution of electrostatic potential can be changed over the entire system geometry to keep up with charge carrier motion over time.

The volumetric rate of heat generation in an electronic system can be measured using the drift-diffusion method until the electric current flowing through an electronic device as a result of a specific applied potential difference has been determined [7]:

$$\mathrm{Q}''' = \mathbf{J}.\mathbf{E} + (\mathrm{R} - \mathrm{G})(E_g + 3k_B T) \quad (1.20)$$

Where the first time on the right-hand side is the dot product of the current density **J** and the electric field **E** , and represents the volumetric rate of Joule heating. The second term, in which E_g is the band gap energy, represents the heat generation rate associated with the non-radiative electron and hole generation (G) and recombination (R) rates, which result in heat dissipation to the lattice either directly or via phonon emission from an excited charge carrier [16].

$$\mathbf{J} = \mathbf{q}\mathrm{n}\bar{\mathrm{v}} \quad (1.21)$$

Where q is the elementary charge of an electron, n the electron density and $\bar{\mathrm{v}}$ is the average electron velocity.

$$\frac{\partial T}{\partial t} = \frac{1}{\rho C}(k\nabla^2 T + Q''') \quad (1.22)$$

Where k is the thermal conductivity, ρ is the density and C is the specific heat capacity of the constituent material. The existence of spatial heat generation knowledge provided by the presence of the electric field and current density vectors in the mathematical formulation is an advantage given by this method over the expression of Eq. 1.22. However, since energized electrons travel a few mean free paths until they are able to completely dissipate their energy to the lattice by phonon emission.

Well-established models such as Coventerware and COMSOL Multiphysics that are known for their adequacy in modeling gadgets have too applied/implemented these strategies in their work. Subsequently these methods hold conspicuous esteem for advance investigate. Moreover, these computer program suites give different progressed highlights and were created considering broader utilization. These program suites require a significant sum of computation control and offer a soak learning bend. Be that as it may, the magnificence of COMSOL Multiphysics lies within the COMSOL Server with Java application programming interface, which empowers get to toward COMSOL's modeling capabilities with customized interfacing.

1.7. Research Objectives:

Having developed how the need for better processing power and the pattern of miniaturization necessitate the study of Joule heating in electronic devices, and having defined the various methods used to investigate the effect of this phenomenon, this work aims to:

1. Examine heat dissipation in nanoscale electronic devices using Joule heating module in COMSOL Multiphysics package for simulations. This study will not attempt to create a new Joule heating model; instead, a set of well-established models created by previous researchers will be compared and tested for fitness of function.
2. Validate simulation parameters such as the hot spot location on nanowire, measure the change of temperature by changing electric current, and study the overall effect of changing substrate material on temperature of semiconductor nanowire while maintaining the same operating conditions during simulation.
3. Investigate the effects of crucial parameters (such as electric field power, temperature change over changing current etc.) on the output of nanoscale devices.

Following a review of the different methods for studying Joule heating in electronic devices (as mentioned in the previous chapter), the numerical Joule heating in COMSOL Multiphysics software was chosen for the current analysis due to its superior precision over other numerical techniques. COMSOL Multiphysics is a multi-physics simulation and finite element analysis program that runs on any computer. It supports both traditional physics-based user interfaces and coupled partial differential equations systems (PDEs). For electrical, mechanical, fluid, acoustics, and chemical applications, COMSOL offers an IDE and a single workflow. It has its own materials library and different modules.

Joule heating in COMSOL Multiphysics is a module in which is used to model resistive heating and dielectric heating in which inductive effects are negligible i.e., skin depth is larger than the studied device [5]. An Electric Currents interface and a Heat Transfer in Solids interface are used in this multi-physics interface. The electromagnetic power dissipation is added as a heat supply by the multiphysics couplings, and the electromagnetic material properties can be affected by temperature. Stationary modelling, frequency-domain modeling for the Electric Currents interface, stationary modeling for the Heat Transfer in Solids interface, called frequency-stationary and frequency-transient modeling, and time-domain modelling are provided in all space dimensions, depending on the licensed products. Electric Currents and Heat Transfer in Solids interfaces are applied to the Model Builder when a predefined Joule Heating interface is added from the Heat Transfer>Electromagnetic Heating branch of the Model Wizard or Install Physics windows. The Multiphysics Branch has also been included, which contains the Multiphysics coupling function Electromagnetic Heating by default.

The Electric Currents interface calculates electric field, current, and potential distributions in conducting media under conditions where inductive effects are almost negligible, i.e., where the skin depth is much greater than the system being tested. Time and frequency domain formulations that account for capacitive effects are also offered, depending on the approved goods. Modeling heat transfer by conduction, convection, and radiation is feasible with the Heat Transfer in Solids interface. On all domains, the Heat Transfer in Solids model is active by domains. Other domain styles, such as a fluid domain, may be used using the same features. In solid domains, the temperature equation refers to the differential version of Fourier's law, which can require additional contributions such as heat sources.

As predefined couplings, such as Joule Heating, are used to incorporate physics interfaces, basic configurations are used for the physics interfaces and coupling functions.

Methodology

Upon investigating the various methods available to study Joule heating in electronic devices, as described in the previous chapter, the numerical drift diffusion model was chosen for the present study due to the better accuracy it offers over other numerical techniques. The drift diffusion model used in COMSOL Multiphysics allows for flexibility in the descriptions of the charge density, iso-thermal contours, temperature profile and give variety of materials to simulate through simplifying assumptions that are applicable to a certain range of operating conditions. Furthermore, the method allows for simulations to be performed at conditions that are difficult to be maintained in physical experiments, for the investigation of the theoretical performance of materials, and for the identification of the effects of material properties on the observed phenomena. This chapter describes the methodology adopted by the present study in detail, and includes a comparative discussion of the different drift diffusion models that have been used by previous researchers.

A numerical solution of the governing equations is typically sought when determining the performance characteristics of electronic devices with complex geometrical features and spatially inhomogeneous material properties, as aforementioned. The COMSOL Multiphysics software, a commercial device simulator, has been used in this study. This simulator incorporates the mathematical model required to describe electric currents, electrical heating, and heat transfer in semiconductors within its Joule Heating interface module [68], [69].

2.1 General Algorithm

The basics of the drift diffusion method as applied to various problems of interest have been covered in extensive detail in past studies [45], [46], [49], and form the basis for the development of Joule heating models with varying assumptions. Joule heating module in COMSOL Multiphysics is applicable to both steady-state and transient transport processes, although the former are less computationally demanding [51]. The simulation of time- or space-dependent phenomena require the explicit simulation of an ensemble of carriers.

The present study uses the ensemble drift diffusion approach to perform transient simulations of the joule heating in field effect transistor. Figure 2.1 presents a flowchart of the basic steps of the Joule heating implemented in the current study. Practically joule heating in nanoscale electronic devices is studied by a noninvasive optical method name micro Raman spectroscopy in which variation in the optical phonon frequency in detail downshifting of the first order Strokes Raman

band are correspond to change in temperature of nanoscale device. In COMSOL Multiphysics change in temperature is predicted by selecting a module named joule heating. In this module inductive heating is neglected by increasing skin depth of device being studied [69]. When Joule heating module is added electric current, heat transfer in solids and electromagnetic heating interface are also added with it. In electric current interface is used to compute electric field, current, and potential distribution. Current conversion equation based on Ohm's law is solved in this interface. There are two domain studies exist in Joule heating module in COMSOL Multiphysics. One is time domain and second one is frequency domain. In Joule heating or resistive heating source Q_{rh} of heating depends on which type of domain is being selected. In time domain heating source is $Q_{rh} = J.E$ and for frequency domain its expression is $Q_{\gamma h} = \frac{1}{2} R_e(J.E)$. Heat transfer interface provides features of conduction, convection and radiation for modeling devices. The temperature equation defined in solid domains corresponds to the differential form of the Fourier's law that may contain additional contributions like heat sources.

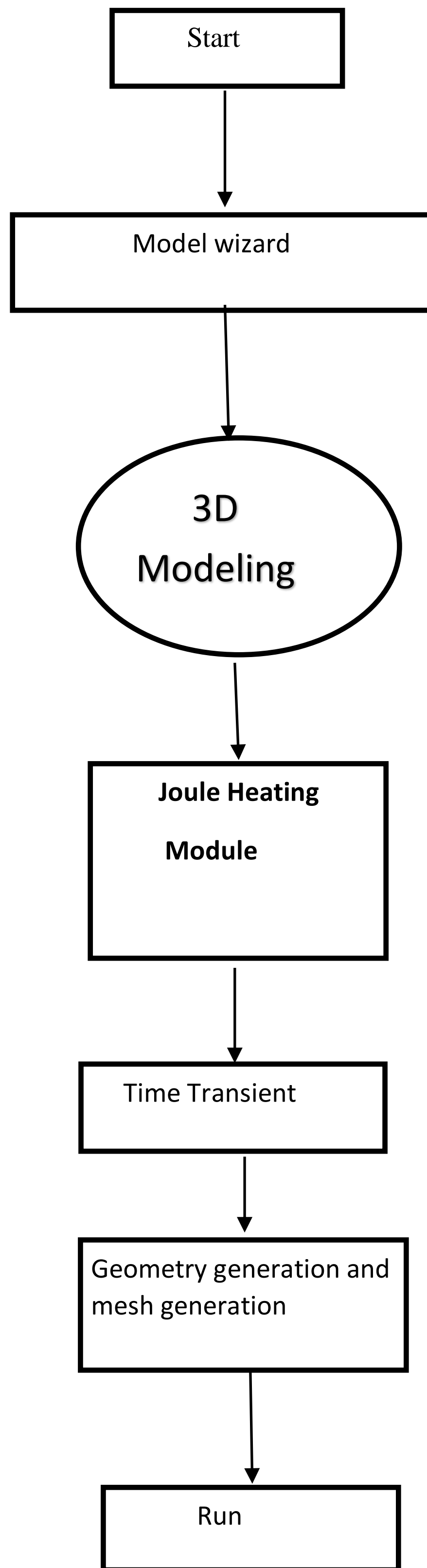
Start
Model wizard
3D
Modeling
Joule Heating
Module
Time Transient
Geometry generation and
mesh generation
Run

Fig 2.1: Flow chart of COMSOLE Multiphysics simulation used in this study

2.2 Joule heating in Literature

Nanowires (NWs) are a modern applied material that has sparked renewed interest in the rapidly growing field of nanotechnology. Nanowires ware used to investigate single-electron transistor phenomena [70] and quantum confinement properties [71, 72] in basic mesoscopic physics. These quantum confinement effects, in which charge carriers, such as electrons or holes, are confined in the lateral direction of these quasi one-dimensional nanostructures, are predicted to play a key role as the nanowire diameter reaches the carriers' de Broglie wavelength. This will cause a hindrance to flow of charge carriers. This hindrance increases the temperature of electronic device to safe limit and main reason of its failure. This complexity of nanowire structures has prompted different groups of researchers to develop their own numerical simulations with varying assumptions to describe the confinement effect involved in nanowire. Two different analytical approximations—the Raman spectroscopy and the finite element tools like COMSOL Multiphysics—have been widely used in literature as alternatives to the full band model that simplify the quantum confinement description and reduce computational costs.

In the study of Joule heating and carrier transport in electronic devices, consideration of the phonon dispersion is also important, since interactions with phonons can cause electrons to transition between states in different conduction band valleys. As made evident by Eq. 1.17, lattice self-heating occurs through electron-phonon scattering, which allows the electrons accelerated by externally applied electric fields to dissipate their energy and return to equilibrium as they leave the device [73].

Lugstein *et al*. studied Joule heating and rise the temperature of nanowire through Raman spectroscopy and also with COMSOL Multiphysics[74]. They measure the downshifting of first-order Stokes Raman band and find its relation by applying electrical bias to find the change in temperature of Germanium nanowire. Results of both techniques were compared to find the rise of temperature. Different configurations like bare Germanium nanowire on Silicon di oxide and Germanium nanowire connected through contact pads placed on silicon di oxide at same power were studied. Current is ramped every 15 μs to 50 amperes to maximum value.

Fangohr *et al*. [75] performed same work on COMSOL Multiphysics. They studied joule heating on nanowires, current density distribution model to find the temperature distribution due

to current. Within the nanowire and the substrate, the spatial current density distribution, related heat production, and heat diffusion are all modelled. They investigate various nanowire and constriction geometries, as well as various substrates, including (thin) silicon nitride membranes, (thick) silicon wafers, and (thick) diamond wafers. In 3 dimensional substrates the substrate thickness greatly exceeds the nanowire length three different regimes of heat propagation through the substrate is identified. The first region is the region in which nanowire temperature increases logarithmically with time. In second region nanowires temperature remain constant because heat front hemispherical moves away toward substrate and reaches the boundary of substrate material. In third region substrate and nanowire temperature increase very rapidly.

Ramos *et al*. [89] also studied joule heating in a ferromagnetic nanostripe with a notch at its center. They find when an electric current is applied a temperature rise pulse is injected in a ferromagnetic nanostrip. They first experimentally generate that pulse then correlate it through simulation on COMSOL Multiphysics at same conditions. The best match for these experimental curves was found by including the electrical resistivity of nanostripe and the thermal conductivity of the substrate change with temperature (SiO2). They find increased current density in the notch and the lower interface thermal resistance, the temperature in the notch can rise significantly, resulting in a huge horizontal thermal gradient. The main difference in Fangohr *et al*. [75] work is they assume perfect thermal contact between nanostrip and substrate while Ramos *et al* includes thermal resistance interface to calibrate $\boldsymbol{T}(\mathrm{t})$.

2.3 Boundary Conditions

Three-dimensional simulation is performed in this work. In which Copper is behaves like a connecting pad and there are region of Cu_3Ge layer is formed. The layer has specific resistivity of $34\mu\Omega cm$ at room temperature. Electrical conductivity of Germanium nanowire is calculated first we calculate the resistivity of nanowire Lugstein *et al*. [74] use the electrical resistance of Germanium nanowire $6.5M\Omega$ and we have length of nanowire $1522nm$ and cross-sectional area of nanowire varies as the radius of nanowire varies from 10nm to 28nm .By using equation below:

$$\rho = \mathrm{R.A/L} \tag{2.1}$$

Where whole nanowire field effect transistor is insolated so that no heat can flow in or out. Heat only flows downward from channel to substrate region through conduction. Room temperature is set as initial temperature and initial voltage is zero. Electric current is ramped to maximum value.

.

Joule heating in current carrying nanowire

3.1 Introduction

Having studied the heat generation and effect of substrate material in Joule heating in nanowire field effect transistor under the influence of an externally-applied electric field, as discussed in the previous chapter, the same numerical methodology was extended to the investigation of the electrical and thermal properties of simple nanowire field effect transistor. Nanowire is frequently used as channel material in field effect transistors [76].

Figure shows a schematic representation of the 3D nanowire field effect transistor device investigated in this study. The channel length i.e., length of nanowire is kept constant while the electric current, nanowire's material, nanowire diameter, substrate thickness, substrate and nanowire's configuration are varied for the purposes of this study.

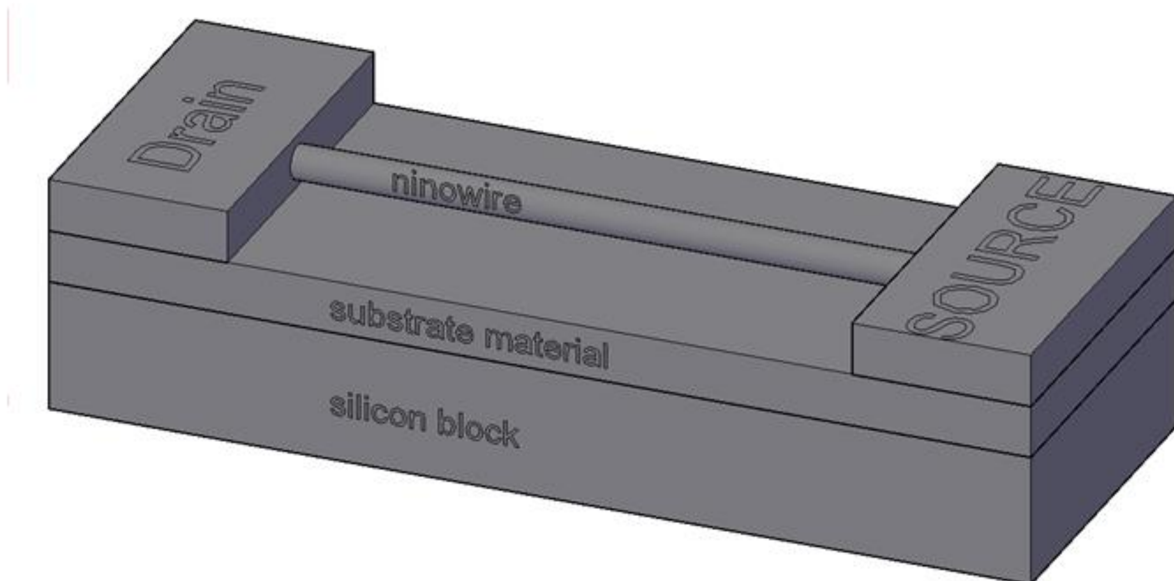

Figure 1: Nanowire supported on substrate

The dimensions of nanowire field effect transistor are given below. The applied voltage, substrate thickness and device dimensions are both expected to have a significant role in the determination of Joule heating and velocities through their influence on the electric field distribution in the devices.

Dimensions	Silicon Block	Substrate material	Copper pads	Copper pads
width	3000	3000	739	739
Depth	1100	1100	1100	1100
Height	400	200	80	80

Table 1: Dimensions of blocks in nanometer(nm).

Radius	changed from 10 to 28nm
Length	1522nm

Table 2: Dimensions of nanowire.

The device geometries are created in the COMSOL Multiphysics software. This module solves the Poisson equation to update the electric potential distribution over the device geometry with the motion of the charge carriers, and both electron and hole transport is simulated through the drift-diffusion equations Materials is selected from material library. Electrical conductivity is measured through intrinsic resistance of Germanium nanowire which is 6.5MΩ [74] and its value varies when size of nanowire changes. Potential difference across the device boundaries for the Joule heating simulation is also fixed by adding terminal and ground on source and drain of device. Furthermore, a periodic boundary condition is applied to the device contacts, such that the particles escaping from one contact are reinjected with thermal energy and inwards momentum at the other contact to maintain current continuity through the device. A uniform grid, with grid independence checked beforehand, is used to study the joule heating. Different schemes of nanowire field effect transistor are studied.

3.2.Validation:

Solving problem of our interest, simulations are performed to validate the published article. The results of validation help to establish a level of confidence in the adopted methodology by confirming that the geometry and mesh information. Figure 2 shows the previous on Germanium nanowire. It shows the Joule heating produced in Germanium nanowire of 22.5nm diameter and length of 1522nm.

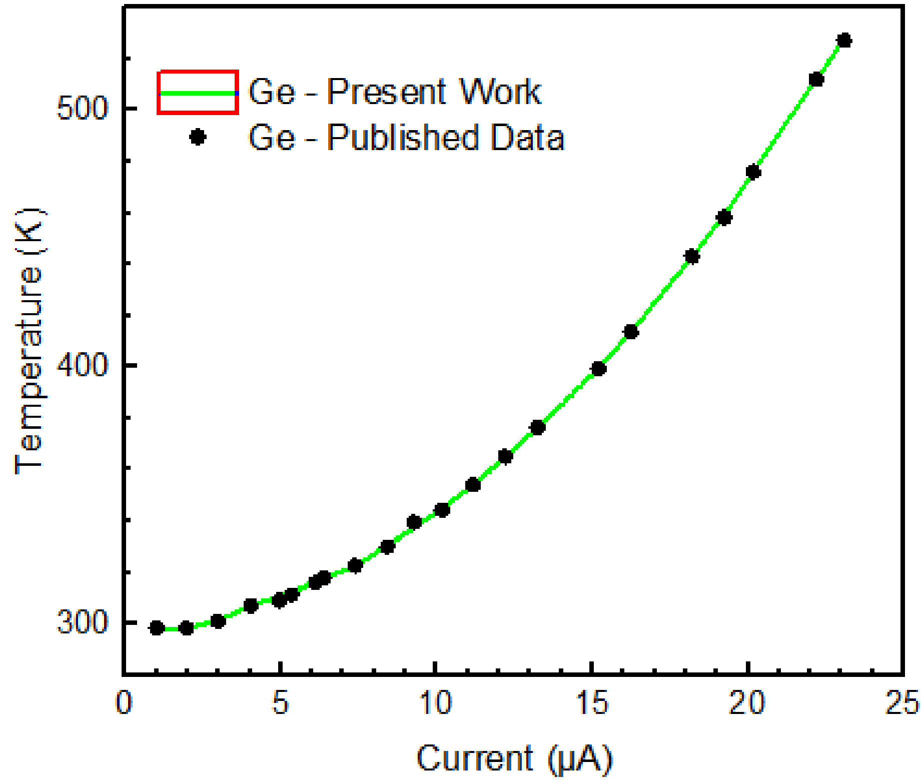

Figure 2: Validation of Joule heating produce in Germanium nanowire field effect Transistor

3.3 Mesh independence in COMSOL Multiphysics:

We perform mesh independence test in COMSOL Multiphysics by putting number of mest elements on x-axis and maximum temperature on y-axis. Our finds in this study is in start there is sudden rise of temperature and after 4×10^4 when the mesh elements increases from that number it becomes smoot after it.

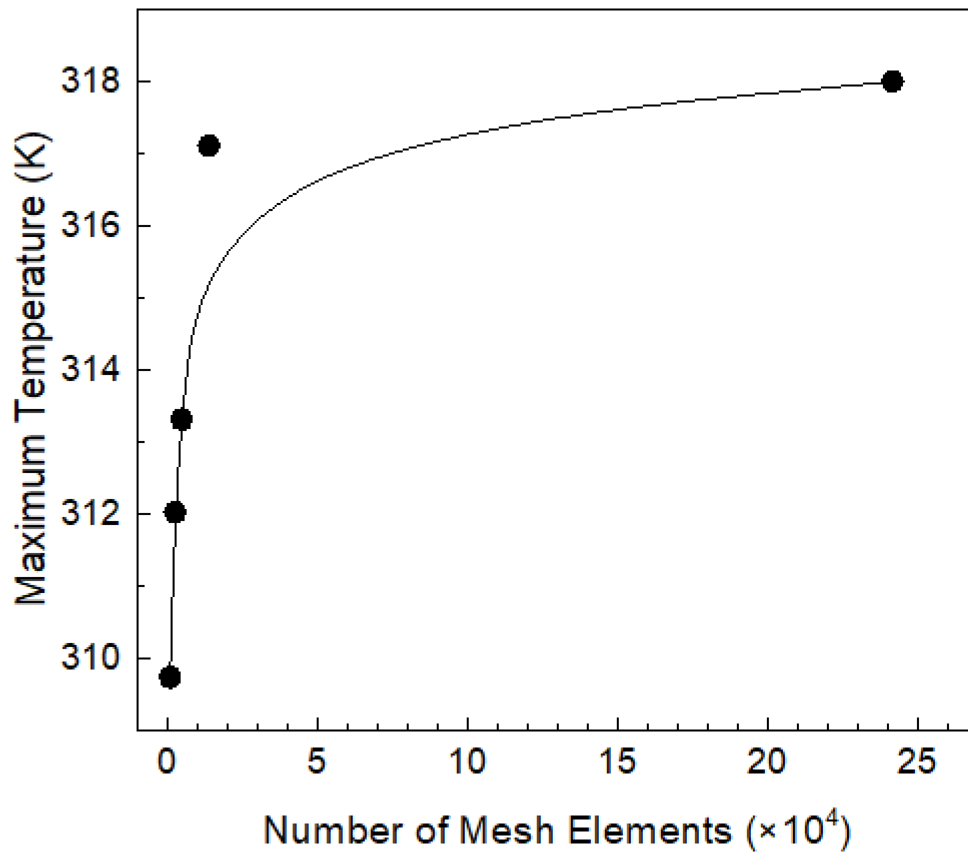

Figure 3: Mesh independence

3.4 Nanowire supported on substrate:

In order to create the device geometry nanowire supported on substrate material COMSOL Multiphysics provide different options to user i.e. either generate it on COMSOL Multiphysics interface or import it from other tools. Silicon block of 3000nm wide, 400nm height and 1100nm deep is lower most block. The upper block is also called substrate block of nanowire field effect transistor. Its dimensions are 3000nm long, 1100nm deep and 200 highs. Nanowire has a varying radius which varies from10nm to 28nm while length of nanowire is 1522nm. The source, channel and drain are created as separate intervals of same dimensions from left to right by providing

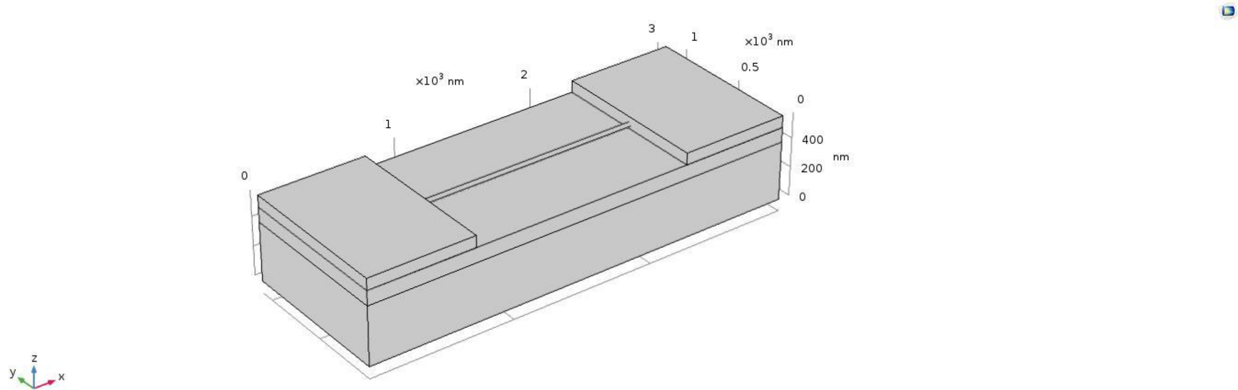

Figure 4: Snapshot of the geometry of a 1522 nm channel 3D nanowire supported on substrate created using the COMSOL Multiphysics software.

the 739,1100 and 80nm width, height and depth respectively. After creating, a union at their mutual interfaces. Germanium and Indium Arsenide nanowire is supported on Silicon di Oxide, Silicon Nitride and Aluminum Oxide substrate.

3.3.1. Temperature distribution of supported nanowire of 28 nm diameter and 1522 nm long:

The temperature profile is shown in Figure 3 which indicates that, the center is heated, while contacts remain at room temperature. Charge carrier density is maximum at the center of nanowire channel and at that point carrier interaction is maximum *i.e.* quantum confinement, sharp features in the one-dimensional density of states [77], increased boundary scattering of electrons and phonons [78], and modified electron–phonon and phonon–phonon scattering. These scatterings are in the same region as the locations with the highest magnitude of ∇E^2. This cause center of nanowire to be heated [79], [80]. This behavior can be explained by the heating power ($P = I^2R$) provided at hot-spots, which is dependent on the current passing through the gap and the resistance to electrical conduction. Current density and area available for current flow will determine how much current passes through a gap area [81]. The heating in nanowire will essentially be determined by the strength of local electric field and transversal distance.

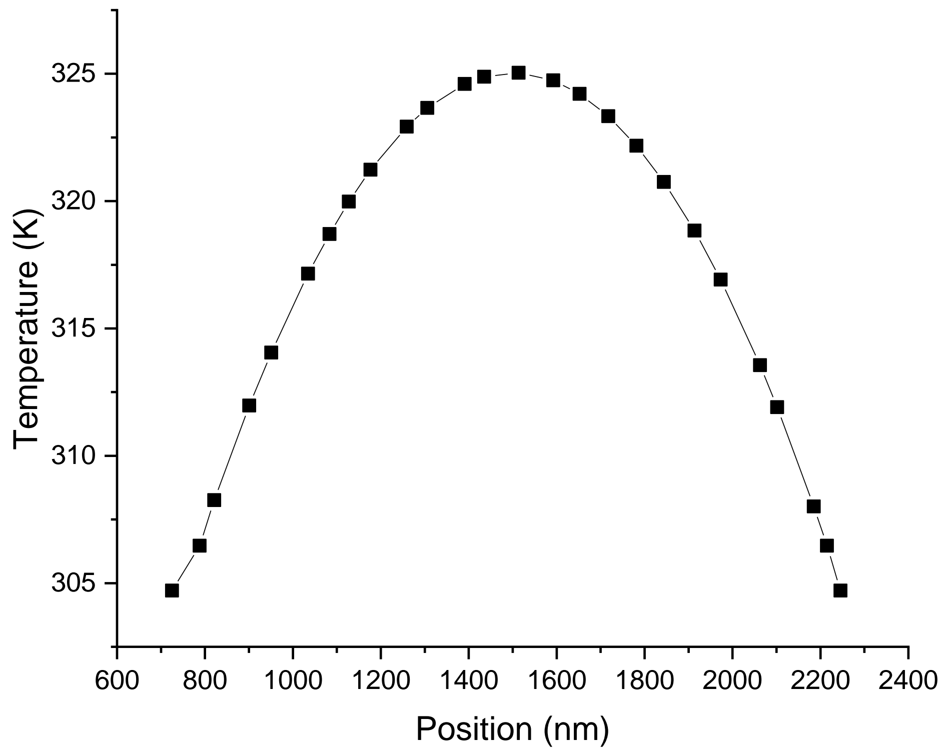

Figure 5: Temperature profile of 22 nm wire at 10 μA current.

Charge trapping at the dielectric is minimum or absent, which enables uniform power distribution along the device. Same profile is found for different diameters of 28 nm to 10 nm.

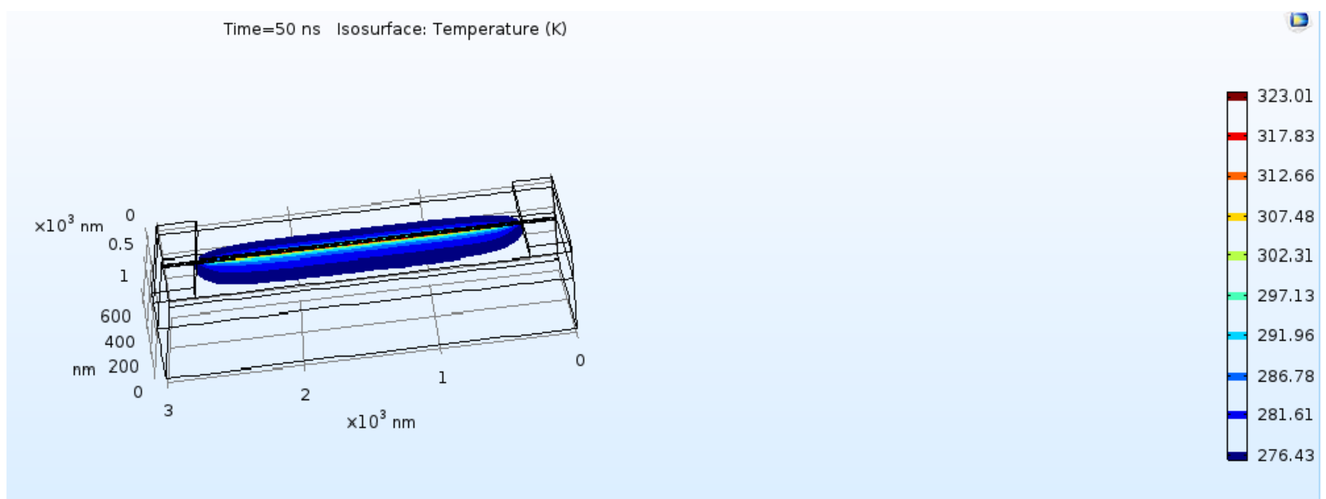

Figure 6: Isothermal contours of Germanium supported nanowire on Silicon di Oxide substrate

3.3.2. Effect of diameter on supported nanowire:

Germanium nanowire is supported on silicon di oxide substrate having 1.4 W/m·K thermal conductivity. Decreasing aspect ratio of nanowire of constant length causes a rise of temperature in supported as well as suspended nanowire. Most theoretical studies have found carrier mobility to increase with radius for sub-10 nm Si NWs, attributing the trend of the dominant surface roughness.

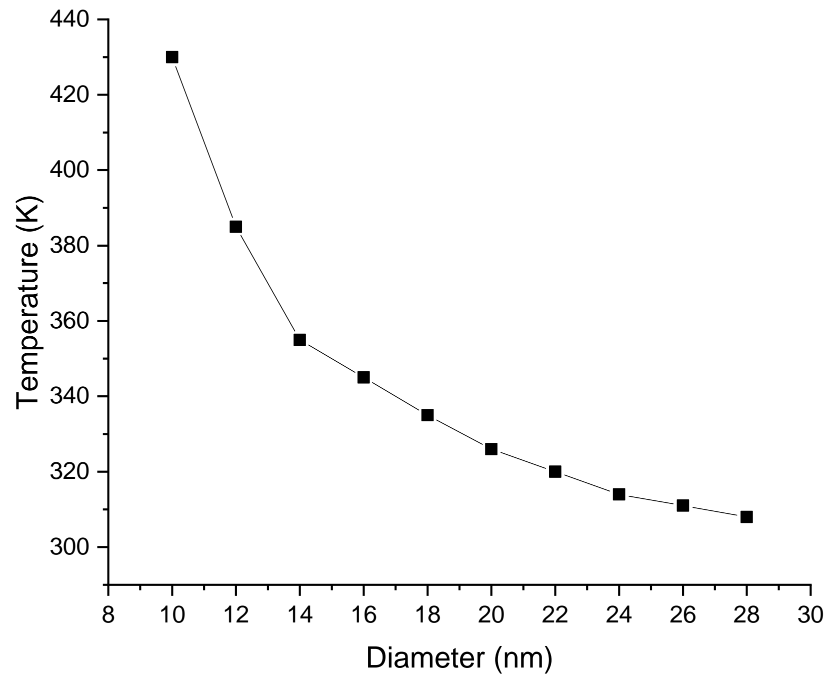

Figure 7: Size reduction effect of Joule heating on Germanium nanowire supported on Silicon di oxide

Scattering in smaller radius NWs of 15 nm or an enhanced phonon scattering rate due to an increased electron-phonon wave function overlapping in smaller radius nanowires [82], [83]. This enhanced scattering rate is shown in figure 4.

3.3.3. Diameter effect on voltage:

The decrease in diameter causes the surface-to-volume ratio to increase and when current is applied at decreasing diameter voltage is increased. This trend confirms the heating is due to Joule heating [84].

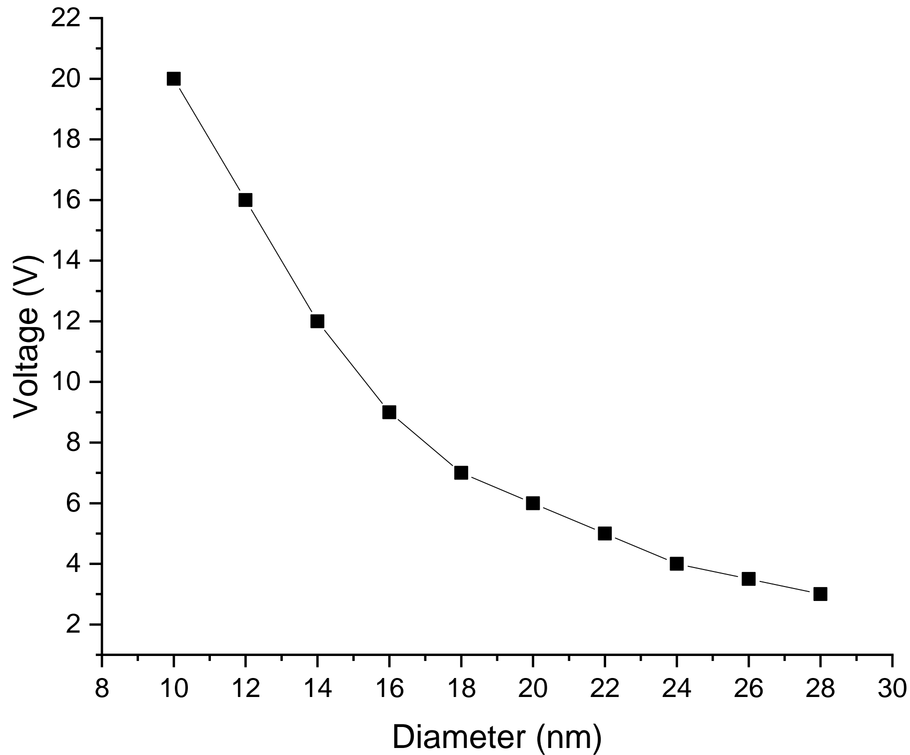

Figure 8: Effect of diameter variation on current carrying nanowire

3.4.Suspended nanowire:

The suspended nanowire field effect transistor is one in which is channel is suspended. Silicon block of 3000nm wide, 400nm height and 1100nm deep is lower most block. The upper block is also called substrate block of nanowire field effect transistor. Its dimensions are 739nm long, 1100nm deep and 200 highs. Nanowire has a varying radius which varies from10nm to 28nm while length of nanowire is 1522nm. The source, channel and drain are created as separate intervals of same dimensions from left to right by providing the 739,1100 and 80nm width, height and depth respectively. After creating, a union at their mutual interfaces. Electric current at source is applied by applying terminal at source and potential difference is created by grounded drain terminal.

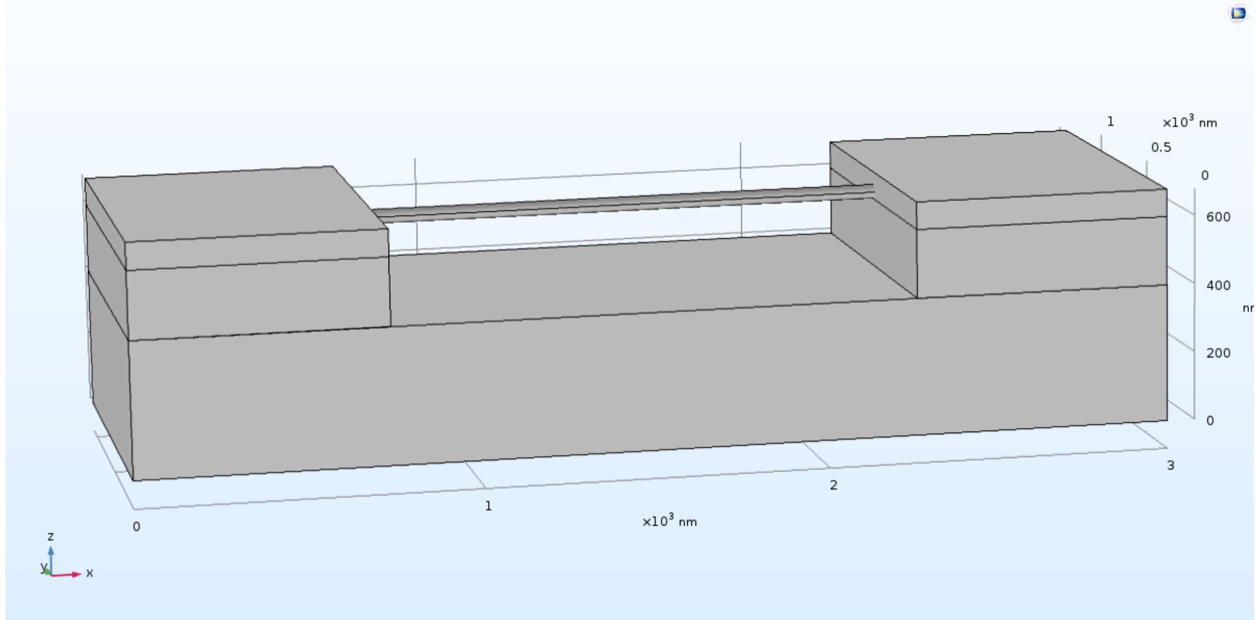

Figure 9: Suspended nanowire

3.4.1. Effect of diameter on supported nanowire:

Thermal conductivity also depends on diameter of nanowire. It is reported that the thermal conductivity of Germanium nanowires is reduced to 1.5 ~1.2 W/m·K from bulk of 56 W/m·K [85]. Phonon-phonon scattering, phonon electron scattering is very prominent when size is reduced to nanometer [86]. An important characteristic is the length scales that determine the applicability of various models to study the Joule heating, have included the phonon mean free path, the phonon wavelength and the lattice spacing, as these helps identify whether the phonons may be treated as particles or waves [87].

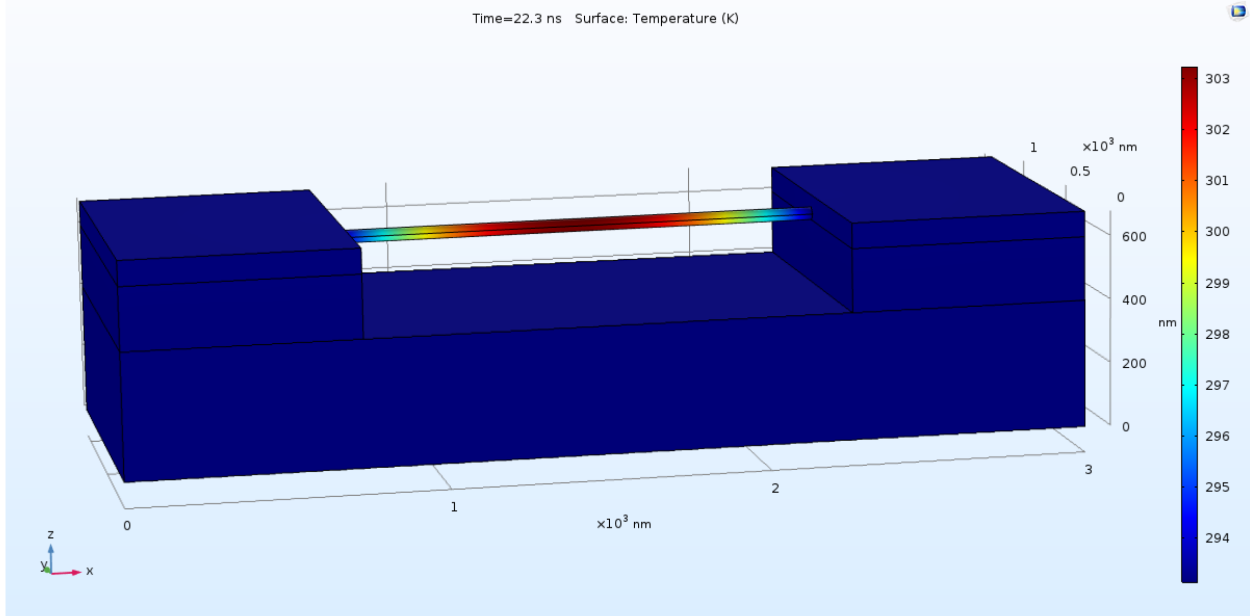

Figure 10: Temperature profile of suspended nanowire

In field effect transistor (FET), the substrate material changes mobility of charge carriers [88] that's why there is a significant rise of temperature in suspended nanowire.

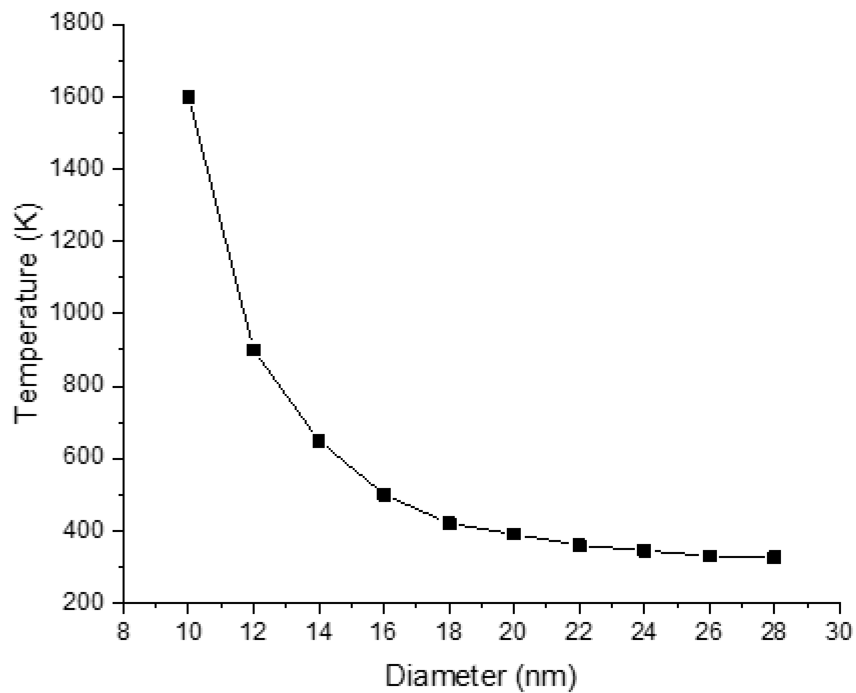

Figure 11: Size reduction effect of Joule heating on Germanium nanowire suspended on Silicon di oxide

Figure 5 and 8 indicates that a reduction in the channel diameter from 28 nm to 10 nm causes a significant increase in the heat generation rate for the same applied voltages. The effects of changing the channel diameter on the device performance were thus studied in greater detail by simulating devices with channel diameter varying from 28 nm to 10 nm. The devices are subjected to an applied current of 10μA and an initial temperature of 293.15 K, and have 739 nm long electrodes.

Figure 4 and 7 illustrates isothermal contours and temperature profile of supported and suspended nanowire. The reference point of the x-coordinate is taken at the start of the device in these figures. Note that a normalized distance ($\frac{x}{x_{total}}$) of 0.5 corresponds to the center of the devices, which coincides with the center of their channel, since the source and drain have equal lengths of 739 nm. Center point nanowire is heated as there are more scattering of charge carrier occurs.

3.5. Effect of substrate thickness on Joule heating:

Substrate thickness also effects the Joule heating because it alters the charge carrier mobility [88]. The substrate and top layer of a thin-film transistor may affect its performance through the introduction of disorder (either long-ranged charge disorder, or short-ranged disorder caused by chemical bonding or roughness) which reduce the charge carrier mobility, and by dielectric screening which may enhance the mobility.

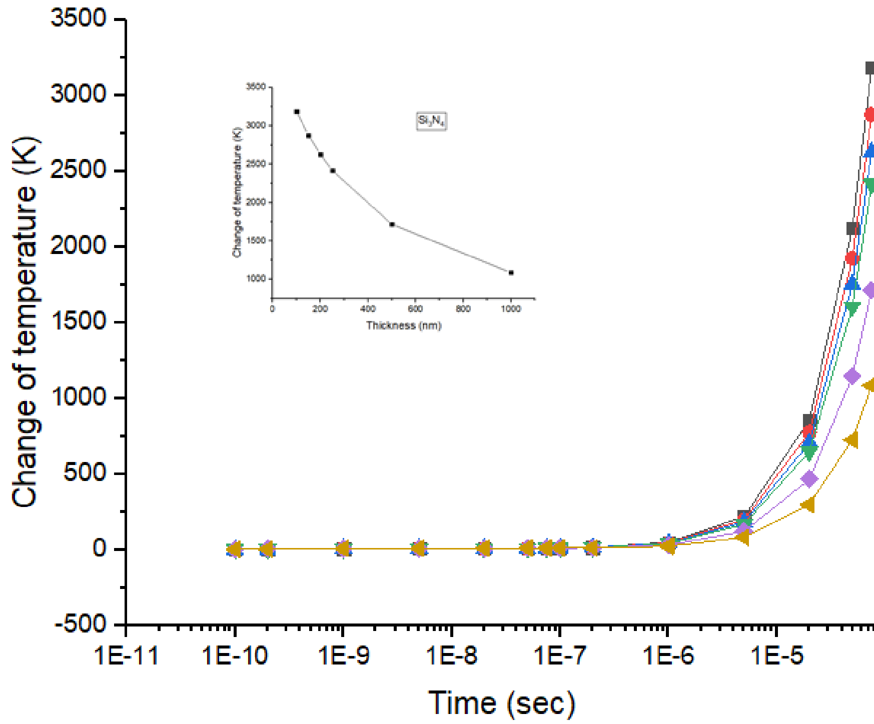

Figure 12: Silicon nitride varying thickness

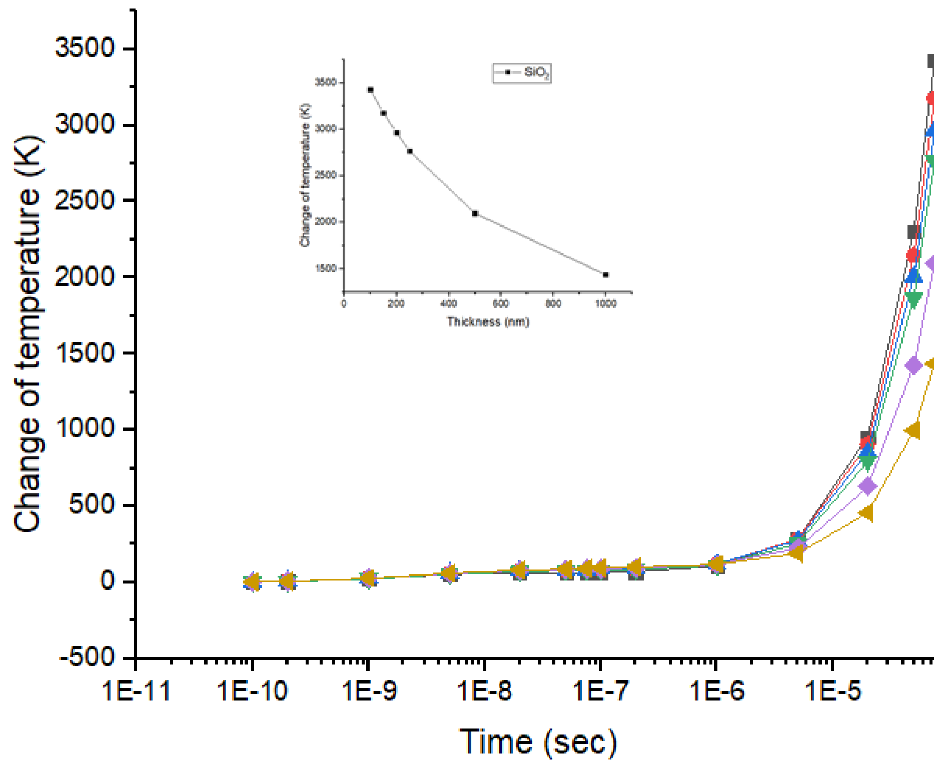

Figure 13: Silicon di oxide varying thickness

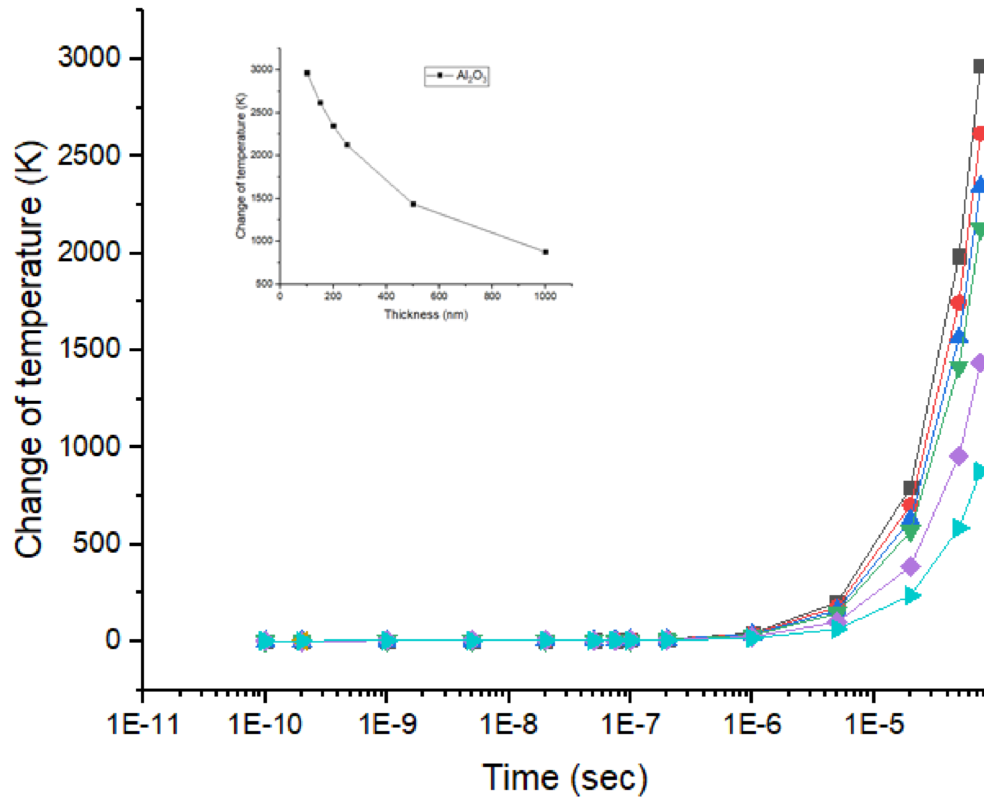

Figure 14: Aluminum oxide varying thickness

3.6 Effect of substrate material on Joule heating:

Joule heating is also affected by substrate material. Substrate material has great impact on heat dissipation phenomena i.e., heat conduction. Heat flows from channel region to substrate material so a better choice of material will help better heat management in MOSFET.

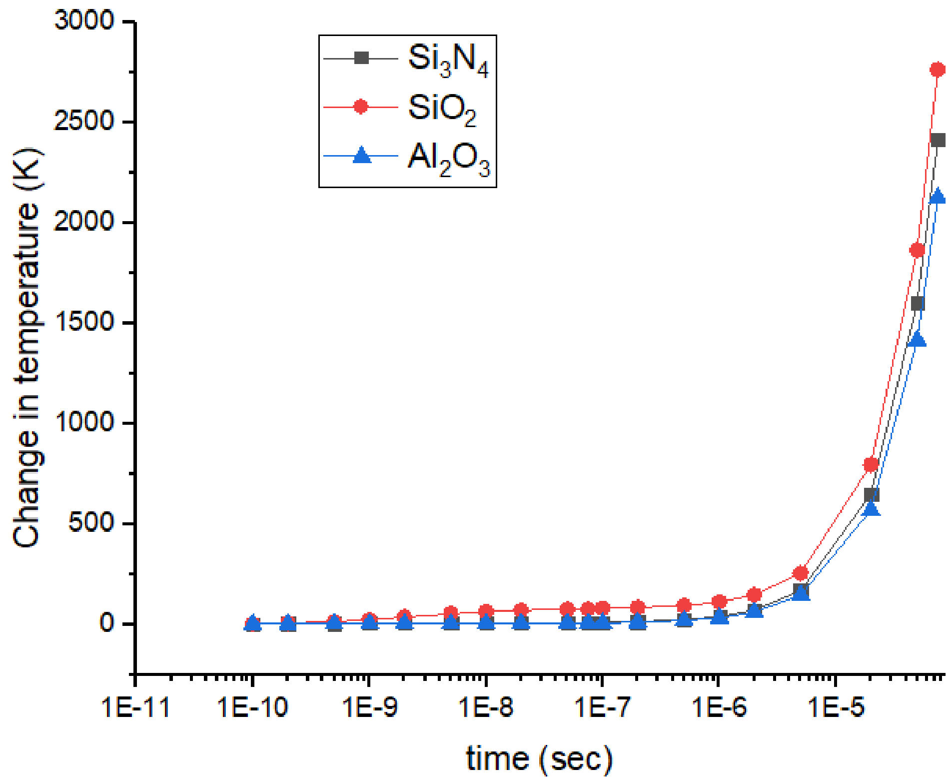

Figure 16: Effect of substrate material

3.7 Effect of variation of length on Joule heating:

We had change the length of nanowire while keeping same the boundary conditions constant. The values of lengths are 1300nm, 1800nm and 2400nm. We found out that rise of temperature is very dependent on length and rise of temperature is almost same.

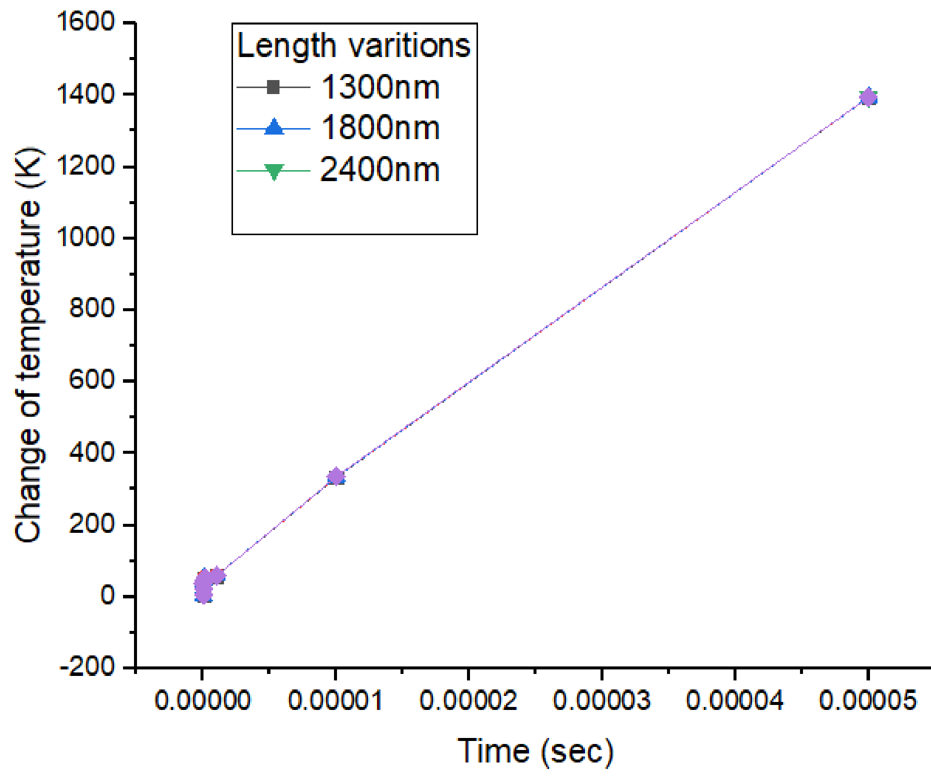

Figure 3.16: Effect of length

Conclusions and future recommendations

4.1.Conclusions:

In this thesis we have focused on the investigation of the effect of Joule heating in nanowire field effect transistor. So we are concluding with these conclusions:

- Joule heating increases by reducing diameter
- Joule heating is severe in suspended nanowire
- Center of nanowire is heated due to carrier density is maximum at that point
- Aluminum oxide shows the least temperature rise, followed by Silicon Nitride and Silicon di oxide shows highest temperature rise

4.2.Future recommendations:

For future studies two dimensional channel and substrate materials with different characteristics is needed. So that a better selection of material will used for portable gadgets. This work can be extended by using different connecting pads.

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