DESIGN OF HIGH SPEED HIGH VOLTAGE CAPACITOR CHARGING SWITCH MODE POWER SUPPLY

By

Rashid Ghani

Submitted to the Department of Electrical Engineering
in Partial Fulfillment of the requirements for the Degree of

Master of Science
in
Electrical Engineering

Thesis Advisor

Dr Mohammad Bilal Malik

College of Electrical and Mechanical Engineering

National University of Sciences and Technology, Pakistan

2008

ABSTRACT

Pulsed power applications like lasers, electronic beam welding etc require conversion of power at high voltages and at high switching speed. Numerous methods and topologies are available for tackling the requirement but selection of a specific topology requires thorough analysis. This research work deals with a 48 V to 800V DC- DC converter capable of charging a 22 µf capacitor within 100 ms.

After study of many topologies, full bridge topology has been selected for this specific application keeping in view the advantages for this specific requirement. MOSFETs are switched using Pulse Width Modulated pulses. Soft start has also been incorporated. The complete converter has been simulated in PSPICE and results achieved are shown and discussed.

ACKNOWLEDGMENTS

I express my extreme gratitude to my project supervisor Dr. Mohammad Bilal Malik for his kind, affectionate and consistent help and guidance not only in academics but also in solving any sort of simulation or fabrication problem. It was he who enabled me to look into every problem with philosophical look and take a logical decision. He always indicated a very high standard of every requirement and pushed me hard till achievement of the goal. His relations with me remained very cordial through all ups and downs of the research work.

I am also very thankful to my friend Mr. Arbab Waleed Ahmad regarding circuit and simulation problems beside countless long discussions over different small problems. He sacrificed his precious time and always gave priority to my work.

My MS colleague and a very close friend Mr. Asim Ijaz extended all out cooperation both technically and administratively during the whole process of my thesis work, rather he hampered his work by sparing me his seat and computer with kind thinking to facilitate completion of my work.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1.

1.1 INTRODUCTION

The voltage regulator assumes a very unique role within a typical system. In many respects, it is the mother of the system. It gives the system life by providing consistent and repeatable power to its circuits. It enables the system to function optimally and protects its wards by not letting them to cross specified limits. If the regulator experiences a failure within itself, it must fail gracefully and not allow the failure to affect other parts of the system.

The requirement that is to design a high voltage high speed switched mode step up converter that is capable of charging a 22uf capacitor within 100 ms provided with a feedback loop to keep the output constant. Inrush current and output ripples are also very important to be kept at their minimum.

Broadly there are two major power supply technologies that can be considered within a voltage regulator system :-

1. Linear voltage regulators.
2. Switched mode power supplies (smps).
    a. Hard switched
    b. Soft switched

Each of these technologies excels in one or more of the system considerations mentioned above and must be weighed against the other considerations to determine the optimum mixture of technologies that meet the needs of the final product. The voltage regulator industry has chosen to utilize each of the technologies within certain areas of product applications. Details of the two techniques are discussed as under:-

1.2 Linear Regulator

The linear regulator is the original form of the regulating power supply. It relies upon the variable conductivity of an active electronic device to drop voltage from an input voltage to a regulated output voltage. In accomplishing this, the linear regulator wastes a lot of power in the form of heat, and therefore gets hot. In general, the linear regulator is quite useful for those power supply applications requiring less than 10 W of output power.

Above 10 W, the heatsink required becomes so large and expensive that a switching power supply becomes more attractive.

1.2.1 **Basic Linear Regulator Operation** . All power supplies work under the same basic principle, whether the supply is a linear or a more complicated switching supply. All power supplies have at their heart a closed negative feedback loop. This feedback loop does nothing more than hold the output voltage at a constant value. Figure 1 shows the major parts of a series-pass linear regulator. Linear regulators are step-down regulators only, that is, the input voltage source must be higher than the desired output voltage.

There are two types of linear regulators: the shunt regulator and the series-pass regulator. The shunt regulator is a voltage regulator that is placed in parallel with the load. An unregulated current source is connected to a higher voltage source, the shunt regulator draws output current to maintain a constant voltage across the load given a variable input voltage and load current. A common example of this is a Zener diode regulator. The series-pass linear regulator is more efficient than the shunt regulator and uses an active semiconductor as the series-pass unit, between the input source and the load.

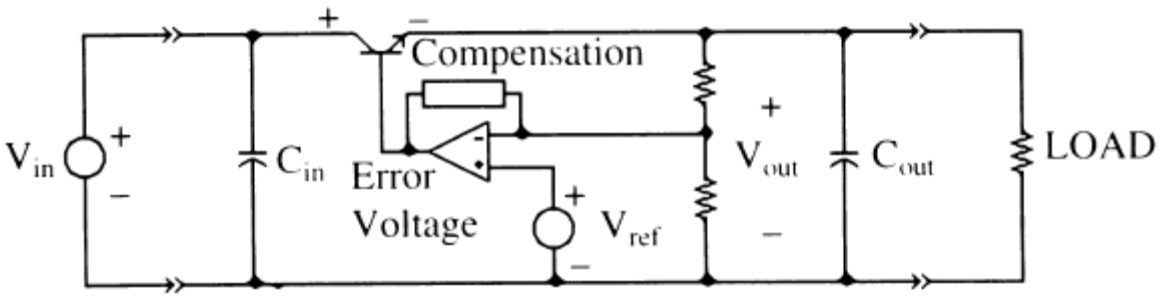

Figure 1. Linear regulator

Figure 1. shows the basic linear regulator. The series-pass unit operates in the linear mode, which means that the unit is not designed to operate in the full on or off mode but instead operates in a degree of "partially on." The negative feedback loop determines the degree of conductivity the pass unit should assume to maintain the output voltage. The heart of the negative feedback loop is a high-gain operational amplifier called a voltage error amplifier. Its purpose is to continuously compare the difference between a very stable voltage reference and the output voltage. If the output differs by mere millivolts, then a correction to the pass unit's conductivity is made. A stable voltage reference is placed on the noninverting input and is usually lower than the output voltage. The output voltage is

divided down to the level of the voltage reference. This divided output voltage is placed into the inverting input of the operational amplifier. So at the rated output voltage, the center node of the output voltage divider is identical to the reference voltage. The gain of the error amplifier produces a voltage that represents the greatly amplified difference between the reference and the output voltage (error voltage). The error voltage directly controls the conductivity of the pass unit thus maintaining the rated output voltage. If the load increases, the output voltage will fall. This will then increase the amplifier's output, thus providing more current to the load. Similarly, if the load decreases, the output voltage will rise, thus making the error amplifier respond by decreasing pass unit current to the load.

The speed by which the error amplifier responds to any changes on the output and how accurately the output voltage is maintained depends on the error amplifier's feedback loop compensation. The feedback compensation is controlled by the placement of elements within the voltage divider and between the negative input and the output of the error amplifier. Its design dictates how much gain at dc is exhibited, which dictates how accurate output voltage will be. It also dictates how much gain at a higher frequency and bandwidth the amplifier exhibits, which dictates the time it takes to respond to output load changes or transient response time. The operation of a linear regulator is very simple. The very same circuitry exists in the heart of all regulators, including the more complicated switching regulators. The voltage feedback loop performs the ultimate function of the power supply's maintaining of the output voltage.

1.3 **Switched Mode Power Supplies.** Although pulsewidth modulated (PWM) switching power supplies have been around for a long time, it wasn't until the mid-1970s that they became more acceptable and broadly applied. Switching power supplies offer many advantages over linear regulators. Switching power supplies are more efficient and are smaller in size than linear regulators of similar ratings. They are, however, more difficult to design and radiate more electromagnetic interference (EMI).

Today, there are two ways to approach the design of switching power supplies. The design of board-level, dc/dc (dc-in, dc-out) switching power supplies require standardized approaches that are much more complex and difficult to be tackled. The operation of switching power supplies can be relatively easy to understand.

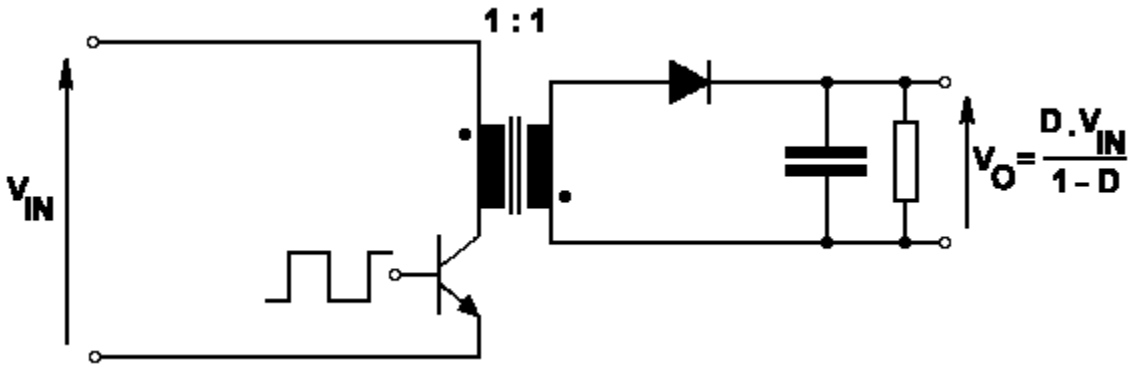

Figure 2. switched mode power supply

Unlike linear regulators which operate the power transistor in the linear mode, the PWM switching power supply operates the power transistors in both the saturated and cutoff states. In these states, the volt-ampere product across the power transistor is always kept low. This EI product within the power device is the loss within all the power semiconductors. This more efficient operation of the PWM switching power supply is done by "chopping" the direct current (dc) input voltage into pulses whose amplitude is Pulsewidth Modulated. Switching Power Supplies uses the magnitude of the input voltage and whose duty cycle is controlled by a switching regulator controller. Once the input voltage is converted to an ac rectangular waveform, the amplitude can be stepped up or down by a transformer.

Additional output voltages can be derived by adding secondaries to the transformer. Ultimately these ac waveforms are then filtered to provide the dc output voltages. The controller, whose main purpose is to maintain a regulated output voltage, operates very much like a linear style controller. That is, the functional blocks, voltage reference, and error amplifier are arranged identical to the linear regulators. The difference is, the output of the error amplifier (the error voltage) is then placed into a voltage-to-pulsewidth converter stage prior to driving the power switches.

There are many factors which are taken care in designing a regulator. All these factors are demand dependent. Some common important issues that influence design of voltage regulator are:

a. Cost.

b. Weight and space.

c. How much heat can be generated within the product?

d. The input power source.

e. The noise tolerance of the load circuits.

f. Battery life (if the product is to be portable).

g. The number of output voltages required and their particular characteristics.

Chapter 2

SWITCHING REGULATORS TOPOLOGY SURVEY

2.1 Introduction.

There are about 14 basic topologies commonly used to implement a switching power supply. Each topology has unique properties which make it best suited for certain application.

Some are best used for AC/DC off line converters at low output power, some at higher output power. Some are better choice for higher AC input whereas some are for lower AC input. Some have higher DC output, some have lower parts count. Lesser input or output ripples and noise is a frequent factor in a topology.

Thus to make a good choice of a topology, it is essential to look into all merits, drawbacks and practicability of design and fabrication. In this chapter a topological survey of existing switching voltage regulators have been carried out and their schematics and functions are discussed in more detail which will aid in selection of a specific topology most suitable for our requirement. Salient features are as follow:-

2.1.1 Buck Converter:

The series switch is turned ON & OFF at a high frequency (20 kHz – 100 kHz) and the Diode acts as a free wheeling diode. The output is regulated in a similar manner i.e. sensing the output voltage, comparing it with a reference to get the error signal and then determining the duty ratio 'D' by comparison with a linear ramp waveform. The input output voltage relation obtained is;

$$\frac{V_{out}}{V_{in}} = D \qquad (2.1)$$

The topology is shown in figure 3

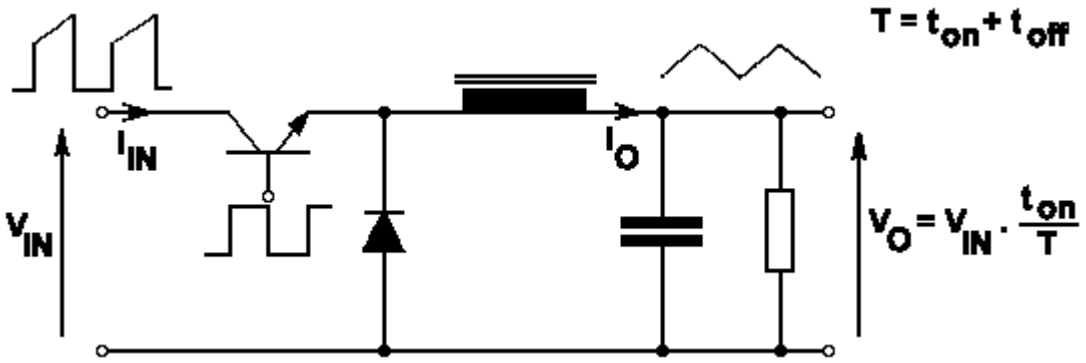

Figure 3. Buck converter

2.1.2 Boost Converter:

The basic topology is shown in figure 4.

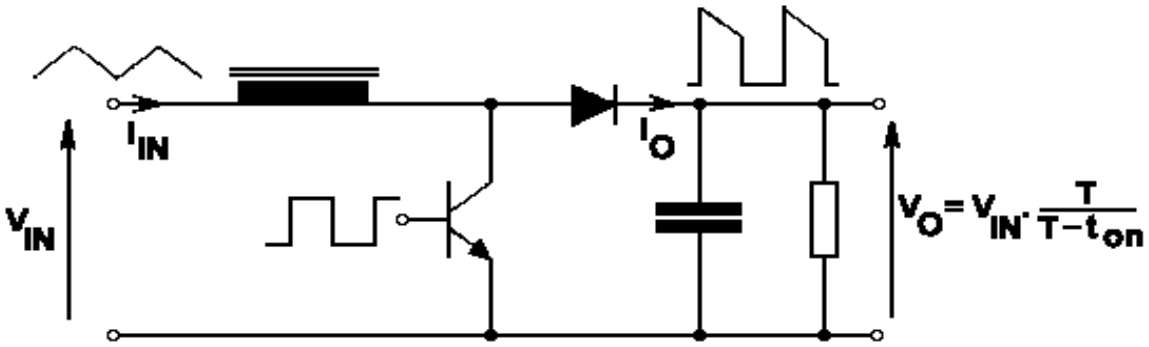

Figure 4. Boost converter

A shunt switch is turned ON and OFF at high frequency (20 kHz – 100 kHz) and the output is regulated by taking a sample of the output voltage and comparing it with a reference and then generating and appropriate PWM signal which drives the active shunt switch.

The voltage conversion ratio is

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \qquad (2.2)$$

From the input output relationship we get the constraint that the out put voltage must be higher than the peak of the input voltage.

2.1.3 Buck-Boost converter:

The basic topology is as shown in the figure 5.

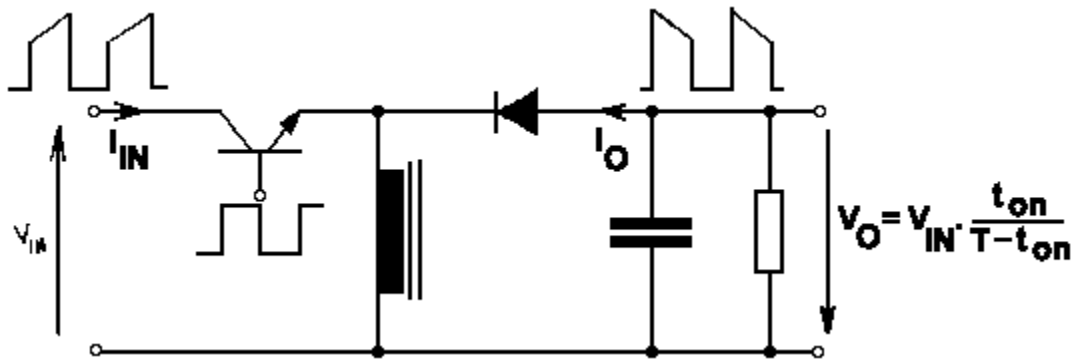

Figure 5. Buck boost

It has dual qualities as it is a cascade combination of Buck converter and Boost converter. The significant feature being that the output voltage is negative w.r.t the common terminal of the input voltage. It follows the same voltage regulation principle as discussed above with the input output voltage relationship given by

$$\frac{V_{out}}{V_{in}} = -\left(\frac{D}{1-D}\right) \qquad (2.3)$$

This shows that the output voltage can be higher or lower than the input voltage with a negative polarity. The disadvantage being that the input current is highly discontinuous.

2.1.4 Flyback Converter

The flyback converter topology is shown in fugure 6.

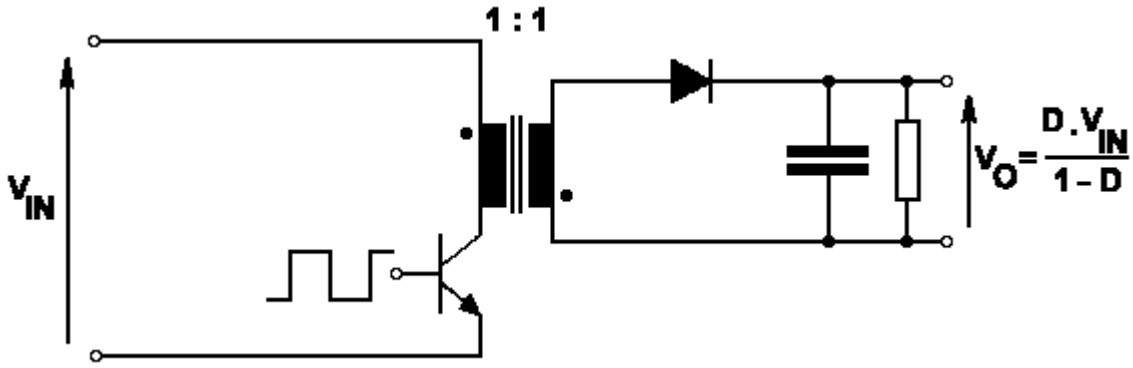

Figure 6. Fly back converter

It is simpler and used at comparatively lower power levels as compared to the buck or boost converters. It has the advantage that the input and output sides are isolated.

$$\frac{V_{out}}{V_{in}} = \frac{N_s}{N_p}\left(\frac{D}{1-D}\right) \qquad (2.4)$$

i.e the out put voltage can be higher or lower than the input voltage and can be scaled by a factor of Ns/Np. However the disadvantage is that the input current is highly discontinuous and generates sufficient EMI.

2.1.5 Cuk Converter:

This converter named after its inventor Slobodan Ćuk is obtained by applying the duality principle to the Buck boost converter (Fig 7).

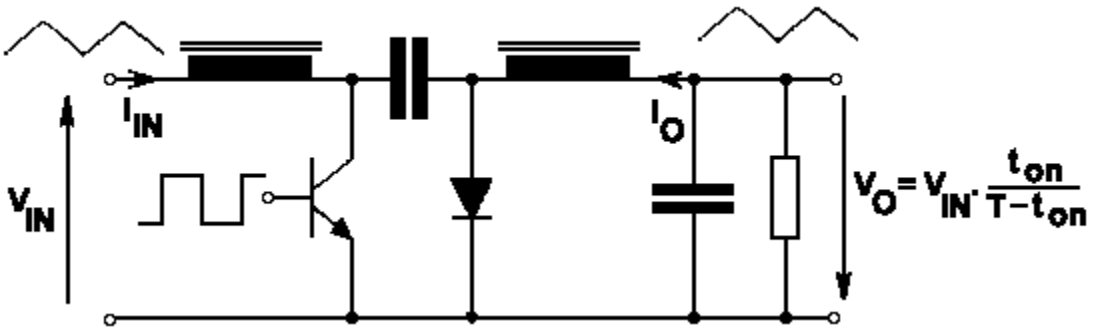

Figure 7. Cuk converter

It is a bit complicated as compared to the ones discussed earlier as it uses more storage elements (two inductors and two capacitors) and control is a bit complicated as it acts as the intermediate storage element. It is charged with the switch S open and discharged with the switch S closed thus transferring the energy to C2 and hence to the output.

The input output voltage relationship is

$$\frac{V_{out}}{V_{in}} = -\left(\frac{D}{1-D}\right) \qquad (2.5)$$

i.e the output voltage is negative w.r.t common terminal of the input voltage. The output voltage can be higher or lower than the input. The biggest advantage being that the input current is continuous.

2.1.6 Half Bridge Converter:

. This topology is used for medium power conversions. It is an electrically isolated type converter. Its operation is based on two switches functioning alternately. The basic topology is a shown in figure 8

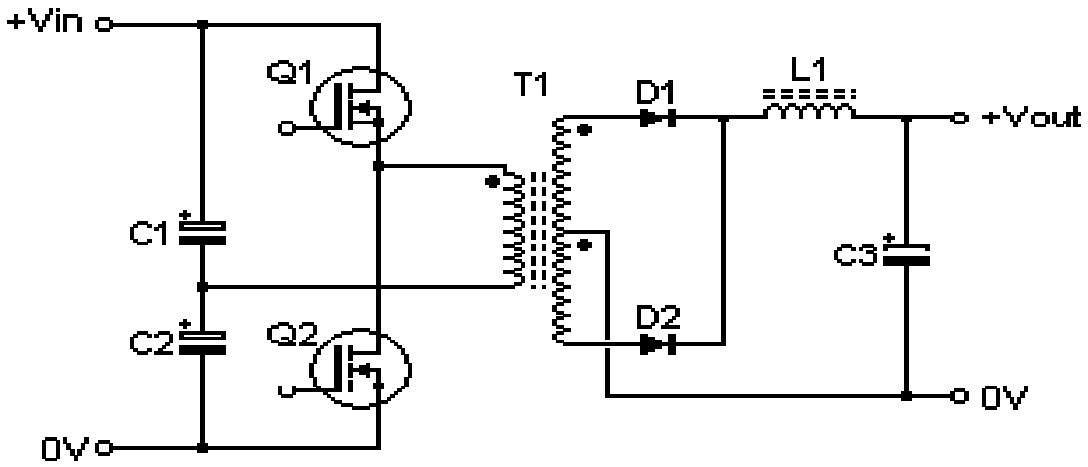

Figure 8. Half bridge converter

The half bridge converter is similar to the push pull converter, but a centre tapped primary is not required. The reversal of the magnetic field is achieved by reversing the direction of the primary winding current flow. This voltage impressed across the transistors is half of the input voltage. This is being achieved due to connection of one end of transformer primary between the junction of two capacitors. Disadvantage is doubling of current and in turn more stress over transistors. For the half bridge converter, the output voltage V_o equals the average of the waveform applied to the LC filter

$$V_{out} = \frac{V_{in}}{2}\frac{N_s}{N_p}\left(T_{on,q1} + T_{on,q2}\right) f \qquad (2.6)$$

where

V_{out} ; Output Voltage - Volts

V_{in} ; Input Voltage - Volts

N_s; 0.5 x secondary turns

N_p; primary turns

f ; operating frequency - Hertz

Ton,q1 ; Q1 conduction time - Seconds

Ton,q2 ; Q2 conduction time - Seconds

Q1 and Q2 are never conducting at the same time. The control circuit of a half bridge converter is similar to that of a push-pull converter

2.1.7 Full Bridge converter:

Basic topology is shown as under.

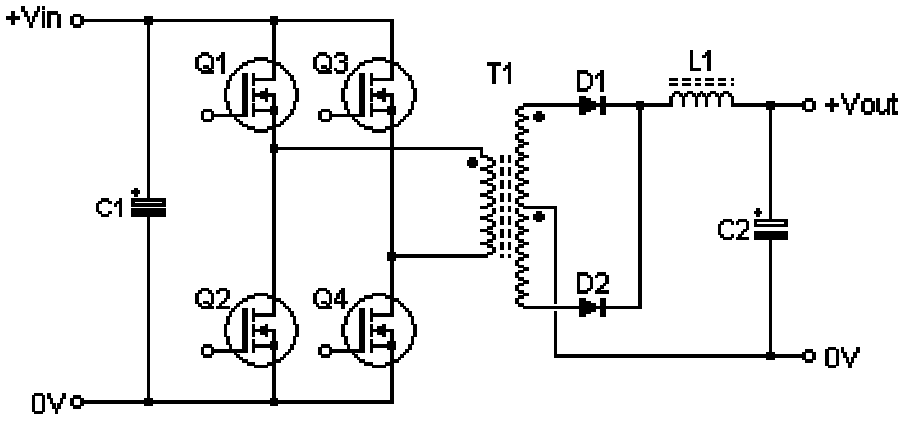

Figure 8. Full bridge converter

The full bridge converter is similar to Half Bridge converter, but a centre tapped primary is not required. The reversal of the magnetic field is achieved by reversing the direction of the primary winding current flow. Diagonal pairs of transistors will alternately conduct, thus achieving current reversal in the transformer primary. This can be illustrated as follows:-

With Q1 and Q4 conducting, current flow will be 'downwards' through the transformer primary and with Q2 and Q3 conducting, current flow will be 'upwards' through the transformer primary.

The control circuit monitors V_o and controls the duty cycle of the drive waveform to Q1, Q2, Q3 and Q4. This type of converter is found in high power applications. Advantage of this topology is that full input voltage is applied across the primary of the transformer, reducing current to half as compared to half bridge topology. This topology is used from medium to high range of power conversion requirements. For the full bridge converter, the output voltage V_o equals the average of the waveform applied to the LC filter.

$$V_{out} = \frac{V_{in}}{N_p} \frac{N_s}{N_p} \left(T_{on,q1} + T_{on,q2} \right) f \qquad (2.7)$$

where

V_{out} ; Output Voltage - Volts

V_{in} ; Input Voltage - Volts

N_s ; 0.5 x secondary turns

N_p ; primary turns

f ; operating frequency - Hertz

Ton,q1; Q1 conduction time - Seconds

Ton,q2;= Q2 conduction time - Seconds

The control circuit operates almost in the same manner as for the half-bridge converter, except that four transistors are being driven instead of two.

Chapter 3

Selection of the Most Suitable Topology

3.1 Introduction

Many evolutionary changes have occurred to make the switching power supplies that meet the needs of many diverse applications. For this reason, many variations have evolved, each with merits that make it better suited for a particular application. Some topologies work better at high input voltages, some at higher output power levels, and some are targeted for the lowest cost. Many topologies can work for each particular application, but one topology usually has the right combination of features that makes it the best choice.

The requirement that is to be fulfilled is to design a high voltage high speed switched mode step up converter that is capable of charging a 22uf capacitor within 100 ms provided with a feedback loop to keep the output constant. Inrush current and output ripples are also very important to be kept at their minimum.

To be able to select the best suited topology that fulfills our requirement optimally, analysis of all previously discussed topologies have been carried out.

3.2 Factors Affecting the Choice of an Appropriate Topology

In order to select an appropriate topology for our application it is necessary to analyze the subtle differences between the topologies and

Factors that make them more desirable for our requirement. Four primary factors differentiate the various topologies from one another.

a. **Current Stress**. This is a measure of how much stress the power semiconductors must withstand and tends to limit a particular configuration in the output power it can deliver. Inrush current at the time of switching ON the regulator some time ranges upto hundreds of amperes which can destroy the switches in a split second. Ways and means are required to limit this inrush current.

b. **Voltage Stress**. It is a very important parameter that can be placed across the power semiconductors. This indicates how effectively power can be derived from the input line. Switches are exposed to very high voltage stresses at ON and OFF. Switches required to operate around 1000 v are not cost effective beside not very easy availability

c. **Electrical Isolation of the Input.** It is another important factor to isolate input from the load. This provides electrical isolation of the output from the input and allows the design to add safety of the two sides and components with ease. Transformer isolation is therefore necessary in order to meet the safety requirements dictated by the specific requirement.

d. **Cost and Reliability**. It is the priority of any design to select a configuration that requires the minimum number of parts without subjecting the components to undue stress and in turn reduce the overall cost.

At the beginning of power supply design efforts are required to perform a little predesign estimation exercise. This is done by making a reasonable assumption about the regulator efficiency and working with the general equations involving the peak currents and voltages. From this exercise, we can select the best switching power supply topology, preliminary choice of the semiconductors, and even estimate the amount of losses within the components. It may also guide us in an approach to packaging the power supply and provide some idea as to the final cost of the supply. This effort can act as an early roadmap during the design phase and also saves time because the we can order the semiconductor components before the power supply is even designed. The boundaries to these areas are determined primarily by the amount of stress the power switches (MOSFETs in our case) must endure and still provide reliable performance. Higher peak currents can be used but the power switches would begin unusual failure, and items such as board layout and lead lengths would become even more critical. Then the failures could be hardly protected by transformer isolation. The non-transformer-isolated topologies have very predictable and catastrophic failure modes and we will not prefer to risk.

3.3 Non-Transformer-Isolated Switching Power Supply Topologies

The three basic non-transformer-isolated topologies, the buck (step-down), the boost (step-up), and the buck-boost (inverting) topology generates and regulates an output voltage that is above or below the input voltage. Each also has only one output. Non-transformer-isolated supplies have definite restrictions as to their application in regard to their input voltage with respect to their output voltage.

a. **The Buck Regulator Topology.** It is a simple and versatile topology operated by a single switch. The buck regulator can be used only as a step-down regulator for this reason, it is not feasible for our requirement.

b. **The Boost Regulator Topology.** The boost regulator is a step-up regulator. This topology is limited to a 50 percent duty cycle since the core needs sufficient time to empty its energy into the output capacitor. This topology operates at about three times the peak current of forward-mode regulators. This is mainly due to having a 50 percent duty cycle limit. This high peak current limits its usefulness as the stress on the semiconductor power switch becomes too great. As with all non-transformer-isolated topologies, the ability of the boost regulator to prevent hazardous transients or failures within the supply from reaching the load is quite poor. This topology can also be not selected.

c. **The Buck-Boost Regulator Topology.** The buck-boost regulator is also limited to below a 50 percent power switch duty cycle since it requires time to empty the core of its stored energy. This topology cannot be used because semiconductors offer poor isolation and protection against failures and failure-inducing conditions.

3.4 **Transformer-Isolated Switching Power Supply Topologies**

a. **The Flyback Regulator Topology.** The flyback transformer, because of its unipolar use of the B-H curve, does exhibit very high flux excursions that could easily result in the core material saturation. When this happens, the linear current ramp exhibited by the flyback during the power switch on-time quickly becomes nonlinear and proceeds rapidly toward infinite current. The flyback topology is unsuitable due to much higher peak currents

b. **The Push-Pull Regulator Topology.** This topology is sometimes used above 150 W which exhibits some fundamental shortcomings that make it tricky to use. It suffers from one serious flaw which is a real-world factor i.e no two power switches are identical and no two halves of a center-tapped winding are identical. These means that one side of the primary will have a fraction of a turn less than the other side or that the power switch will turn off slightly slower or have a slightly lower saturation voltage. This condition guarantees that the transformer core will never operate symmetrically around the origin of the B-H curve. This results in magnetic

core imbalance which requires expensive and complicated symmetry circuits.

c. **TheHalf-Bridge Regulator Topology.** The capacitor center node voltage is at approximately one-half of the input voltage, and the power switches present the other end of the primary winding with an alternating input voltage and ground. This means that only half the input voltage appears across the primary winding. This results in an average and hence twice peak current as compared to Full Bridge topology. Half-bridge regulator topology is also not feasible for our requirement.

d. **The Full-Bridge Regulator.** The full-bridge converter is the most popular transformer-isolated converter topology. Like the other double-ended regulators, its transformer's flux is driven in both the positive and negative polarities. Its performance with respect to output power is significantly improved over that of the half-bridge converter. This is because the balancing capacitors are replaced with another pair of half-bridge style power switches identical to the first pair. This time, two of the four power switches are turned on simultaneously. During one conduction cycle the diagonal pair of power switches is turned on. Each associated pair of power switches conduct on alternate cycles. This places the full input voltage across the primary winding, thus reducing the peak currents in the primary for any output power as compared to the half bridge regulator. This effectively doubles the maximum power-handling capability of this topology over the half-bridge. The full-bridge regulator topology can be used in applications requiring output powers of 100 W to many kilowatts.

It is now very much clear that we require a transformer isolated type topology. After thorough analysis of all the topologies and keeping in view the power parameters of our requirement, a combination of full bridge and buck converter topology has been adopted for the design. Salient considerations are as follow:-

a. More power rating.
b. Less stress over switches

c. Full input voltage across MOSFETs
d. Less current with same core
e. No hazard of magnetic core imbalance
f. No symmetry circuit required
g. Better voltage regulation

CHAPTER 4

TRANSFORMERS

4.1 DEFINITION OF TRANSFORMER

A transformer consists of two electrical circuits interlinked by a magnetic circuit. We can recognize the insignia of the “three links”, one of the two electrical circuits is designated as the primary, and the other as the secondary, while the link connecting the two is the core. The primary circuit receives the energy and is referred to as the input whereas the secondary circuit discharges the energy and is referred to as the output. A transformer is a very efficient device and if we exclude the core and copper losses (usually about 1 %) the input power will equal the output power. Transformer is basically a static device that converts the level of energy and not the form of energy.

4.1.1 HISTORICAL BACKGROUND

Transformers are electrical devices which change or transform voltage levels between two circuits. In the process, current values are also transformed. However, the power transferred between the circuits is unchanged, except for a typically small loss which occurs in the process. This transfer only occurs when alternating current (a.c) or transient electrical conditions are present. Transformer operation is based on the principle of induction discovered by Faraday in 1831. He found that when a changing magnetic flux links a circuit, a voltage or electro motive force (emf) is induced in the circuit. The induced voltage is proportional to the number of turns linked by the changing flux. Thus when two circuits are linked by a common flux and there are different linked turns in the two circuits, there will be different voltage induced. This situation is shown in Fig. 9 and 10 where a core is shown carrying the common flux. The induced voltage V1 and V2 will differ since the linked turns N1 and N2 differ.

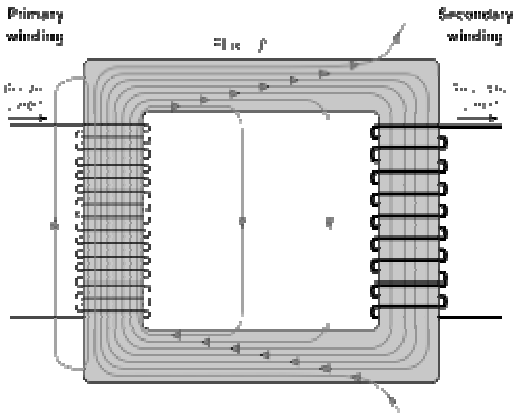

Figure 9 Basic transformer

Transformer just changes ratios of different components of power and other parameters and also provides an excellent isolation between the input and output side. Transformer behavior regarding different electrical parameters is as following:-

$$\frac{V_p}{V_s} = \frac{I_s}{I_p} = \frac{N_p}{N_s} \qquad (4.1)$$

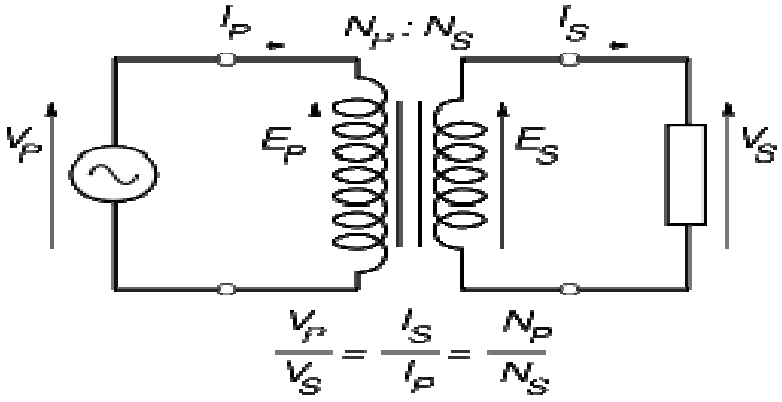

Figure 10. Transformation ratios

4.2 **BASIC MAGNETISM**

The discovery by Oersted that currents give rise to magnetic fields led Ampere to propose that material magnetism results from localized currents. He proposed that large numbers of small current loops, appropriately oriented, could create the magnetic fields associated with magnetic materials and permanent magnets.

The relation between induction, **B**, magnetization, **M**, and fields, **H**, in SI units, is

$$\mathbf{B} = \mu_{\circ} (\mathbf{H} + \mathbf{M}) \qquad (4.2)$$

For many materials, M is proportional to H,

$$\mathbf{M} = \chi \mathbf{H} \qquad (4.3)$$

Where χ is the susceptibility which need not be a constant. Substituting into equation (4.1)

$$\mathbf{B} = \mu_{\circ} (1 + \chi) \mathbf{H} = \mu_{\circ} \mu_{r} \mathbf{H} \qquad (4.4)$$

Where $\mu_{\circ} = 1 + \chi$ is the relative permeability. We see directly in (4.1) that, as **M** saturates because all the domains are similarly oriented, **B** can only increase due to increases in **H**. This occurs at fairly high **H** or exciting current values, since **H** is proportional to exciting current. At saturation, since all the domains have the same orientation, these are not domain walls. Since **H** is generally small compared to **M** for high permeability ferromagnetic materials up to saturation, the saturation magnetization and saturation induction are nearly the same, As the temperature increases, the thermal energy begins to compete with the alignment energy and the saturation magnetization begins to fall until the Curie point is reached where ferromagnetism completely disappears.

4.3 Types of Transformers

A variety of specialized transformer types have been created for the electrical transformer to fulfill specific requirement. Despite their design differences, the various types employ the same basic principle as discovered in 1831 by Michael Faraday, and share several key functional parts. Some major types of transformers are as under:-

a. Power transformers

(1) Laminated core
(2) Toroidal
(3) Autotransformer
(4) Variac
(5) Constant voltage transformer (ferro-resonance)
(6) Stray field transformer
(7) Polyphase transformers
(8) Resonant transformers
(9) Oil cooled transformer
(10) Isolating Transformer
(11) Microwave Oven Transformer

b. Instrument transformers

(1) Current transformers

(2) Voltage transformers

C. Pulse transformers

d. RF Transformers

(1) Air core transformers

(2) Ferrite core transformers

Ferrite core transformers are widely used in switched mode power supplies. The powder core enables high frequency operation, and hence much smaller size to power ratio than laminated iron transformers. Ferrite transformers are not usable as power transformers at mains frequency.

(3) Transmission line transformers

(4) Baluns

e. Audio transformers

(1) Speaker transformers (public address)

(2) Output transformer (valve)

(3) Small Signal transformers

(4) 'Interstage' and coupling transformers

4.4 **LOSSES IN TRANSFORMER**

4.4.1 Primary and Secondary losses. The energy losses in a transformer may be classified as the primary loss, the secondary loss, and the core loss. The primary loss is a true I^2R loss and is expressed in watts. This loss is caused by the resistance in the primary winding. The power loss in the secondary is also an I^2R loss, caused by the resistance in the secondary windings. When there is no load on the transformer, the transformer is not supplying current, and the power loss in the secondary is zero.

4.4.1.1 Core Losses. The loss in the core is a power loss and is expressed in watts. The core loss may be divided into two parts, one is called eddy-current loss, the other hysteresis loss discussed as under:-

a. Eddy-Current Loss. The eddy current in any core is a true electric current induced in the core by the changing magnetic flux, just as if the core was the

desired conductor. Induced current in the core is undesirable, since such currents require power input to the device and simply convert the electrical input into heat thus increasing the resistance and therefore the power loss in both coils. The eddy-current loss is very less in soft ferrite cores. It is 1/49 of the solid iron core.

b. Hysteresis Loss. "Hysteresis" is a Greek word meaning to lag. Hysteresis in a core means that the magnetic flux, or lines of force, lags behind the magnetizing force that causes them. The nature of the hysteresis effect may be understood by considering that whenever a new piece of iron is subjected to a magnetizing force and the magnetizing force is removed, a portion of the magnetic flux remains in the iron. In order to remove this residual magnetism, another magnetizing force must be applied to the iron in a direction opposite to that of the initial magnetizing force. In other words, energy has to be supplied to demagnetize the iron. In the operation of the transformer the primary current is constantly changing not only in value but also in direction , so that the magnetizing force of the primary is first in one direction and then in the opposite direction. For each single change in magnetization from one direction to the opposite one a certain amount of power or energy is demanded. The total amount of energy thus required per second will evidently depend upon the number of reversals that occur each second as well as upon the quality of the core. A soft ferrite core retains few lines of force and hence requires less applied energy to demagnetize it.

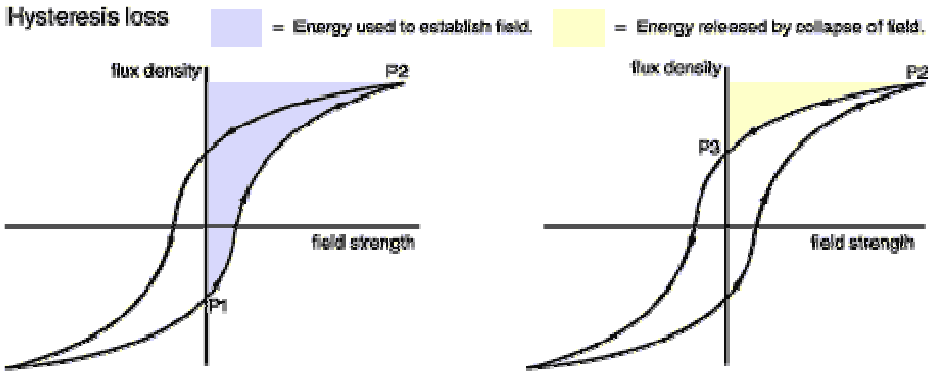

Figure 11. B-H curve

` Fig 11 serves to represent the simplest form of an alternating voltage, current, or magnetic flux. The magnetic flux, increases from zero to a certain positive, or P2, maximum, decreases to P3 when field strength is reduced to zero. The magnetic flux increases in the opposite direction to a negative, maximum, and finally returns to zero, ready to repeat a similar cycle of values.

It is important point to be noticed that the copper loss of the transformer varies as the square of the load current whereas, the core loss depends on the terminal voltage and the frequency of the supply. The core loss is constant from no load to full load because the factors affecting it are also constant, i.e. frequency, voltage, etc.

4.5. **Core Material and Geometry.** Although almost any magnetic material may be used in designing high frequency power transformer, ferrites have been almost exclusively used in modern converters. Ferrites may not have very high operating flux densities, most ferrites have B_{sat} from 3000 to 5000 G but they offer low core losses at high frequency, good winding coupling and ease of assembly.

Cores made from ferrites come in many shapes and sizes, and various power ferrite materials specifically aimed at high-frequency transformer design have been developed by manufacturers. The geometry of the core used for a specific application depends on the power requirements. E-E, E-I, E-C, and pot cores are some of the most popular shapes. Because of their constructions, Pot Cores are very well suited for low to medium power applications, anywhere from 10 to 150 W. They are particularly attractive for designs requiring low flux leakage, and their inherent self-shielding design minimizes EMI.

For higher power levels E-E, E-I, and E-C cores may be used. The E-C core is a compromise between an E-E and a pot core, combining the advantages of each shape. Manufacturers of cores list all the important parameters required to design a power transformer, and if a particular parameter is not listed, it can easily be calculated using the magnetism equations.

TABLE -1- Heavy Film-Insulated Magnet Wire Specifications

AWG	Diameter over insulations (inches)		Nominal circular mil area	Resistance per 1000 ft	Current capacity in milliamperes based on 1000 c.m / A	AWG
	Min.	**Max.**				
8	0.130	0.133	16510	0.6281	16510	8
9	0.116	0.119	13090	0.7925	13090	9
10	0.104	0.106	10380	0.9985	10380	10
11	0.0928	0.0948	8230	1.261	8226	11
12	0.0829	0.0847	6530	1.588	6529	12
13	0.0741	0.0757	5180	2.001	5184	13
14	0.0667	0.0682	4110	2.524	4109	14
15	0.0595	0.0609	3260	3.181	3260	15
61	0.0532	0.0545	2580	4.020	2581	16
17	0.0476	0.0488	2050	5.054	2052	17
18	0.0425	0.0437	1620	6.386	1624	18
19	0.0380	0.0391	1290	8.046	1289	19
20	0.0340	0.0351	1020	10.13	1024	20
21	0.0302	0.0314	812	12.77	812.3	21
22	0.0271	0.0281	640	16.20	640.1	22
23	0.0244	0.0253	511	20.30	510.8	23
24	0.0218	0.0227	404	25.67	404	24
25	0.0195	0.0203	320	32.37	320.4	25
26	0.0174	0.0182	253	41.02	252.8	26
27	0.0157	0.0164	202	51.44	201.6	27
28	0.0141	0.0147	159	65.31	158.8	28
29	0.0127	0.0133	128	81.21	127.7	29
30	0.0113	0.0119	100	103.7	100	30
31	0.0101	0.0108	79.2	130.9	79.21	31
32	0.0091	0.0098	64	162	64	32
33	0.0081	0.0088	50.4	205.7	50.41	33
34	0.0072	0.0078	39.7	261.3	39.69	34
35	0.0064	0.0070	31.4	330.7	31.36	35

4.6 High-Frequency Transformer Considerations

Some practical and fundamental design equations and procedures will be used for the design of the isolation transformer. The majority of the design equations are fundamentally valid for any types of magnetic circuit, and they may be adapted to solve a variety of magnetic applications, whether transformers, chokes, or a combination of both.

In any case, it is a good design practice to keep the temperature rise of a switching power supply transformer to a low value, since most of these transformers are constructed using ferrites, which have thermal limitations. Ferrites have a Curie temperature of about 100°C. Curie temperature is the temperature at which a material changes its ferromagnetic properties and becomes paramagnetic.

Varnish impregnation may not be necessary with a ferrite transformer, since oxidization of the core due to moisture, as is the case with iron laminations, is not a factor. Also the acoustical noise which is associated with low-frequency transformers is not present in the ferrite high-frequency transformers, which generally operate above the human acoustical range. That is not to say that ferrite transformer assemblies may not generate mechanical or acoustical noise. They may, because whatever they are mounted on, acts as a sounding board. A phenomenon associated with ferrites, called magnetostriction, shortens or lengthens the part due to the applied magnetic field, which in turn causes mechanical resonance of the core assembly. In fact magnetostriction changes polarity, from negative to positive, as the temperature of the core rises. Therefore, care must be taken to use proper methods when mounting the transformer to the board, in order to reduce or eliminate any acoustical mechanical noise.

CHAPTER 5

Design Considerations of High Speed High Voltage Capacitor Charging Switched Mode Power Supply

5.1 Requirement. The main task is to design a high speed high voltage DC- DC regulator that will convert 48 VDC to 800 VDC and will charge a capacitor of 22 μf within 100 ms. All the prerequisites have so far been completed.

5.2 Overall Design. After thorough analysis of requirement and problem and studying all the popular topologies, it is decided that full bridge topology is the most suitable one to tackle the problem. As discussed earlier, in full bridge topology four switches work in two pairs. The two pairs of MOSFETs work diagonally. MOSFETs have been selected due to its fast switching speed and better safe operating area. Block diagram is shown below;

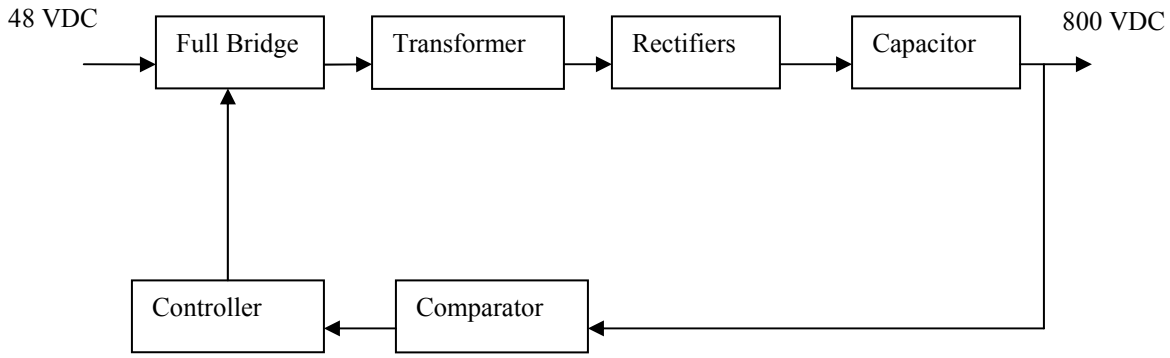

Figure 12. Block diagram of the regulator

Function and designing of each block will now be discussed in detail. Following are the basic available data;

Capacitor	C1	=	22 μf
Input voltage, V_{in}		=	48 VDC
Charging time, t_{ch}		=	100 ms
Output voltage, V_o		=	800 VDC
Switching frequency, f_{sw}		=	100 Khz
Output power, P_o		=	200 W
Assuming 90 % efficiency			
Input power, P_{in}		=	223 W

5.2.1 **Switching circuit**

The topology selected is full bridge as shown below;

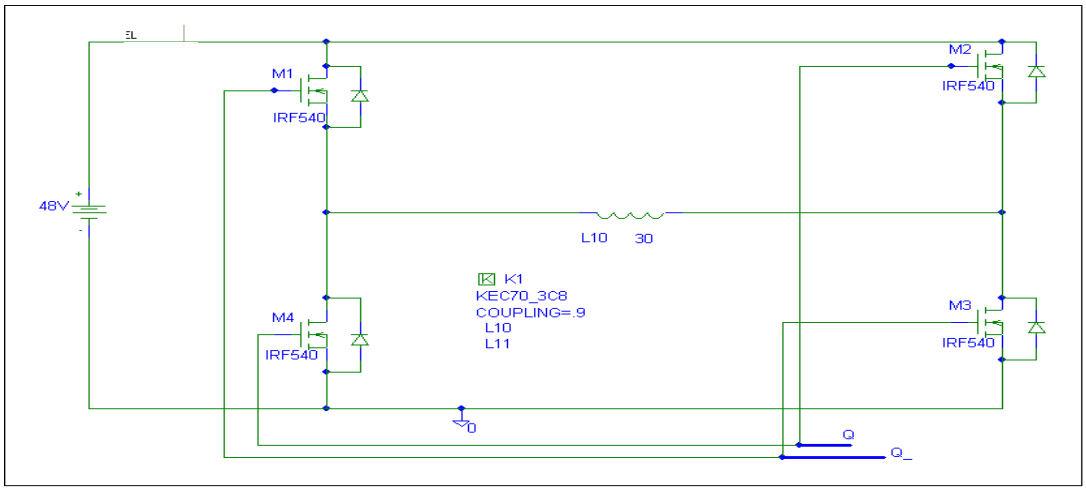

Figure 13 switching circuit

Four MOSFETs are connected and powered with 48 VDC as shown above. The two pairs M1,M3 and M2 ,M4 are working in parallel. Time period is 10 µs. Each pair switching time has been kept from 0.5µs upto 8 µs. The duty cycle has been controlled by PWM and soft start which will be discussed in more detail later on. First the pair M1, M3 is turned on that energizes the primary of transformer. Then second pair M2, M4 is turned on. In this manner the two pairs are switched on alternately. MOSFET, IRF 540 has been selected as this can handle a spike of 108 amperes whereas it can safely conduct 28 amperes continuously. Commutating diodes have been connected across each MOSFET to guard against reverse leakage current during off period. Transients at turn off are a problem that has to be kept at their minimum. The best way to control is implementation of snubbers. Both RCD and RC snubbers have been tried with a no of simulations. On the basis of the results finally RC snubbers have been incorporated due to its simplicity and in turn reduction of components. Although it is associated with little dissipation but it is affordable. Transients without snubbers can be well estimated from the simulation figure shown below;

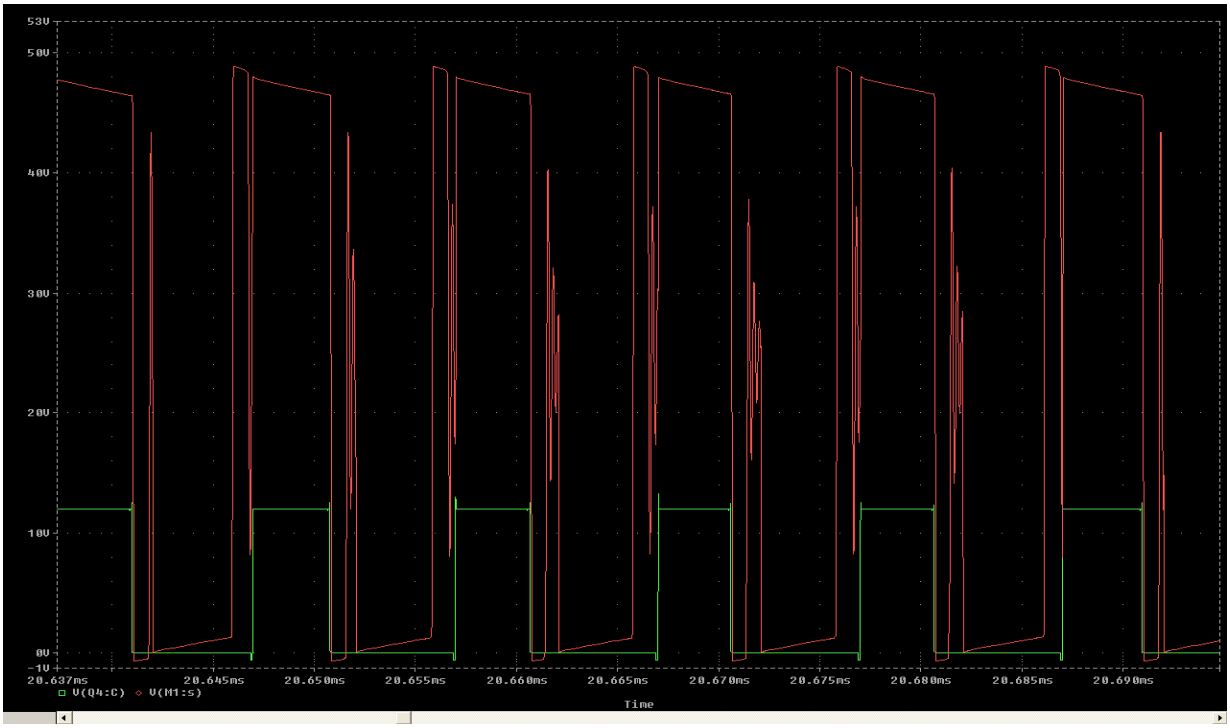

Figure 14 Pulses with ringings (without snubbers)

These ringings have greatly reduced after incorporation of snubber across each MOSFET as clear from the figure below;

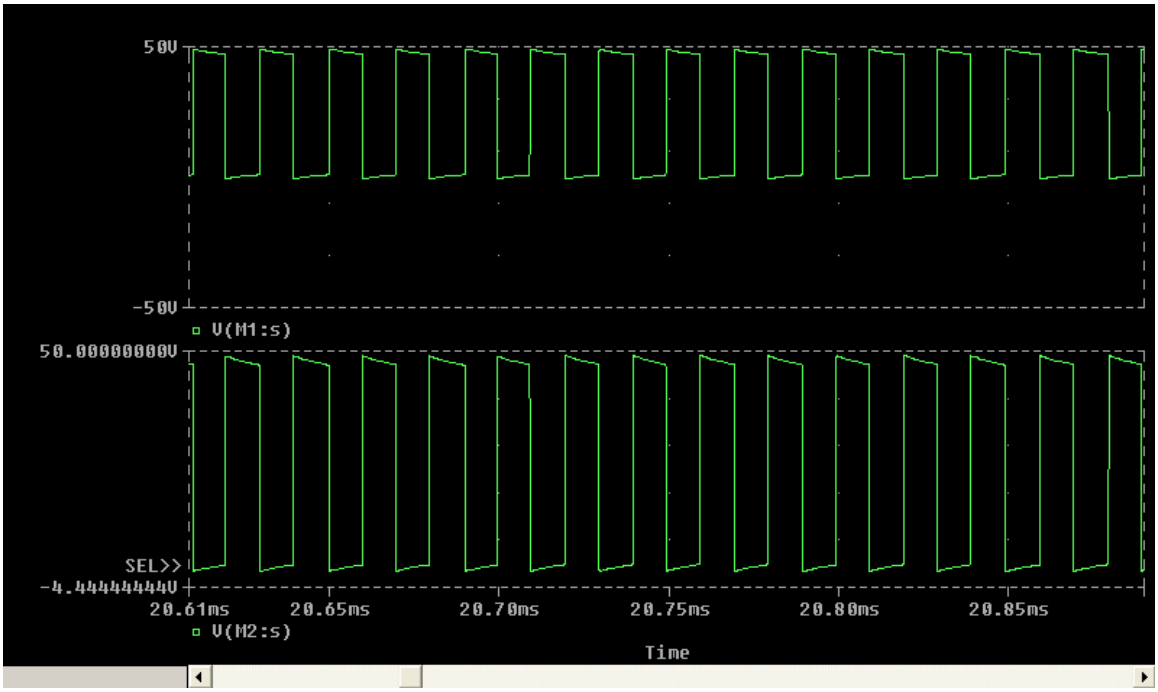

Figure 15. Pulses without ringings (with snubber)

5.2.1.1 **Incorporation of Snubber**. Snubber networks usually dissipative resistor-capacitor or diode networks are often fitted across switching devices and rectifier diodes to reduce switching stress and EM1 problems during turn-off or turn-on of the switching device. When MOSFETs are used, generally the snubber circuit is not required but still implementation is beneficial in the shape of improvement in safe operating area and reduction of ringings at turn off as can be judged from figure 15.

a. Snubber Component Calculations. Capacitor has been chosen such that the voltage across MOSFET, $V_{DSS,}$ is 70% of the rated value i.e. 48 v for IRF 540. Assuming that the primary inductance maintains the primary current constant during the turn-off edge, and assuming a linear decay of drain to source current in the MOSFET then the snubber current will increase linearly over the same period. Fall time of the source current is 43 ns as per manufacturer's datasheet. During the source current fall time of MOSFET, the current in capacitor will be increasing linearly from zero to maximum. Hence the mean current over this period will be $I_P/2$. We have known the maximum primary current I_P, and turn-off time, the value of the optimum snubber capacitor C_s is calculated as follows;

$$\frac{dv_c}{dt} = \frac{I_p}{2C_s} \qquad (5.1)$$

The 1/2 factor assumes a linear turn-off ramp on the source current, such that the mean current flowing into C_s is 1/2 the turn-off peak value during the turn-off period. Hence, if the source voltage is to be not more than 70% of V_{DSS} when the source current reaches zero then,

$$C_s = \frac{I_p * t_f}{2 * 0.7 V_{DSS}} \qquad (5.2)$$

Where I_P = maximum primary current, 18A.

t_f = MOSFET fall time, 0.043 µs

V_{DSS} = Drain to source rated voltage of MOSFET

Putting values we get,

C_s = 11.52 nf

b. Turn off dissipation in MOSFETs. C_s and MOSFET see the same mean current and voltage during the turn off period, hence the dissipation in the MOSFET during the off period will be the same as the energy stored in the C_s at the end of the turn off period hence,

$$P_{off} = \frac{1}{2} C_s * \left(0.7 V_{DSS}\right)^2 f \qquad (5.3)$$

Putting values we get

P_{off} = 0.85 mW

c. Snubber Resistor. The snubber discharge resistor R_s is chosen to discharge the snubber capacitor C_s in the minimum selected "on" period. The maximum "on" period is 8 µs. The CR time, constant should be less than 50% of the minimum "on" period to ensure that C_s is effectively discharged before the next "off' period. Hence

$$R_s = \frac{t_{off}}{2C_s} \qquad (5.4)$$

R_s = 67 ohm

A value of 78 ohms gave best results during simulations.

5.2.1.2 Blocking Capacitor. It is film type nonpolar capacitor connected in series with primary of transformer. This capacitor is capable of handling the full primary current. The purpose of this capacitor is to counter the volt –second unbalance that has been created due to very slight unmatched turn off timings. As if this unbalance is allowed to drive the transformer, flux walking occurs which results in core saturation.

$$C_b = I * \frac{dt}{dv} \qquad (5.5)$$

Where I = Primary current

dt = MOSFET off time

dv = 10 – 20 % of impressed voltage

= 1.39 µF

It is another benefit of full bridge topology that this flux imbalance normally does not occur. During many simulations, no marked effect was noticed as core saturation hardly occurred without insertion of this capacitor. A number of simulations were carried out without this coupling capacitor with correct outputs.

5.2.2 **Transformer Design.** It is the most tricky yet very important part of regulator design. Correct designing of transformer has very significant effect over the performance of the regulator. Before designing the transformer certain calculations are required as depicted below;

$$I_{out} = \frac{P_{out}}{V_{out}} \qquad (5.6)$$

$$= \quad 200/800$$

$$= \quad 0.25 \text{ Amp}$$

$$I_{in} = \frac{P_{in}}{V_{in}} = 223/48 = 4.65 \text{ Amp}$$

$$I_{rms} = \frac{1.4P_{out}}{V_{in}} = \quad 1.4 \text{ x } 200/48 = 5.83 \text{ Amp}$$

We have the basic energy equation for capacitor

$$E = \tfrac{1}{2} CV^2 \qquad (5.7)$$

$$= \quad 7.04 \text{ Joules}$$

Now

$$E = VQ \qquad (5.8)$$

$$= \quad Pt$$

$$P = \quad 7/80 \text{ x } 10^{-3}$$

$$P = \quad 88 \text{ watts}$$

To be safer and protect the transformer from heating and optimally loading the regulator at its 50%, we suppose the power of regulator as 200 watts.

To calculate the current in the primary side:-

$$I_p = \frac{1.6P_{out}}{V_{in}} \qquad (5.9)$$

$$I_p = \frac{1.6*200}{48}$$

$$I_p = 6.67 \text{ A}$$

The transformer has been over wound for 1000 V output. The benefit of over wounding is that the desired voltage of 800 V has been achieved earlier than normal. It can be assess well that when the transformer was wound for 800 V output, this voltage was achieved in 98 ms and when the same transformer was over wound, 800 V were achieved

below 50 ms time. The charging time has been delayed to 84 ms, just to cut down the initial rush of current

Transformer has been designed in following steps.

Step 1. Core Geometry and ferrite material

For this design Ferroxcube EC Core and ferrite of 3C8 material has been chosen. EC core is used for higher power levels with more confidence. EC Core is a compromise between Pot core and E-E Core, Combining the advantages of both the Cores. EC-70 core has been selected which is capable of handling power up to 5 KW.

Step 2. Working B_{max}

The saturation flux density for ferrite 3C8 is 3300 G. Half of the B_{sat} i.e. 1600 G is selected as working B_{max} . This choice guarantees that transformer will not saturate.

Step 3. Maximum Primary Current

The transformer primary has to conduct the maximum possible current at the low input side i.e,

$$I_p = \frac{1.6 P_{out}}{V_{in}}$$

$$I_p = \frac{1.6 * 200}{48}$$

$$I_p = 6.67 \text{ A}$$

Step 4. Core and Bobbin Size

Current density of 400 c.m/A has been selected for calculations. From the catalogue of Philips,

a. Effective area, $A_e = 2.79 \text{ cm}^2$

b. Core area, $A_c = 4.77 \text{ cm}^2$

so $A_e A_c = 13.308 \text{ cm}^4$

Step 5. Wire Size

Since 400 c.m/A has been chosen, the wire current density for this design, therefore the primary winding wire size is,

6.67 x 400 = 2668 c.m

From the wire specification table-1, shown previously, AWG 15 is sufficient.

Step 6. Primary no of turns

To calculate the primary number of turns, we have the formula

$$N_p = \frac{(V_p) \times 10^8}{K f B_{max} A_e} \qquad (5.10)$$

Whereas

V_p = impressed primary voltage, V

f = frequency, Hz

N_p = Primary number of turns

B_{max} = Max flux density, gauss

K = 2, core factor

So $N_p = \frac{48 \times 10^8 \ldots\ldots\ldots\ldots\ldots}{2 \times 100 \times 10^3 \times 1600 \times 2.79}$

= 5.37 □ 6 turns

Step 7. Number of layers

From the table of wire specification it is clear that 15AWG has a maximum diameter of 0.06 in, for double insulation wire. From catalogue the bobbin width is 0.11 in

So

0.11/0.06 = 1.83

It means the 6 turns wire be accommodated in 2 layers

Step 8. Transformer secondary turns

We have

$$\frac{N_p}{N_s} = \frac{V_p}{V_s} \qquad (5.11)$$

$$N_s = \frac{N_p V_s}{V_p}$$

= 6 x 1000/48

N_s = 125 turns

The secondary RMS current is 0.28 amp

So 0.28 x 400 = 112

So AWG 29 is sufficient and numbers of layers are

= 0.11/0.0133 = 8.27□ 9 layers

After winding the transformer, the safe gap of 4 mm is still left at both the sides. Both the windings will be interleaved so as to reduce the effect of leakage inductance.

Simulation results of voltage and current at the primary of transformer are as shown below;

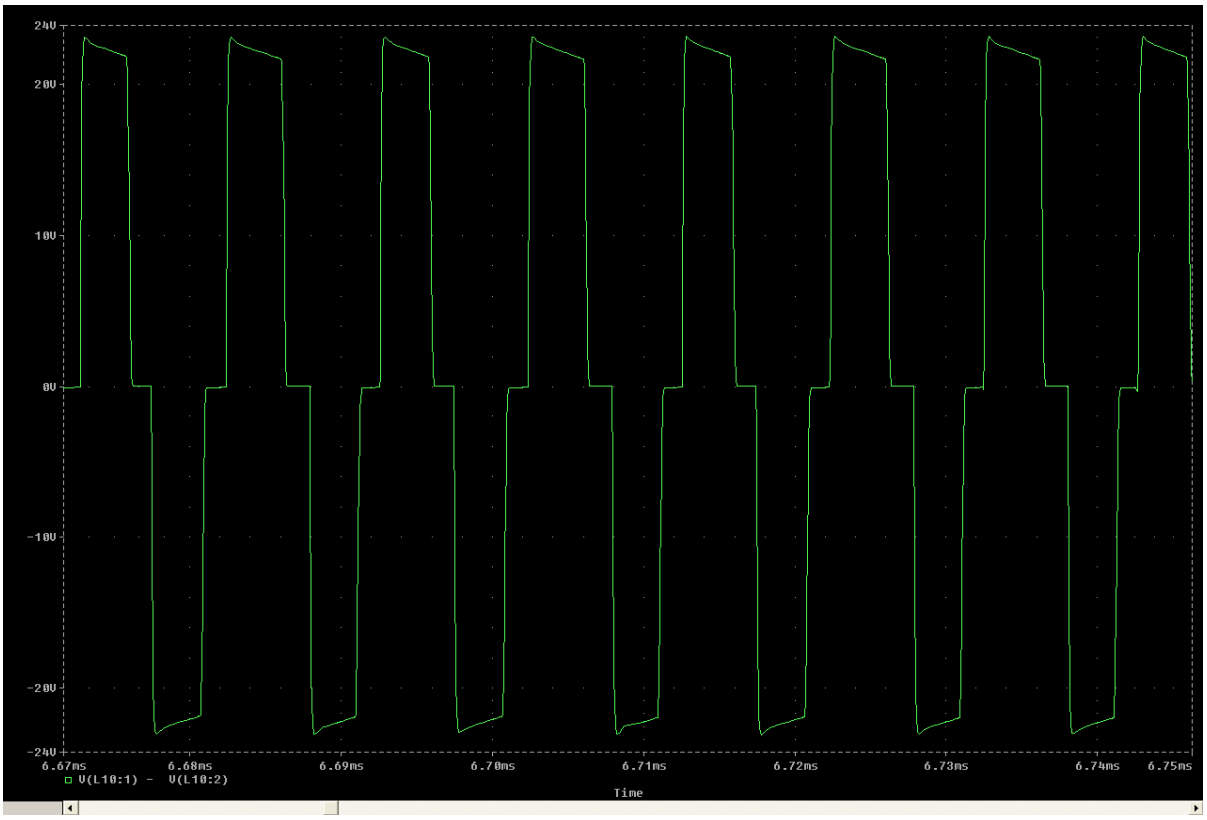

Figure 16. Voltage pulse at primary of transformer

5.2.2.1 Linear Coupling. The simulations were carried out through PSPice. Initially a linear magnetic coupling was used. With linear coupling initial current surge was more than 200 amps and later on I_{pk-pk} started from 80 amps and came down to 30 amps at the end of charging time. With this much high current choice and number of MOSFETs required ware difficult. The wave shapes of other parameters were also not fulfilling the requirement like slope of current wave shape, appearance of unnecessary transient spikes and unpredictable behavior of the circuit Whereas after replacing the linear coupling with EC-70-3C8 ferrite core, the primary current reduced remarkably i.e. I_{pk-pk} started from 19 amps and finished at less than 5 amps. Definitely low current mean low losses, low heat and increased efficiency. With this current ratings MOSFETs are also easily available. The

comparison can be well judged from figure 18 and figure 19 that current has reduced after replacement of linear coupling with nonlinear coupling;

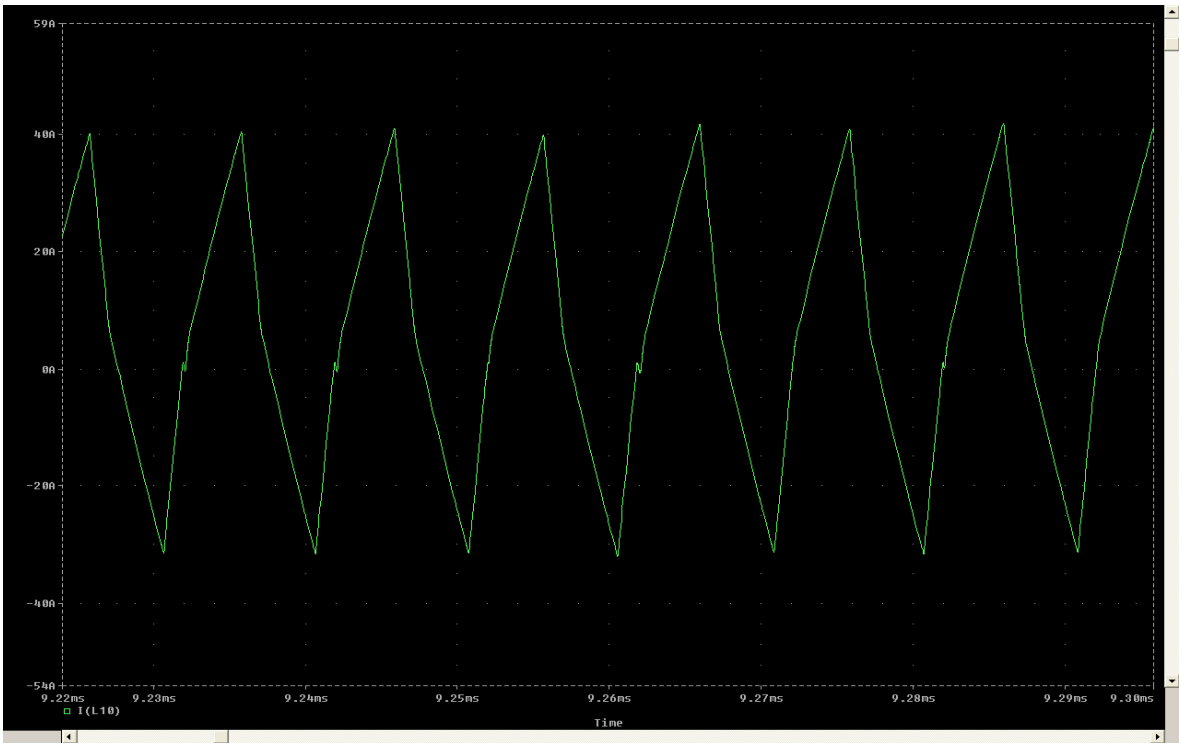

Figure 17. Current with linear coupling

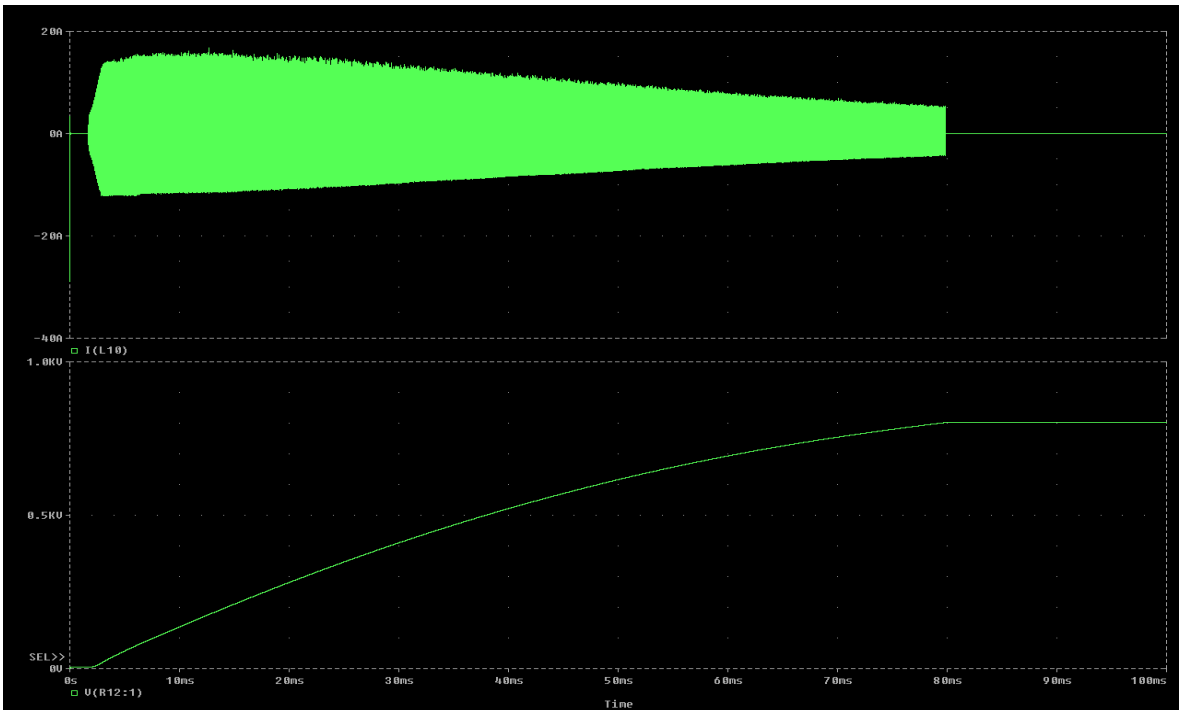

Figure 18. Current with nonlinear coupling

The MOSFETs used in the circuit are capable of conducting an initial surge of current up to 108 amps and later on 28 amps continuously. So it means the power switches will not be stressed. Efforts have been made to design and select components in such a manner that loading is just 50%. This will increase performance, life and reliability of the regulator.

5.2.2.2 Primary Copper loss

Mean turn length = π x d (5.12)

= 3.14 x 3.05

= 9.6 cm / turn

Total length of primary winding,

= 6 x 9.6 = 57.6 cm

Resistance per cm for AWG 15 = 3.181/30000

= 0.0001 Ω / cm

Total resistance = 57.6 x 0.0001

= 5.7×10^{-3} Ω

Copper loss = I^2R = 0.26 W

5.2.2.3 Secondary Copper loss

Mean turn length = π x d

= 3.14 x 3.05

= 9.6 cm / turn

Total length = 9.6 x 125

= 1200 cm

Resistance per cm for AWG 29,

= 81.21/30000

= $2.7 \times 10^{-3}\ \Omega$

Total resistance = $2.7 \times 10^{-3} \times 1200$

= 3.24 Ω

Copper loss = I^2R = $(0.28)^2 \times 3.24$

= 0.25 W

Total copper loss = 0.26 + 0.25 = 0.51 W

5.2.2.4 Core loss

From chart for 100 KHz, EC-70 and 1600 G flux density,

Core loss = 34 mw/g

Total core Wt = 125 g

Total core loss = 4.25 W

Total loss = Copper loss + Core loss + Snubbers loss + MOSFETs loss

= 0.51 + 4.25 + 8.2 + 0.054+4

= 17 W

$$\text{Efficiency} = \frac{\text{output power x 100}}{\text{Output power + losses}} = \frac{200 \times 100}{200 + 17} = 92\ \%$$

5.3 **Output Portion**. This portion is responsible for conversion of AC, got from secondary of transformer, into DC through a full wave rectifier. All the four diodes used are of very fast recovery type. Another innovative thing is implementation of a freewheeling diode. This diode provides a path for reverse current of output inductor when the transformer pulses are not there. It is an aid to prevent sharp rise of current at the time when regulator is switched on.

To get the feedback, a potential divider has been formed. To get 12 v for feedback, a 152 k resistance has been connected in series with 10 M ohm resistance as follow;

$$V_{pd} = \left(\frac{R_1}{R_1 + R_2} \right) * V_{out} \qquad (5.13)$$

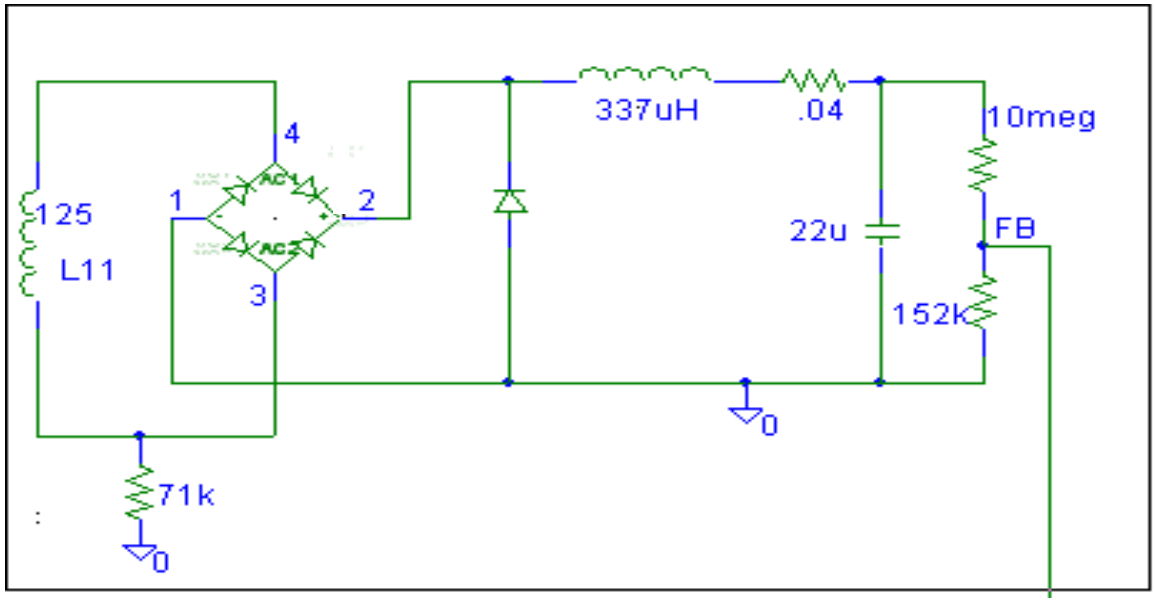

Figure 19. Output portion

Required output of 800 VDC across the charging capacitor of 22 uf has been achieved within 100ms. Two small resistances having values .01 ohm and .03 ohm have been added to cater for resistance of secondary portion of circuit. Voltage and current pulses at the secondary of transformer are shown as follow;

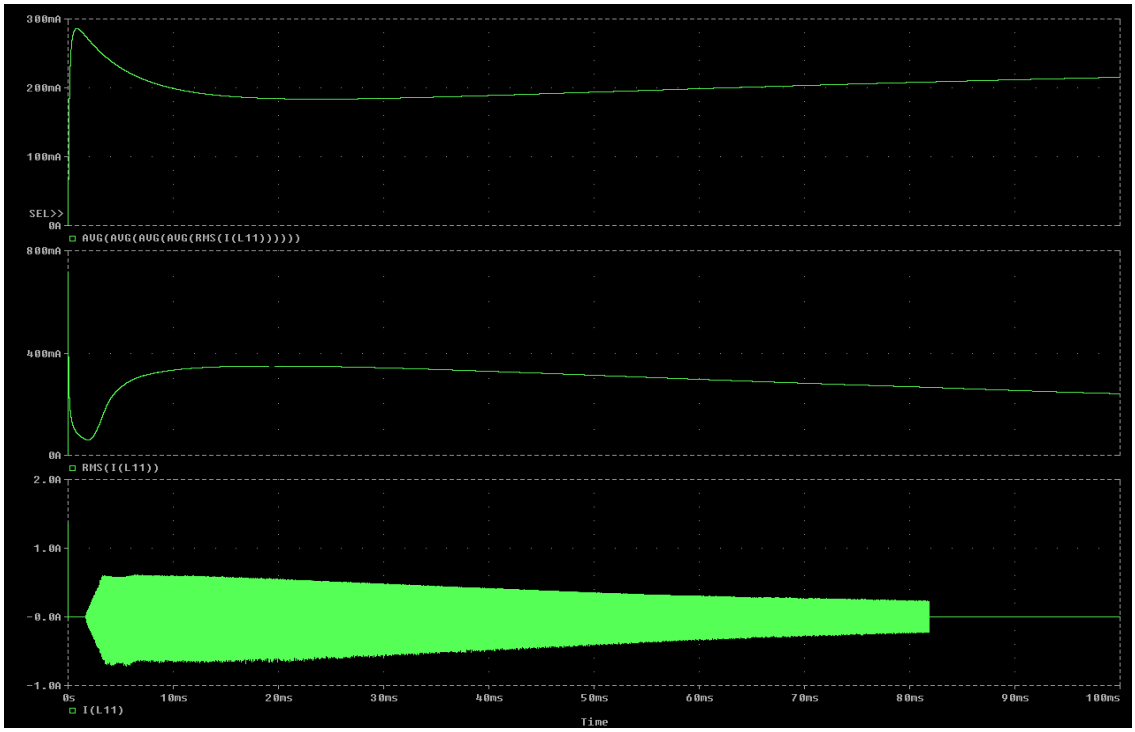

Figure 20. Secondary, overall and rms current

5.3.1 Output Power Inductor Design

Switching power supply designs use an inductor as part of their output filtering configuration. The presence of this inductor is two-fold: first it stores energy during the off periods in order to keep the output current flowing continuously to the load, and second it aids to smooth out and average the output voltage ripples to acceptable levels.

There are a variety of cores that can be used in the design of inductors. The most popular materials used in present days high frequency switching designs are ferrite cores, iron powder cores, and molypermalloy (MPP) cores. All of these cores are good for power inductor designs, and basically the criterion of choosing one versus the other is based on factors such as cost, weight, availability, performance, and ease of manufacture. Iron powder and MPP cores are generally offered in toroid forms, and they are well suited for power chokes because of the following characteristics:

a. High saturation flux density B_{sat} up to 8000 G.

b. High energy storage capability. $V_{pd} = \frac{R_d}{R_o + R_d} * V_{out}$

c. Inherent air gap eliminates the need of gapping the core.

d. Wide choice of sizes.

Ferrite cores, on the other hand, have to be gapped because of their low saturation flux density B_{sat}, they are more temperature sensitive, and they tend to be bulkier. But if pot cores are used for output chokes, radiated EMI will be reduced because of the inherent shielding properties of the pot core. Also, ferrite chokes are easier to wind, especially if heavy gauge wire is involved.

5.3.1.1 Deriving the Design Equations. In the output section of a full bridge converter inductor L12 depicts the output inductor. The voltage at left side of the inductor is E_{in} and at the right is $E_{out.}$ In the case of the PWM full-bridge converter, the voltage E_{in} is roughly 1.25 times the value of the output voltage E_{out} at the maximum primary input voltage V_{in}. Therefore, $E_{in} - E_{out} = E_{L.}$ Average load current is I_{out} with ripple ΔI_L.

Voltage across the inductor is given by

$$V_L = L\frac{di}{dt} \qquad (5.14)$$

Since

$$V_L = E_{in} - E_{out}$$

And

$$di = \quad \Delta I_L$$

Then Eq. 5.14 my be written, solving for L, as follows:

$$L = \frac{\left(E_{in} - E_{out}\right)\Delta t}{\Delta I_L} \qquad (5.15)$$

The time interval Δ_t is equal to the dead time, t_{off}, which occurs between alternate switching half cycles. The inductor must be designed to store enough energy to provide continuous output current during the notch periods.

Expressing Δ_t in terms of secondary voltage E_{in} and E_{out} yields

$$t = t_{off} = \frac{\left(1 - \frac{E_{out}}{E_{in}}\right)}{2f} \qquad (5.16)$$

$$t_{off} = \frac{\left(1 - \frac{800}{1000}\right)}{2*100000}$$

$$t_{off} = 1\ \mu s$$

Here f is the converter's frequency, while the factor ½ relates the notch time t_{off} to the entire switching cycle, since the total switching period encounters two notch time

intervals. In order to keep low inductor peak current and good output ripple, it is recommended that ΔI_L not be greater than $0.25I_{out}$.

Based on the above, Eq. 5.15ay be rewritten as follows.

$$L = \frac{E_L * t_{off}}{0.25 I_{out}} \qquad (5.17)$$

$$L = \frac{200 \text{ x } 1 \text{ x } 10^{-6}}{0.25 \text{ x } 1.9}$$

$$L = 421 \ \mu h$$

After several simulation trials the value of 337 μh gave best results. It means that Eq.5.17 indicated an inductance value which is very close to the practical value and after a little bit fine tuning it is will work in actual application. After the inductance has been calculated, the core size and core material is being chosen in order to complete the design.

5.3.1.2 Design procedures using a ferrite core. The design procedure is analytical and helped a lot in designing optimum filter choke.

The inductor value L capable of delivering output current ΔI_L during t_{off} is

$$L = \frac{E_L * t_{off}}{0.25 I_{out}} = 337 \ \mu H$$

Minimum size of core is selected using the following equation

$$A_e A_c = \frac{(5.067)\ 10^8\ (LI_{out}D^2)}{K\ B_{max}} \qquad (5.18)$$

Where K = 0.8 for bobbins

D = diameter of wire to be used

A_e = core effective area

A_c = bobbin winding area

Current density of 400 c.m. / A is chosen. Then for 1.9 A, the wire is 400 x 1.9 = 760 cm. which corresponds to no.21 AWG wire, with a maximum diameter of 0.0314 from Table 1.

Also selecting a B_{max} = 1600 G, the A_eA_c product is

$$A_e A_c = \frac{5.067 \text{ x } 10^8 \text{ x } 337 \text{ x } 10^{-6} \text{ x } 1.9 \text{ x } 0.0314^2}{0.8 \text{ x } 1600} = 0.25 \text{ cm}^4$$

From ferrite catalogs the 2616 pot core $A_e = 0.948$ cm^2 and $A_c = 0.407$ cm^2, which yields $A_eA_c = 0.386$ cm^4. Because the inductor experiences a large dc bias, it is necessary to gap the core in order to avoid saturation.

The length of the gap is

$$l_g = (0.4\pi LI^2_{out})10^8/A_eB^2_{max} \quad (5.19)$$

$$= \quad 0.4 \text{ x } 3.14 \text{ x } 337 \text{ x } 10^{-6} \text{ x} 1.9^2 \text{ x } 10^8 / 0.948 \text{ x } 1600^2$$

$$= 0.0629 \text{ cm}$$

Since the air gap interrupts the magnetic circuit twice, if a spacer is used to provide the gapping, the spacer thickness will be

$$l_g / 2 = 0.0314.$$

On the other hand, the total gap length must be used if only the center leg is gapped.

Now the number of turns will be calculated.

$$N = B_{max} l_g / 0.4\pi I_{out} \quad (5.20)$$

$$= \frac{1600 \text{ x } 0.0629}{0.4 \text{ x } 3.14 \text{ x } 1.9} = 42.17 \text{or } 43 \text{ turns}$$

Improvements can be made in the actual application, which could include increasing the number of turns for better filtering or increasing the number of conductors to reduce heating effects.

5.4 **Feedback loop**

The purpose of feedback is monitoring the output voltage level. In this case negative feedback system has been adopted. A comparator LP239/5_1/T1 has been selected for this purpose. A potential divider has been established at the out put with following relation;-

$$V_{pd} = \frac{R_d}{R_o + R_d} * V_{out} \quad (5.21)$$

$$V_{pd} = \quad 152\text{k x } 800/(152\text{k}+10 \text{ mega})$$

$$= \quad 11.98 \text{ V} \sqcup 12 \text{ Volts}$$

These 12 volts have been applied to the negative of the comparator. A reference of 12 v has been applied to + ive of the comparator, output of this comparator is given to one of the input of AND gate, CD 4081B. Other input of this gate is, output of soft start.

When the output voltage of regulator reaches 800 V, by that moment the voltage at the mid point of R_{12} and R_{42} is 12 V. This 12 volt when reaches at the – ive terminal of comparator i.e. now 12 V each are at the two terminal of the comparator and so the comparator will give a low output. This low output when reaches the AND gate, it gives a zero output i.e. the pulses of PWM are no more transmitted. As soon as the output of regulator is lowered than 800 V, difference is created between the two inputs and gives a

high output that in turn deliver the AND gate a high signal and AND gate starts passing on the pulses of PWM.

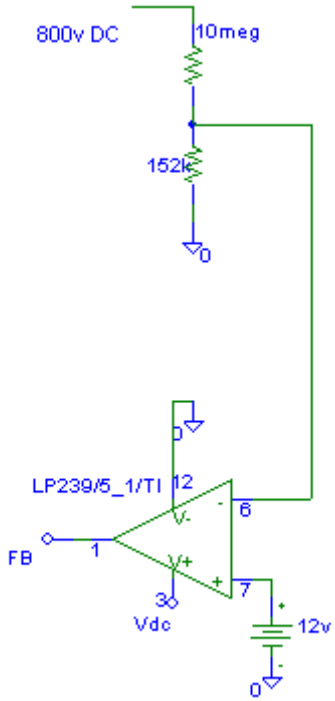

Figure 21. Feedback loop showing comparator

As clear from the figure above, comparator simply compares the output taken out from potential divider with a reference voltage of 12 VDC. Simulation of feedback loop shows high state of comparator till 800v. At 84 ms as the voltage exceeds 800 VDC, comparator output shifts to low states seizing PWM pulses. High state pulses occurs at intervals where the output lowers from 800 v in milli volts thus ensuring a constant 800 VDC output. The two states are shown below;

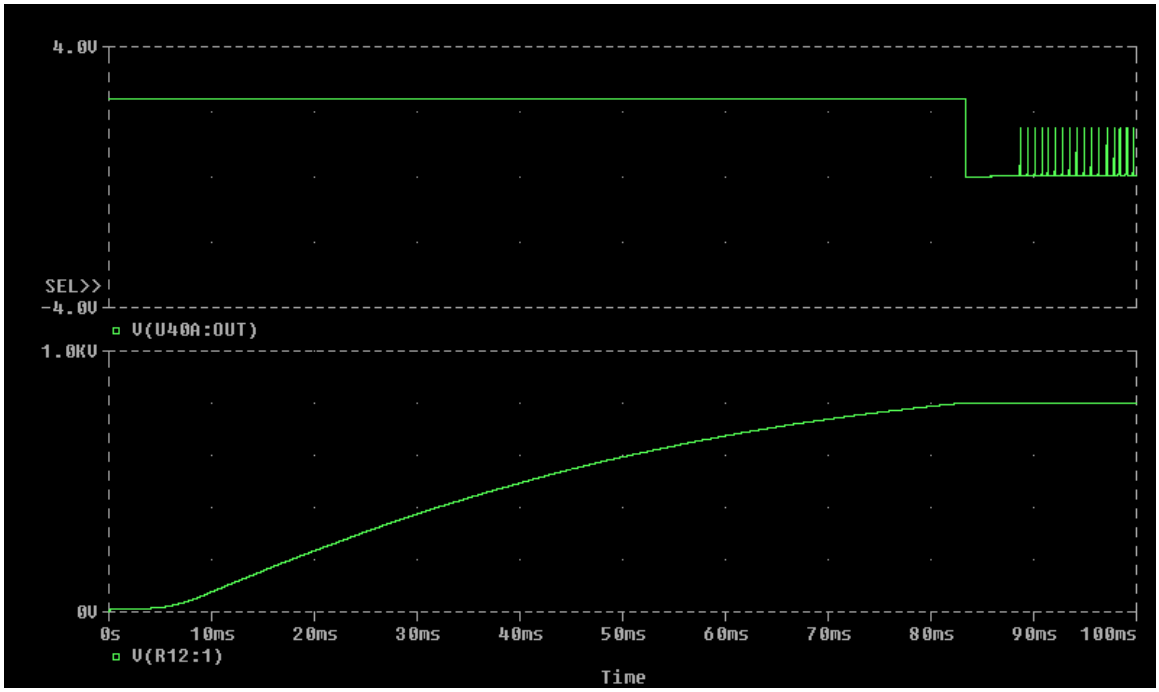

Figure 22. Feedback comparator states with voltage

Earlier the feedback was incorporated through hysteresis band control. It was adjusted in such a way that the output of the comparator remained high till 800 VDC. At 800 VDC the comparator output is lowered and this low state inhibited PWM pulses. When the charge held by capacitor is discharged, adjustment was so that when the voltage fall down to 100 volt then the PWM was triggered to start pulses. This arrangement was replaced with simple comparator due to one major flaw i.e. after 30 ms the output voltage normally starts dropping. So if the regulator is kept undischarged for a longer time then a considerable voltage drop will be there turning the held voltage insufficient to fulfill the requirement.

5.5 **Soft start.**

In most power supplies design it is desirable to introduce certain delay during start up in order to avoid output overshoots and transformer saturation problems at turn on. Circuits which are employed to perform this task are called “soft start circuits”, and in general they consist of an RC network which allows the PWM control circuit output to increase from zero to its operating value very softly.

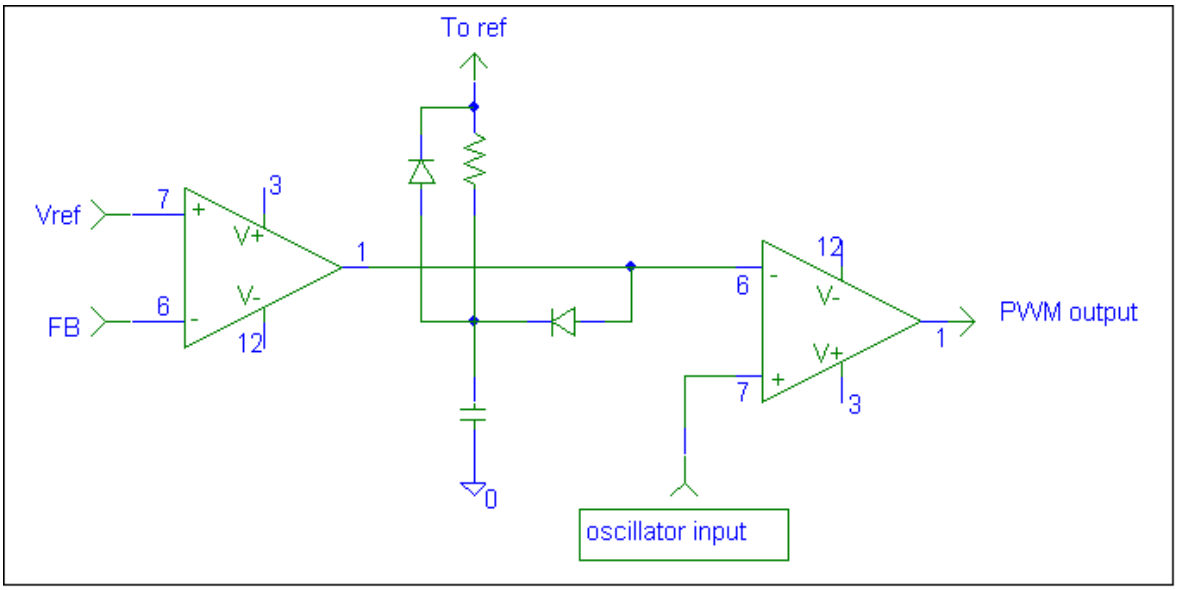

Figure 23. Soft start circuit

To prevent the circuit from inrush current at the time when the regulator is switched ON, some controlling means are required. The target has been achieved by induction of soft start circuit. An oscillator and a linear ramp generator have been connected to negative and positive of the operational amplifier. Potentiometer and ramp generators are connected to same terminal of the OP amplifier. A diode has also been incorporated in the path of ramp linear generator in reverse direction. The purpose of this diode is that at the time when the supply is just switched on, the output is held to ground through the diode. Current will conduct through diode till 0.7 V. After 0.7 V the output of potentiometer and linear ramp generator will be passed on the input of op amp. The slope of the linear ramp generator has been so adjusted that it will gradually develop voltage from o to 12 volts within 20 ms. This will ensure gradual increase of the PWM wave form at the output of comparator, and consequently a soft start of the switching element is initiated

It is due to this soft start that 0.5 % to 70 % pulse width has been achieved within 20 ms. The pulse width can be extended up to 90 % but our requirement is conveniently fulfilled with a max pulse width of 70 %. By varying the pulse width duration, achievement of final output is possible i.e. the required output of 800 V can be achieved from 23 ms till 84 ms. The 800 V within 84 ms have been kept intentionally to cater for the unforeseen delays in different components. The safety margin of 16 ms is sufficient to get required output within 100 ms. Simulation of formation of pulses have been shown as follow;

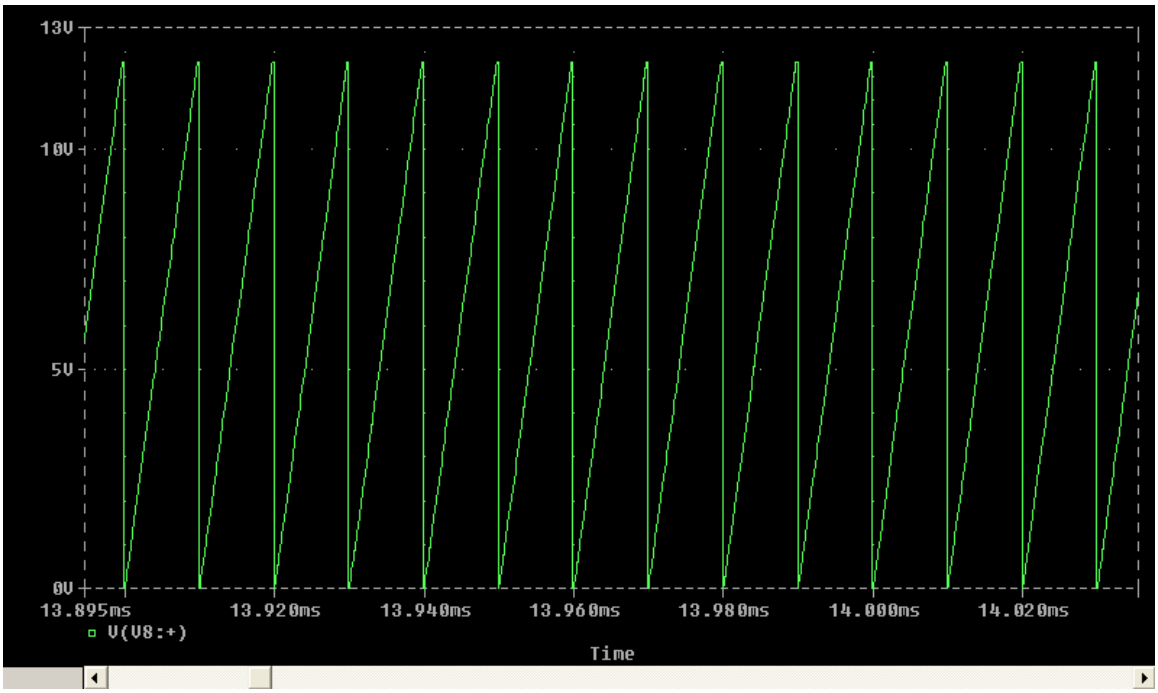

Figure 24. Oscillator pulses

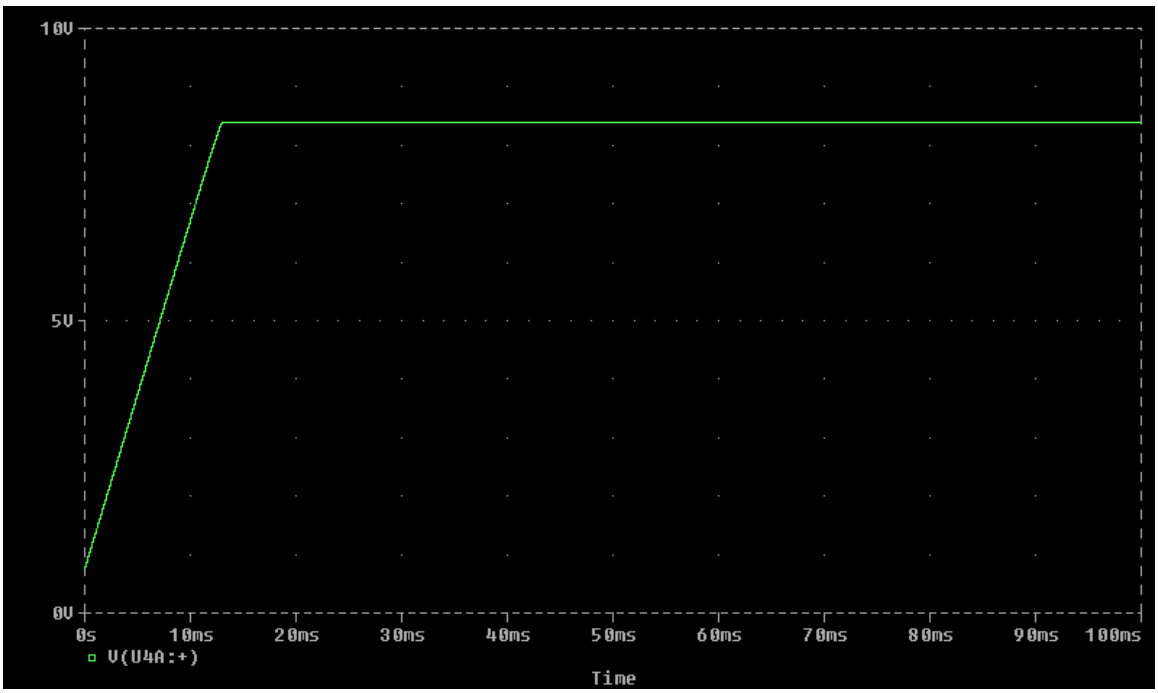

Figure 25. Reference voltage through diode and capacitor

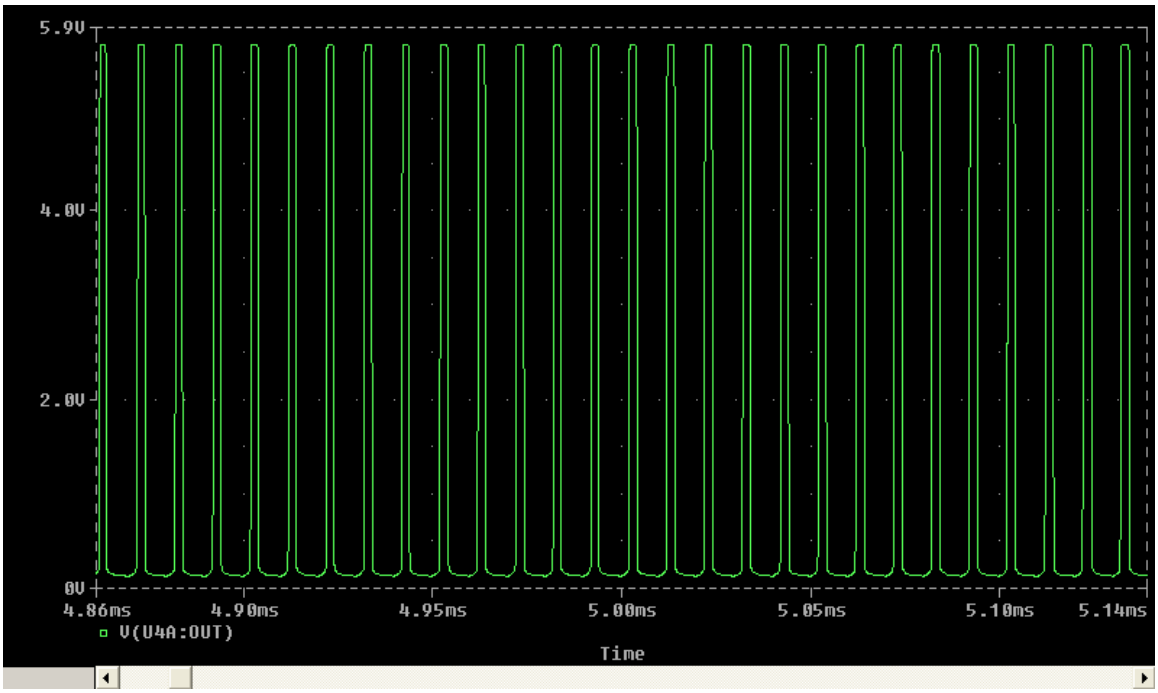

Figure 26. Initial pulses of PWM (5% pulse width)

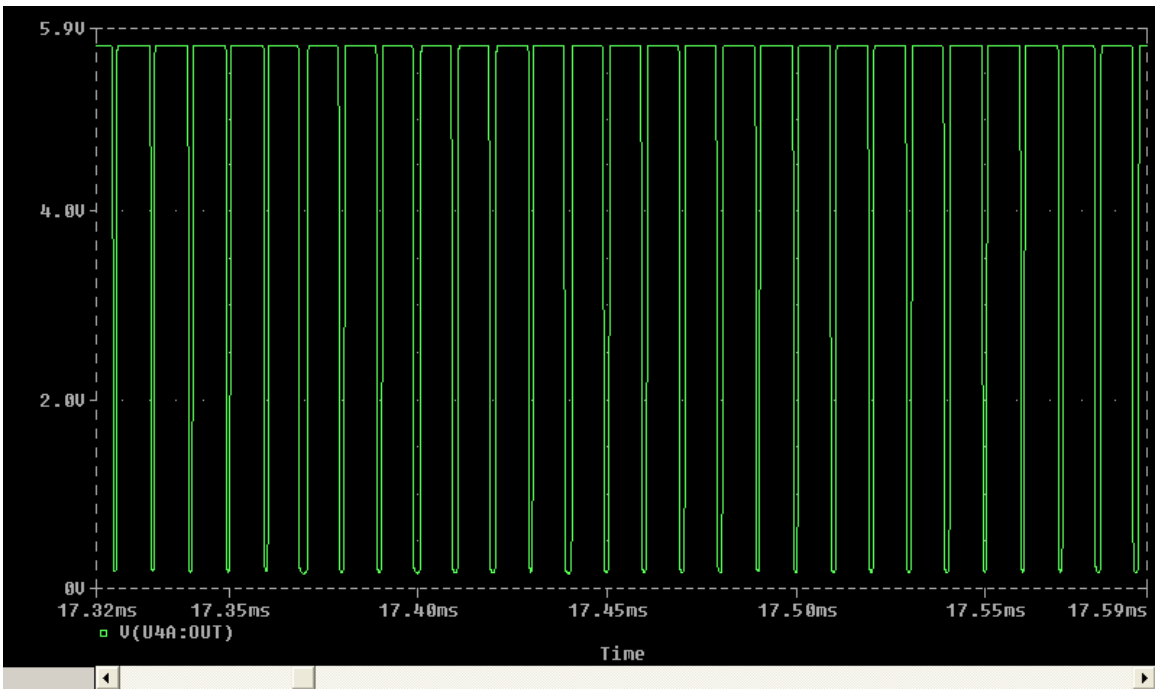

Figure 27. Later stage PWM pulses (80% pulse width)

5.6 **Pulse steering**

The protection of MOSFETs is very necessary by ensuring properly pulsing each pair of MOSFET as if both pairs are switched ON simultaneously then due to cross over current all the four transistors will be immediately destroyed. The problem has been handled by designing two NAND gates, CD 4081B, supplied with pulses from PWM. Clock pulses have same timing as the switching frequency time period i.e. 10µs. clock pulses to one of the gate are supplied through an inverter when clock pulse is high for one AND gate, it is low for the other so at that time only the AND gate with high clock pulse will transmit the "PWM" pulses to one pair of MOSFETs. In this way the PWM pulses are alternately steered to the two pairs of MOSFETs. This arrangement is quite safe and there is no chance of conduction of all the four MOSFETs simultaneously. The arrangement is shown in figure 28 below;

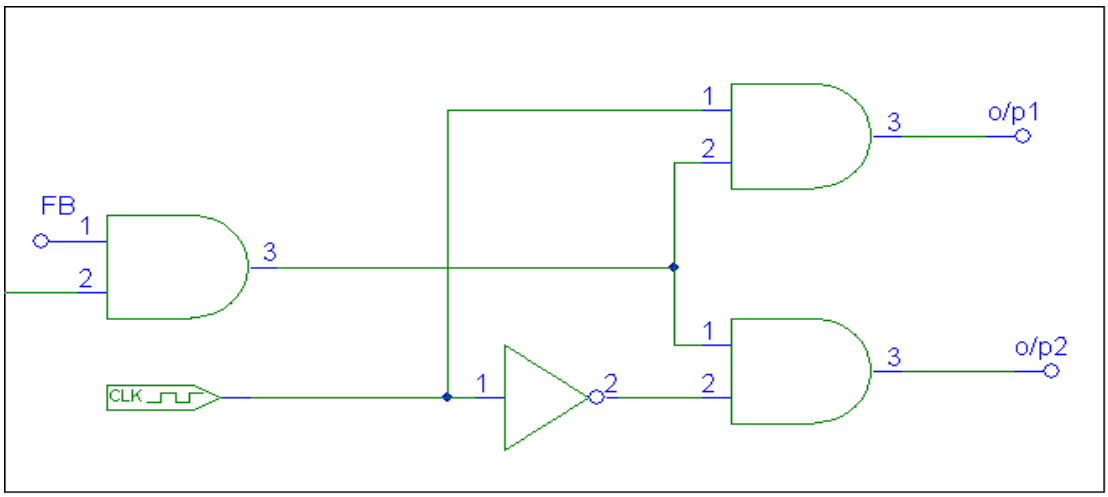

Figure 28. Pulse steering

Simulation of output of the AND gates and clock pulses are shown in figure 29. The simulations show the sequence of pulse steering sent to the two pairs of MOSFETs alternately. Figure 28 also shows that when feedback is turned from high to low, the two outputs of NAND gates are inhibited and switching of the MOSFETs is stopped.

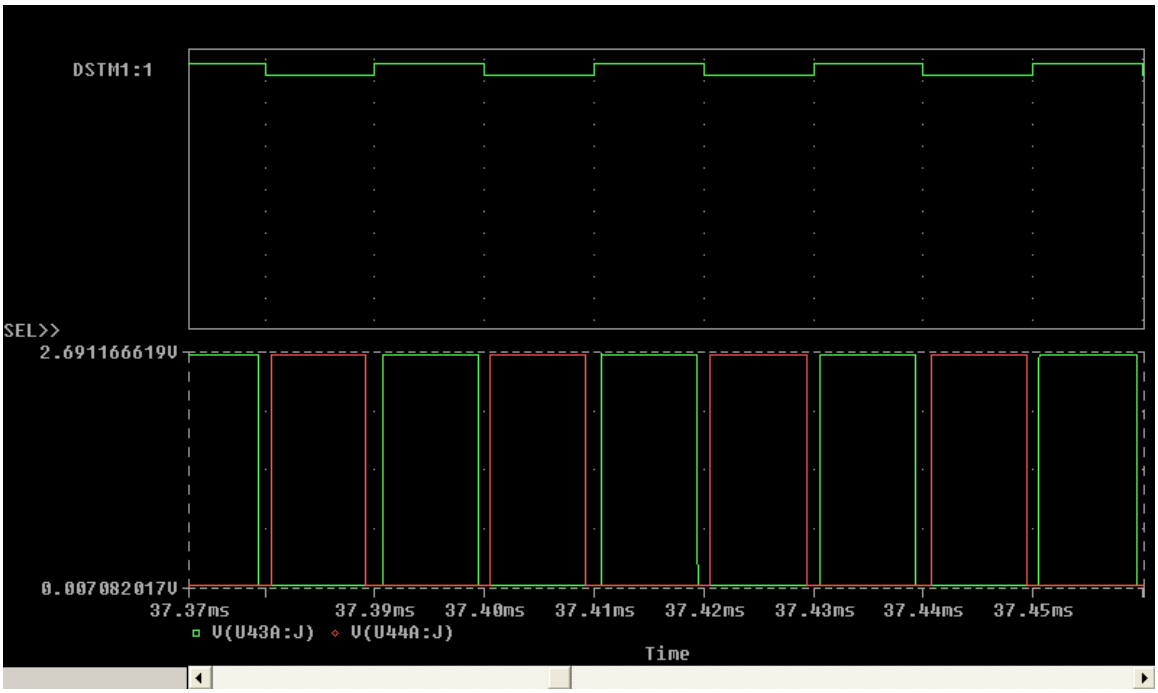

Figure 29. Steering of pulses and clock pulses

Earlier the output of PWM was supplied directly to one pair of MOSFETs and for the other pair a delay of 5µs was given, but there was always a risk, as in case of failure of this 5µs delay, all the four transistors would have conducted simultaneously, rendering immediate destruction.

CHAPTER 6

Conclusion and Future Work

6.1 Conclusion. Designing of this regulator was quite difficult in achieving the output and desired wave shapes with specified parametric limitations. Desired results have been successfully managed, initially through very time consuming simulations and later on by fabrication. Charging of output capacitor within 100 ms associated with controlled inrush current were especially very hard task. Different parameters wave shapes like current, voltage and MOSFETs pulses etc are very closely matched to standard shapes of particular waveforms.

The full bridge topology selected for this particular requirement was justified as proved after achievement of desired results. Output of 800VDC has been achieved in less than 50 ms but to curtail primary inrush current, different techniques have been applied and time has been lengthened till 84 ms. This has also ease out stress over the switches. Optimal designing of transformer and output inductor was also a challenging task that has been finalized after repeated simulations and carrying out slight arbitrary adjustment in values of some components. Also implementation of a free wheeling diode at the secondary side has helped in providing path for reverse current of output inductor. This diode has also greatly aided in controlling inrush currant at the time when regulator is switched ON.

It is also clarified that the designing is not final and it can be improved further by the introduction of certain ICs which can reduce the size and regulator will become more compact and light weight.

6.2 Future Work. Designing of this step up regulator took almost one year to complete. Like any other work, this regulator has also ample room for future work. These enhancements were possible but due to paucity of time this could not be done. Some of the areas are highlighted below;

6.2.1 Introduction of electromagnetic and radio frequency interference United States and international standards for EMI-RFI have been established which require the circuits to minimize the radiated and conducted interference to an acceptable level. It is therefore required to rehash the area of design where some unacceptable deviation exists from FCC Docket 20780 and VDE standards.

6.2.2. Over voltage and over current protection. Both of these parameters are of prime importance as any increase in voltage or current above rated values of components

and over all system can destroy the circuit instantly. To protect the circuit from such hazards, some arrangement is required.

6.2.3 Reduction of primary current. Presently primary current is ranging between 19 to 5 amperes with rms current around 7 amperes. It will be highly desirable if rms current is reduced to less than 4 amperes. This will reduce current stress over semiconductor switches of the regulator and transformer size will also be reduced that will in turn make the power supply more compact

6.2.4 Designing of transformer. Transformer may be redesigned with 3F material instead of 3C8 due to its superior characteristics and small B-H curve area.

REFERENCES

1. Georgre C.Chryssis, " High-Frequency Switching Power Supplies, theory and design second Edition.
2. Abbrahami. Pressman, " Switching Power Supply Design.
3. Soft Ferrites, " Data Hand Book by Philips.
4. Nasser H. Kutkut, Member,IEEE, Deepak M. Divan, Sendor Member , IEEE, Donald W. Novotny, Fellow, IEEE, and Raymond H. Marion. , " IEEE transactions on power electrinics, vol. 13 no.1, January 1998. , " Design Considerations andd Topology selection for a 120 kW IGBT converter for EV Fast Charging.
5. Richard Redl ELFI S.A. Derrey –la- Cabuche CH-1756 Onnens FR, Switzerland.
   Laszlo Balogh Ascom Energy Systems Murtenstrasse 133 CH-3000 Berne 5, Switzerland. David W. Edwards pacific electro dynamics Redmond, Washington, U.S.A (formerly with asom energy system) , " Optmum ZVS full bridge control: Analysis, Design considerations, and experimental results.
6. Eun-Soo Kim, Kee-Yeon Joe, Moon-Ho Kye, Yoon-Ho Kim, Member, IEEE, and Byung-Do Yoon, " IEEE transactions power electronics, vol. 14 No 2, March 1999, " An improved soft switching PWM FB DC/DC converter for reducing converter for reducing conduction losses.
7. Robert C. Steigerwold GE Corporate R&D Schenectady, NY 12031 (518) 387-05076, " A review of soft –switching techniques in high performance DC power supplies.
8. Fatemah-Soheila Hamdad and Ashoka K.S Bhat, Fellow, IEEE, " IEEE transactions on industrial electronics, vol.48 No 1 February 2001, " Anobel pulsewidth control for fixed-frequency zero-voltage switching DC-to-DC PWM bridge converter.
9. Robert L. Steigerwald, Senior Member ,IEEE, " IEEE transactions on power electronics, vol.3 No.2 April 1988, " A comparison of full bridge resonant converter topology.
10. Richard Redl Senior Member, IEEE, Nathan O. Sokal, Fellow,IEEE and Laszlo Balogh , " IEEE transactions on power electronics. Vol.6 No.3, July 1993, " A novel soft-switching full bridge DC/DC converter: Analysis, design considerations, and experimental results at 1.5 kW ,100kHz.

11. Maria D. Bellar, student Member, IEEE, Tzong-Shianm Wu,member IEEE, Aristide Tchandjou, student member, IEEE, and M. Ehsami fellow, IEEE , " IEEE transactions on industry applications, vol.34 No.4 July/August 1998, " A review of soft-switching DC-AC converter.
12. R.A Fisher, K.D.T Ngo, and M.H, Kuo," in Proc high frequency power conversion conf. May 1988, pp 100-110,"A 500 kHz W dc-dc converter with multiple out puts controlled by phase-shifted PWM and magnetic amplifier.
13. M.W Walters and W.M Polivka ," Proc, APEC 1989,pp. 403-412 (IEEE catalog No. 89CH 2719-3),"A high-density modular power processor for distributed military power system.
14. L.H Mweene,CA wright and M.S Schlechht," Proc APEC 1989,pp, 423-432, (IEEE catalog No. 89 CH 2719-3)," A 1 kW, 500 kHz front end converter for a distributed power supply system.
15. R.Redl and N.O Sokal ," in PESC 1987. Cof.Rec., pp 107-118, (IEEE catalog No. 87CH 2459-6),"Overload-protection methods for switching mode dc/dc converters: classification, analysis, and improvements.
16. O.D Patterson and D.M Divan," Pseudo-resonant full bridge dc/dc converter," in PESC 1987 conf. Rec pp 424-430, (IEEE catalog No. 87CH 2459-6).
17. R.Redl, M, Domb, and N.O Sokal ," How to predict and limit volt-second unbalance in voltage fed push-pull power conversion. Conf. (PCI), Orlando, FL,Apr, 1983,pp 314-330.
18. G.W Ludwig G.A. Franz," in Proc APEC 1989, pp 433 – 438, (IEEE catalog No 89CH2719-3),"Control study of a 500 kHz, 250 W dc-dc converter.
19. R.Redl and N.O Sokal ," in Proc APEC, 87,pp 257-265, (IEEE catalog No 87 CH 2402-6),"How to use current mode control with capacitively coupled full bridge converter.
20. D.B Dalal ," in Proc APEC 1990, pp-265-274, (IEEE catalog No. CH 2853-0)," A 500 kHz multi output converter with zero voltage switching.
21. J.A sabot, V Vlatkovic, R.B, Ridley, F.C. Lee, and B.H Cho," in Proc APEC , 90, pp 275-284, (IEEE catalog No. CH 2853-0).
22. Design considerations for high voltage high-power full bridge zero-voltage-switching PWM converter, R.L Steigerwald and K.D.T Ngo," Full bridge losses switching converter," U.S patent 4 864 429 , Sept 5 1989.
23. Johan Bird Second Edition," Electrical circuit theory and technology.
24. Muhammad H Rashid," Prentic Hall international Editions," Power electronics circuits, Devices , and applications second editions.

25. Robert M. Del Vecchio, Bertrand Poulin, Pierre T Feghali, Dilipkumar M. Shah and Rajendra Ahuja," Transformer Design Principles with applications to core-form power transformers.
26. Kenneth L. Gebert Kenneth R. Edwards," Transformers.