DE-40(DEE)

NUST COLLEGE OF

ELECTRICAL AND MECHANICAL ENGINEERING

RF MICROWAVE SPDT SWITCH

A PROJECT REPORT

DE-40 (DEE)

Submitted by

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PROJECT SUPERVISOR

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NUST COLLEGE OF ELECTRICAL AND MECHANICAL ENGINEERING

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YEAR 2022

DEDICATION

This project is dedicated to our parents, their efforts and all the prayers were with us during the project. It is also dedicated to our teachers and all the technical staff who really helped us for the completion of this project.

DECLARATION

We hereby declare that no portion of the work referred to in this Project Thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning. If any act of plagiarism found, we are fully responsible for every disciplinary action taken against us depending upon the seriousness of the proven offence, even the cancellation of our degree.

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ACKNOWLEDGEMENTS

It is a great pleasure of writing this report. We also acknowledge efforts of many people whose names may not be appear on the title page, but their hard work, friendship, cooperation, and understanding were with us to the production of this report.

Here we would like to mention the support and guidance given by our supervisor Dr Mojeeb bin Ihsan. His availability and prompt responses to our issues aided us in successfully finishing this job. Our department (Department of Electrical Engineering) is responsible for enabling us to complete this project and produce outcomes.

CERTIFICATE OF APPROVAL

It is to certify that the project "**RF/Microwave Switch**" was done by **GC M Hassan Ali, GC Hasnain Muaviah** under the supervision of **Dr. Mojeeb bin Ihsan.**

This project is submitted to **Department of Electrical Engineering**, College of Electrical and Mechanical Engineering (Peshawar Road Rawalpindi), National University of Sciences and Technology, Pakistan in partial fulfilment of requirements for the degree of Bachelors of Engineering in Electrical engineering.

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Dr. Mojeeb bin Ihsan

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ABSTRACT

This project report presents design simulation, fabrication and testing of Single Pole Double Throw (SPDT) microwave switch. SPDT is frequently used in RF and microwave applications like radar, telecommunication, satellites and test and measurement equipment. The microwave switch was designed for an operating frequency of 10 GHz, insertion loss of ≤ 2.5dB, and isolation of ≥ 18dB. A silicon beam lead PIN diode DSG 9500-000 was selected as the solid-state switching device due to its low series resistance and bandwidth up to 18Ghz. The simulations were performed on Keysight ADS. As nonlinear model of this device was not available, therefore packaged PIN diode model was used. Values of series resistance R_s and parallel capacitance C_j from datasheet were substituted in packaged PIN diode model for simulation in ON and OFF state. During design process, a draft layout was made with 50-Ohm transmission lines between all the lumped components. The draft layout was simplified to two parallel loads fed by transmission lines from input port. The impedance of parallel loads will change as diodes turn on or off. Single stub tuning was done to match the on-state impedance to 50 Ohm transmission line. Feed line to single stub was used to maximize off-state impedance. Finally, return loss of input port was minimized to allow maximum power to enter the device. The design was implemented on Rogers RO4350 substrate due to its low loss tangent (δ=0.0037) and excellent temperature performance. Through hole platting was done to provide dc ground to cathode of both diodes and to make a short circuited stub. The dielectric constant (ε_r=3.6) makes it possible to achieve reasonable dimensions of the circuit. The final circuit dimensions are 6 cm x 4 cm. The circuit was fabricated using LPKF laser PCB prototyping machine. The PCB was mounted on an aluminum plate with the help of screws. The aluminum plate also provided a means to hold SMA connectors. The device has three ports. One port is specified as input and other two ports as output ports. Both output ports are interchangeable. The fabricated circuit was measured using Network Analyzer PNA E8363B (Agilent Technologies). The measured results of the SPDT switch exhibit an insertion loss of -3.8dB and an isolation of -18.6dB between input and output ports.

Contents

CHAPTER 01: INTRODUCTION

By definition, RF switch or microwave switch is a device that routes RF frequency signals through transmission paths. RF (radio frequency) and microwave switches are used significantly in microwave test systems for signal routing between instruments and devices under test (DUT). RF microwave switch also provides different configurations to the same circuit.

Concept of RF switch is same as it is for a low frequency switch. The purpose is to stop or let a signal pass through by changing a switching voltage at a third terminal. At low frequency, lumped inductors and capacitors are used to separate switching dc voltage from ac signal. This approach fails at high frequency.

After few MHz frequencies, it is domain of RF where transmission paths dimensions start to affect performance. Time delay becomes significant, load impedance starts to transform, and lumped components give changed behavior. Even low frequency switching elements fail. The greater is the frequency, more drastic its impact is. That are the challenges that are to be tackled using the theory of microwave engineering.

RF microwave switch splits in two main categories, Electromechanical switches and Solid state switches.

1.1 Electromechanical Switches:

Electromechanical switches have metal contact which are opened or closed physically. When path is closed it means that all paths are terminated with 50Ω load. Switching functions were performed by mechanical means, but with the advent of microwave semiconductors devices, the use of mechanical switches has died down.

1.2 Solid State switches:

In 1960s, the term ‘solid state’ defines electronic devices which are neither mechanically controlled nor vacuum tube. In these switches electron flow through semiconductor material. These switches have good insertion loss as compared to electromechanical switches. Solid State switches are further divided into two types.

1.2.1 Field-Effect Transistor (FET)

Field Effect Transistor whether they are Silicon junction devices or GaAs MOSFETs, are being used as switching devices. The ratio between ON and OFF resistance of channel is quite high. Figure of merit of switch is typically defined as hypothetical cutoff frequency.

$$w_c = \frac{1}{R_{on}\, C_{off}}$$

R_{on} is the total resistance at ON state, and C_{off} is total drain-to-source capacitance at OFF state.

1.2.2 PIN DIODE

PIN diodes are popularly used in solid state switching due to their high power, high frequency and relatively low insertion loss. PIN diode is silicon semi-conductor diode in which intrinsic I region is sandwiched between positively doped region and negatively doped region. The I-layer separates the highly doped p-type layer and n-type layer. The I-layer is lightly doped and becomes conductive in forward biased condition. In reversed biased condition, depletion layer width increases therefore reducing the diode capacitance. The use of PIN diodes as the switching component in microwave circuits is based on the difference between the PIN diode reverse and forward bias characteristics.

1.3 FUNDAMENTAL PARAMETERS OF A SWITCH

1.3.1 ISOLATION:

By definition, isolation is ratio of power delivered to the load for an ideal switch in the ON state to the actual power delivered to load when it is in OFF state. It is determined by estimating the difference between the power measured at the switch output port with the switch biased ON and the power measured at the switch output port with the switch biased OFF.

Isolation (dB) = P_{out}on (dBm) - P_{out} off (dBm)

$$\textbf{Isolation (dB) = 10 log [1 + }\frac{1}{(4\pi f CjZ\text{load})^2}\textbf{]}$$

1.3.2 INSERTION-LOSS:

Insertion Loss is defined as the ratio of power delivered to the load in the ON state of the ideal switch to the actual power delivered by the practical switch. It is usually expressed in decibels. The insertion loss of a switch can be approximated as: [1]

$$\textbf{IL(dB) =20 log (1+}\frac{R_s}{2Z_{load}}\textbf{)}$$

1.4 SINGLE POLE SINGLE THROW SWITCHES

Single pole Single throw switches require one switching device. It means that it has one input terminal and one output terminal. It works as on-off state switch. Our switching device is PIN diode due to its fast switching time and also low on state impedance. We will discuss the two basic configuration of SPST switch that is series mounted switching device and shunt mounted switching device.

1.4.1 SERIES SPST SWITCH

In series SPST switch configuration, the input signal is routed to output signal when switching device (PIN diode) is in ON state. In this configuration, diode is placed in route of RF path. When diode is in ON state, the RF signal will pass through the transmission line. But, when the diode is in OFF state, the diode impedance will stop RF signal through transmission line. The Figure 1.1 shows series configuration of SPST switch. [2]

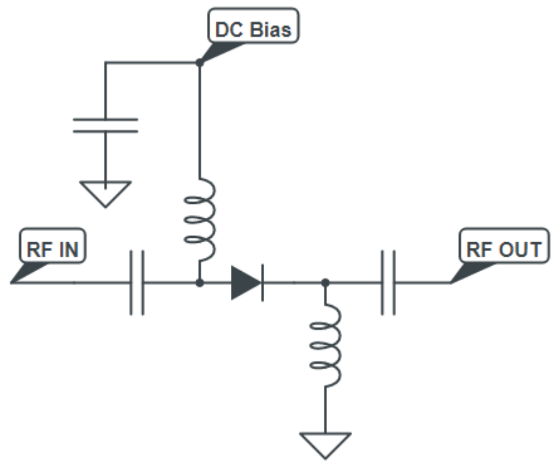


Figure1.1 Series SPST switch [2]

The isolation, insertion loss and power dissipation formula of series single pole single throw switch are mention below: [1][3]

$$IL = 20 \log \{1 + \frac{R_S}{2Z}\}$$

$$ISO = 10 \log \{1 + \frac{1}{4\,\pi f\ Ct\ Zo}\}$$

$$\text{Power Dissipation } (P_d) = \frac{4\ Rs\ Zo}{2Zo + Rs}\ 2\ P_{avg}\ \text{Watts}$$

1.4.2 SHUNT SPST SWITCH

In shunt SPST configuration, the PIN diode of selected ON port is reversed biased while OFF ports are forward biased to create short circuit of transmission line. The Figure 1.2 shows the shunt configuration of SPST switch circuit. [2]

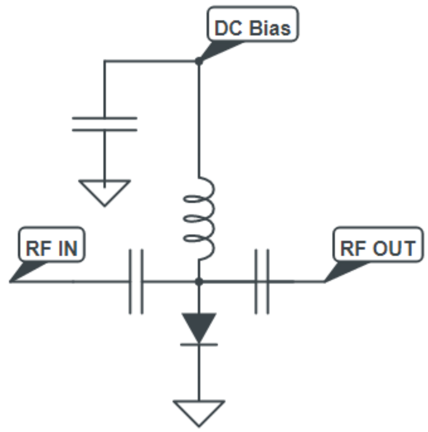


Figure1.2 Shunt SPST Switches [2]

The isolation, insertion loss and power dissipation formula of shunt single pole single throw switch are mention below [1]:

$$IL=10\log \{1+(pf\ C_t\ Z_o)2\}\ dB$$

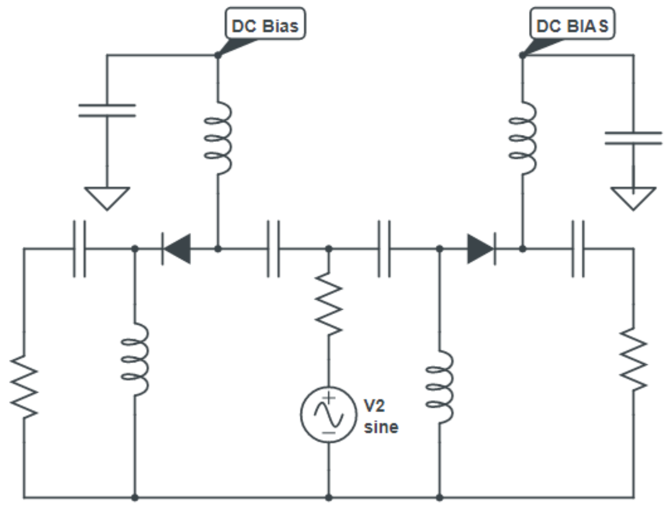
$$ISO=20\log \{1+\frac{Zo}{2\ Rs}\}\ dB$$

$$\text{Power Dissipation, Pd} = \frac{4\ Rs\ Zo}{(Zo + 2\ Rs)2}\ P_{avg}\ \text{Watts}$$

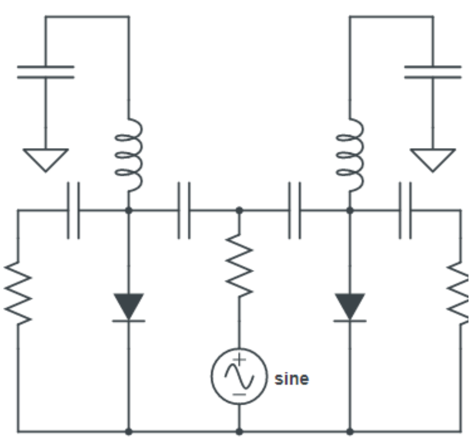
$$Pd = \{\frac{Zo}{Rp}\}\ P_{avg}\ \text{Watts}$$

1.5 SINGLE POLE DOUBLE THROW SWITCHES

Single pole double throw (SPDT) requires a minimum of two switching devices. It is designed as employing switching device in each arm adjacent to common point. At a time, one switching device will be in ON state while the other switching device will be in OFF state. Two basic configuration of SPDT switch is series mounted and shunt mounted devices. In series configuration, the input signal is routed to output when one diode 1 is in ON state and other diode 2 is in OFF state. In either configuration, at any time one diode is ON state while the other is in OFF state. The Figure 1.3(a) shows series SPDT circuit design and Figure 1.3(b) shows shunt SPDT circuit design.



(a) Series SPDT Switch



(b) Shunt SPDT Switch

Figure1.3 Series and Shunt SPDT switch configuration (a) Series SPDT Switch (b) Shunt SPDT Switch

For different type of switch configuration, the formula of isolation and Insertion Loss varies. Table 1.1 shows comparison of series, shunt and series-shunt switch configuration.

Table 1.1 Summary of Formulas for SPST Switches [1][4]

TYPE	ISOLATION(dB)	INSERTION LOSS (dB)
SERIES	$10\log[1+\frac{1}{(4\pi fCrZo)^2}]$	$20\log[1+\frac{Rs}{2Zo}]$
SHUNT	$20\log[1+\frac{Zo}{2Rs}]$	10log [1+$(\pi fCrZo)^2$]
SERIES-SHUNT	$10\log\left[\left(1+\frac{Zo}{2Rs}\right)^2\right]+\frac{1}{4\pi fC_TZ_0}[1+\frac{Z_0}{R_S}]^2$	$10\log[\left(1+\frac{Rs}{Zo}\right)+(\pi fC_T)^2(Zo+Rs)^2]$

CHAPTER 02: DESIGN CONSIDERATION

Our aim is to design SPDT switch using PIN diode as switching device. As we have to design SPDT switch, there are certain requirements to achieve our goal. It includes circuit topology of SPDT, substrate selection and PIN diode selection which is most significant part of design. As in SPDT switch two switching devices are used, selection of devices and substrate has huge effect on performance of switch.

2.1 Circuit Topology

The Figure 2.1 shows series SPDT switch configuration. In this configuration, circuit is designed as employing PIN diode each arm of adjacent to common point. In order to work as SPDT switch, one diode will be in ON state while the other will be in OFF state.

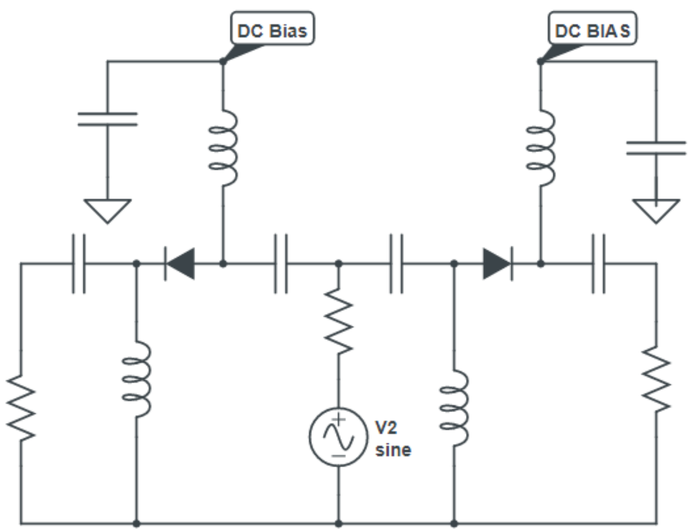


Figure2.1 Series SPDT switch configuration [5]

2.2 Design Specification

The design specification of our series SPDT switch are listed in Table 2.1. The frequency at which we are operating is 10GHz. Our goal is to achieve Insertion Loss < 2 dB and Isolation > 18dB.

Table 2.1 Design Specification

Operating Frequency	10GHZ
Insertion Loss	<2.5dB
Isolation	>18dB
Switching Time	40ns

2.3 Device Selection

Selection of right PIN diode is pivotal in design. A designer must be aware of the requirements and should be willing to make acceptable compromises. Important factors to be considered while selecting a device is switching characteristics, insertion loss of diode, isolation of diode, best results on operating frequency, power dissipation, storage temperature and operating temperature. Our switching device in this design is beam lead diode because it has fast switching device, low resistance and capacitance.

2.4 Substrate Selection

Similar to device selection, substrate selection is also important. Apart from the availability and cost issues the designer need to consider the several electrical and mechanical properties of substrate. Dielectric loss is another factor to consider and is the measure of inherent dissipation of electromagnetic energy usually in form of heat. It is usually given in data sheet as the loss tangent. For our design, the substrate chosen is Rogers RO4350B [6].

2.5 Selected Device

Based on design requirements and availability in the lab, the PIN diode we selected is DSG 9500-000 Beam Lead diode [3]. The detail of beam lead diode is shown in Table 2.2

Table 2.2 Design Requirements

Device Name	**DSG 9500-000**
Manufacturer	Skyworks Inc.
Type	Beam Lead Pin Diode
Breakdown Voltage	200V
Capacitance@1MHz	0.02pF
Series Resistance	4 Ohm
RF Switching Time	25ns
Insertion Loss@10GHz	0.6dB
Isolation @10GHz	-25dB

CHAPTER 03: COMPONENTS DESIGN

Figure 3.1 shows series PIN diode SPDT switch which we have already discussed in chapter 2. In order to implement this circuit, there are certain limitations. To overcome that we have to design certain components of circuit. The circuit shown in Figure 3.1 is designed for low frequency and we are working at an operating frequency of 10GHz. Due to unavailability of inductors for such high frequency we will design BIAS TEE network and also choose specific DC blocking capacitors.

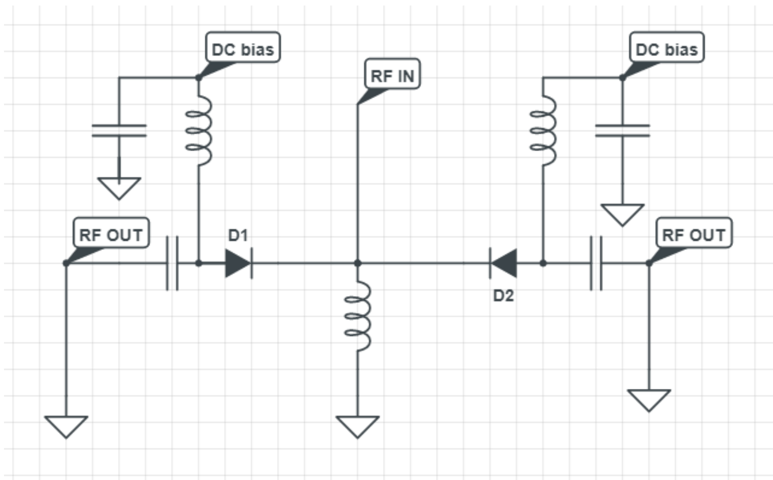


Figure3.1 Series PIN Diode SPDT Switch

3.1 DC Biasing

In circuit shown in Figure 3.1 DC biasing has been done by using inductors. They act as RF Choke. Its function is to stop RF signals from going to DC supply. But as we are operating at frequency of 10GHz we cannot implement inductors at this frequency. Hence we implemented the inductor by designing biased TEE network. Biased TEE will be designed such that it acts as open circuit at operating frequency of 10GHz. The biased TEE network comprises of Radial stub and quarter wavelength. The Radial stub should act as short circuit, and then quarter wavelength away, it will act as an open circuit. Hence RF signal should not pass through it. Initially we will design the radial stub then add quarter wavelength.

3.1.1 Radial Stub

The schematic diagram of Radial stub is shown in Figure 3.2

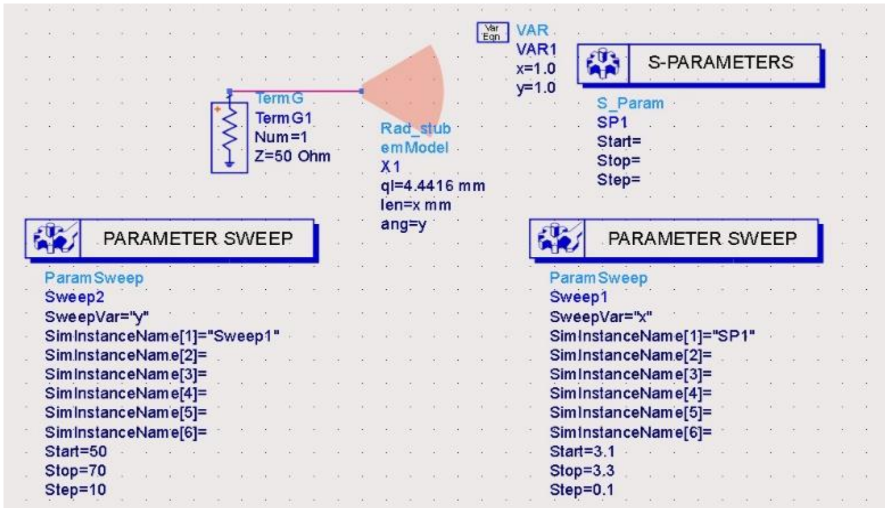


Figure3.2 Schematic diagram of Radial Stub design

Short circuited Radial stub has zero impedence on smith chart. We choose radial stub from ADS component pallet and select two variables of radial stub that is angle ‘q1’ and length ‘len’.We swept both variables over range and obtain certain points as shown in Figure 3.3. The values of length and angle where we achieve almost zero impedence are 3.3mm and 61 degree repectively.

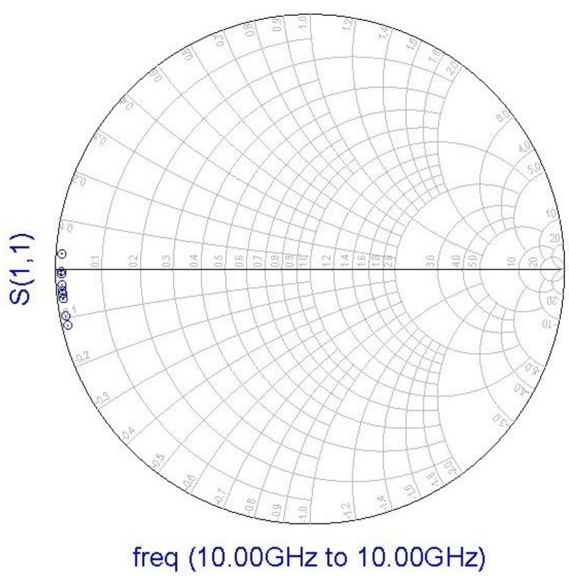


Figure3.3 Smith chart calibration at short circuit radial stub point

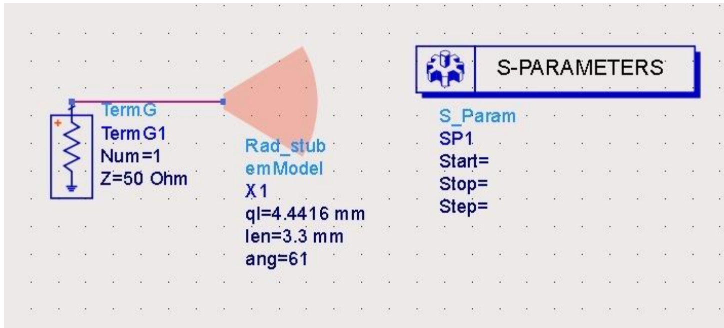


Figure 3.4 Schematic diagram of designed Radial Stub

To make sure that chosen values are correct we put it into radial stub component and simulate. Hence we got point where impedance is zero on Smith chart as shown in Figure 3.5

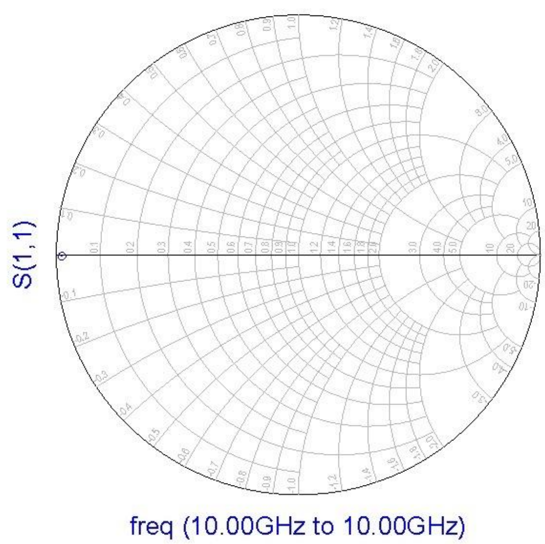


Figure3.5 Simulated Results of Radial stub impedance

3.1.2 Quarter Wavelength

Now we will add quarter wavelength to obtain open circuit path for RF signal. We designed quarter wavelength at operating frequency of 10GHz. Then add it to radial stub therefore short circuit radial stub after connecting to quarter wave it acts as open circuit. The RF signal cannot pass through it due to open circuit path.

The Bias TEE network comprises of Radial Stub and Quarter wavelength. The Figure 3.6 shows the bias TEE schematic diagram.

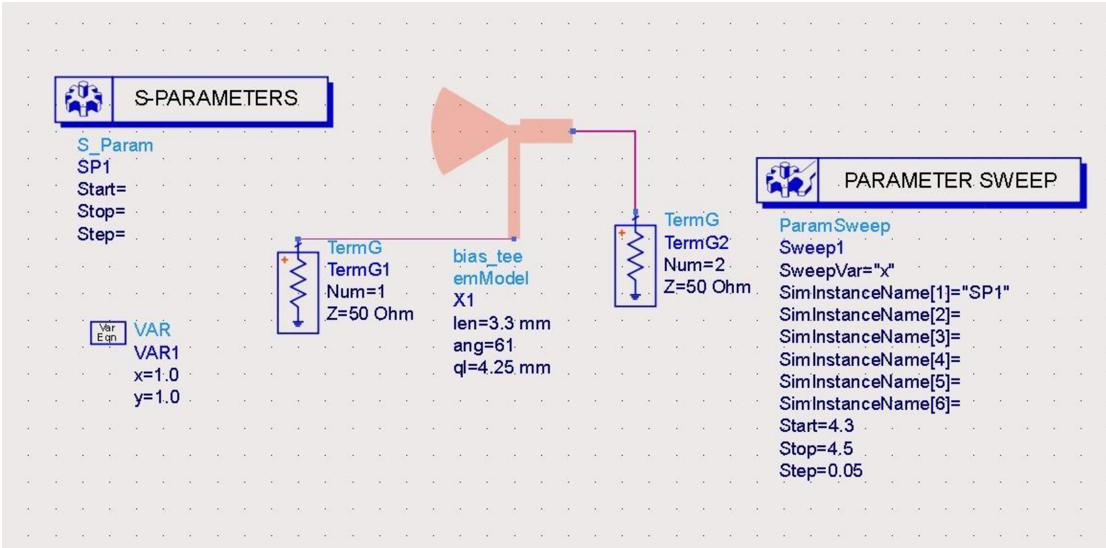


Figure3.6 Biased TEE Network

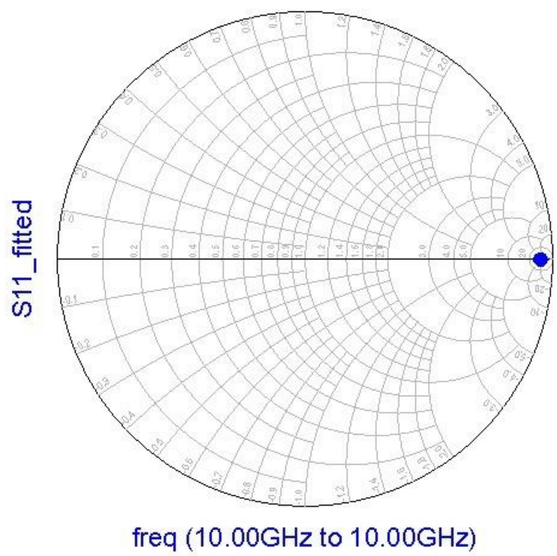


Figure3.7 Smith Chart Impedance of designed Bias TEE

As we discussed that bias TEE network will act as open circuit for RF signal path. In Figure 3.5, it shows that impedance is zero and on left side of smith chart, then we add quarter wavelength the point shifted towards right side as open circuit shown in Figure 3.6. The simulations and results of biased TEE network is shown in Figure 3.7.

3.2 PIN Diode Model

The PIN diode is basically designed in such a way that Intrinsic region I is sandwiched between p-type material and n-type material as shown in Figure 3.8. The width of intrinsic region is larger than p type /n-type layers. PIN diodes can be explained using the following parameters [1]:

- Rs series resistance under forward bias
- C_T or C_j total capacitance at zero or reverse bias
- R_p parallel resistance at zero or reverse bias
- VR maximum allowable voltage
- DC reverse bias voltage
- τ carrier lifetime

The PIN diode we used in our SPDT switch design is DSG 9500-000[7]. The spice model for our diode is not available in ADS Software and on the manufacture's website. So, we used generic model of a PIN diode available in ADS. The parameters of PIN diode model are chosen from datasheet. PIN diode is a nonlinear device and it behaves differently in forward and reverse bias. The working of diode in on/off state will be discussed in next section.

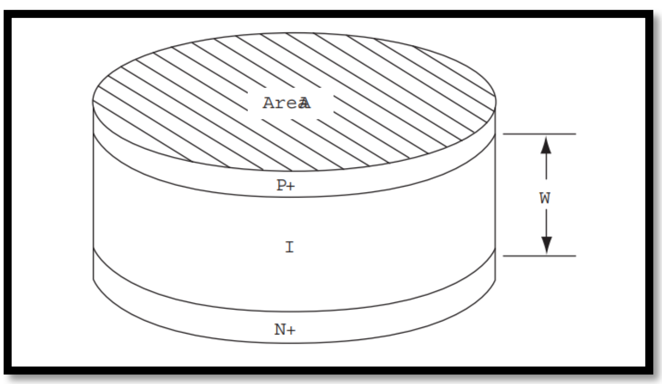


Figure3.8 PIN diode model [1]

3.2.1 Forward Biased Model

When the PIN diode is forward biased, I region has been injected by holes and electrons. These charges do not immediately obliterate each other; instead, they remain for some time, called the carrier lifetime, t. For forward biased state, the model we used is shown in Figure 3.9. The forward resistance Rs decreases as current start flowing through diode, it acts like a variable resistance in forward biased condition. The junction capacitance reactance is minimum in this mode. The on-state model can be simplified by combining R_j, which is a very small quantity during forward-bias conditions, with Rs (contact resistance) to form a new value for Rs. [1]

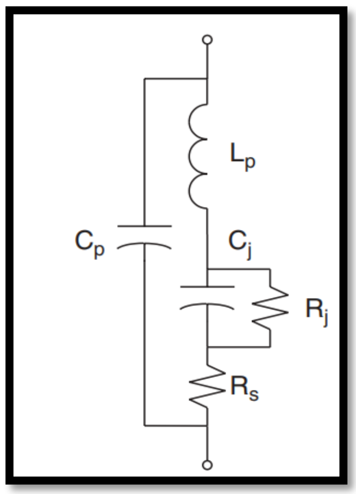


Figure3.9 Forward Biased Model [1]

3.2.2 Reverse Biased Model

In reverse biased condition, there is no stored charged in I region and diode appears as capacitor C with resistance in parallel with it. Typically, the junction resistance R_j can be ignored during reverse-bias conditions, since Rj $> \frac{1}{wCj}$, thus dominating the reverse isolation characteristic of the diode. [1]

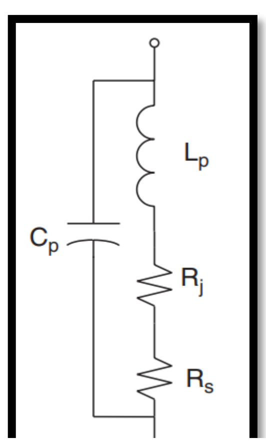


Figure3.10 Reverse Biased Model [1]

We selected the generic model of PIN diode from ADS components palette and substituted the typical values of parameters in it. The effective parameters are series resistance, Rs in forward biased and parallel capacitance, C_j in reverse biased. These two values are taken from DSG 9500-000 datasheet. The values of other parameters are choosing as typical values of Beam Lead PIN diode model. Those typical values are given in Figure 3.11.

Model Parameters for Forward- and Reverse-Bias Conditions

	On State	Off State
R_s or R_j	1.47 Ω	45 kΩ
C_j		0.21 pf
C_p	0.05 pf	0.05 pf
L_p	1.23 nH.	1.23 nH.

Figure3.11 Model Parameters for Forward and Reverse Bias Conditions [1]

The values chosen from datasheet are series resistance, R_s in forward biased and junction capacitance Cj in reverse biased. These values are shown in Figure 3.12.

Low Capacitance Planar Beam Lead Diode

Part Number	Breakdown Voltage @ 10 µA (V)	Capacitance Total @ 50 V, 1 MHz (pF)	Series Resistance (From Ins. Loss @ 3 GHz, 50 mA)(1) (Ω)	Minority Carrier Lifetime I_F = 10 mA, I_R = 6 mA (ns)	RF Switching Time T_S (ns)(2)	Outline Drawing Number
	Min.	Max.	Max.	Typ.		
DSG9500–000	200	0.02	4.0	250	25	169-001

Figure3.12 Datasheet Parameters of Planer Beam Lead Diode [7]

3.3 Capacitors Selection

In Figure 3.1, the design of SPDT, there are certain capacitors used in circuit. These capacitors are chosen for desired frequency of 10GHz.There are two categories of capacitors used in design of circuit that is DC blocking Capacitor and DC supply noise filter capacitor. The values of DC blocking capacitor is very low in order to decrease its impedance to let AC signal pass through it.

CHAPTER 04: DESIGN AND SIMULATION

The microstrip line is the main member of a broad class of transmission lines that are built using printed circuit board technology. Transmission line is made by making required pattern on one side of a low dielectric loss substrate material. We shall refer to this pattern as layout as named in ADS. Sweep controllers were used to optimized lengths to required results. Here, we shall first find width of 50-Ohm transmission line, will make the layout by using sweep controllers in ADS and applying microwave theory. Simulation results are also shown and discussed.

4.1 Layout Design:

Once, the bias tee for our desired frequency and selected the lumped components (diode and capacitors) are designed, we can place these components with microstrip lines in between. The placement is done according to lumped components circuit diagram of Figure 3.1. As, we are making a 50-ohm system, the width of lines from where RF signal is going to pass is always kept 1.081mm.

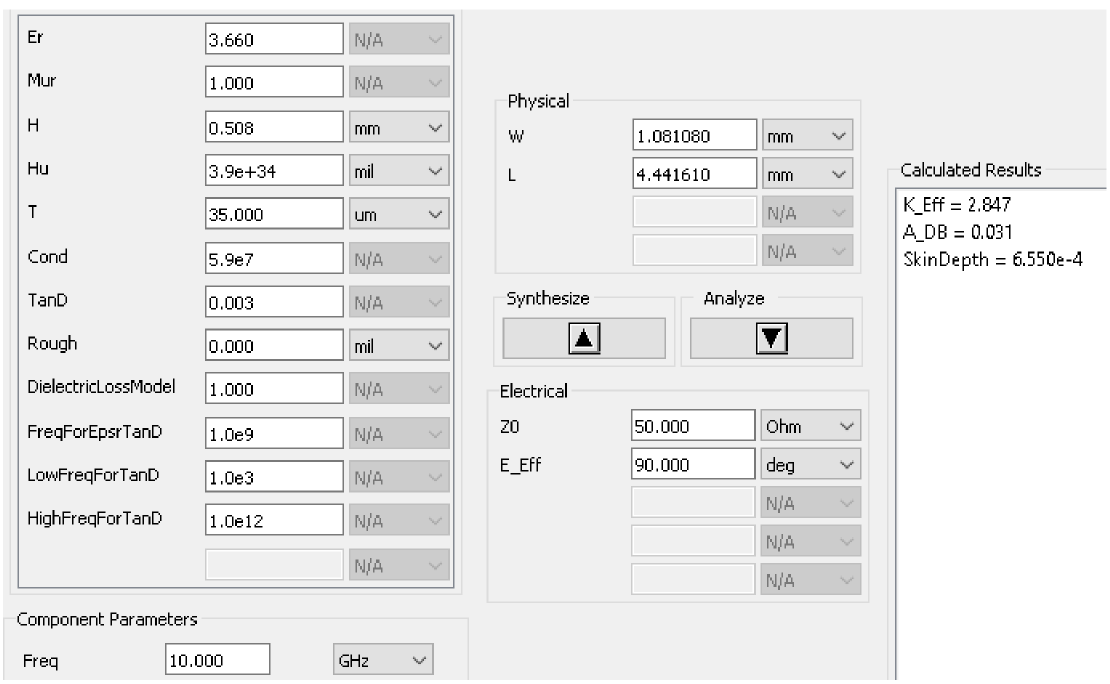


Figure4.1 50-Ohm line dimensions on RO4350B substrate

4.2 Gaps for Components:

The spaces are kept for placing the diodes, resistors and capacitors. Each component has some specific dimensions like total length and length of metal connects attached to it. These are instrumental in leaving gaps for lumped elements.

4.2.1 Diode Spacing:

Figure 4.2 shows detail dimensions, obtained from datasheet of PIN diode DSG 9500-000. It contains a complete structural diagram for the diode. Total length and length of metal connects are the key points. [7]

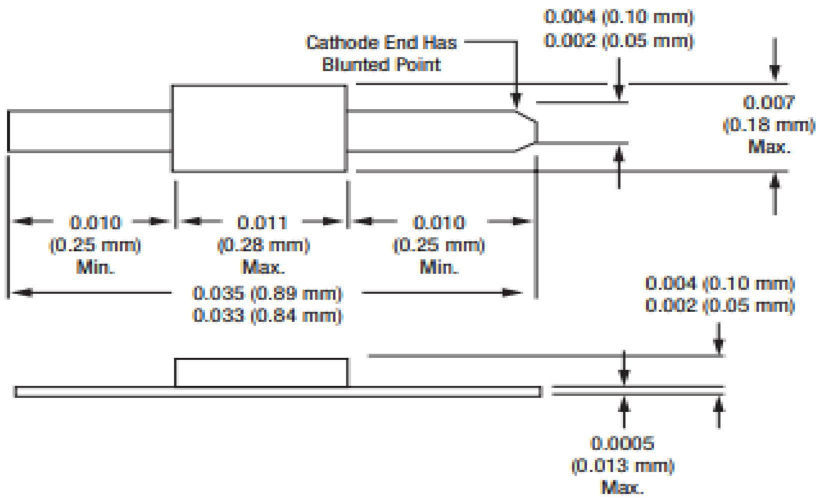


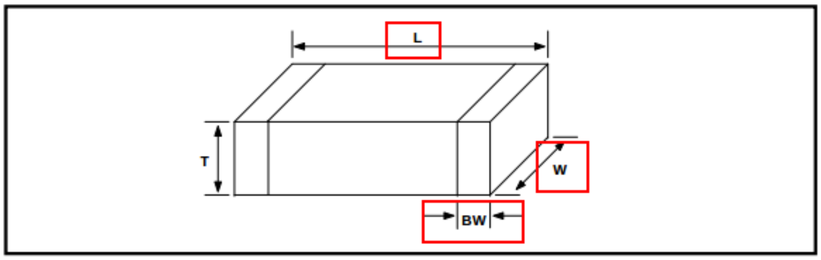
Figure4.2 Dimensions of DSG 9500-000 [7]

There is some tolerance in the dimensions of diodes. We shall choose the maximum length to place diodes. Space to be left for Pin Diodes is 0.3mm.

4.2.2 Capacitor and Resistor Spacing:

We are using 0603 capacitors and resistors in our design. For dimensions of standard 0603 SMD components we referred to datasheet [8].

Figure 4.3 shows the dimensions of 0603 capacitors and resistors.



CODE	EIA CODE	DIMENSION (mm)			
		L	W	T (MAX)	BW
03	0201	0.6 ± 0.03	0.3 ± 0.03	0.33	0.15 ± 0.05
05	0402	1.0 ± 0.05	0.5 ± 0.05	0.55	0.2 +0.15/-0.1
10	0603	1.6 ± 0.1	0.8 ± 0.1	0.9	0.3 ± 0.2

Figure4.3 Dimensions of 0603 Capacitors and Resistance [8]

Space to be left for 0603 components is L-BW. Whole Metallic Pad of SMD should be on the transmission line. That is why maximum value of BW is assumed that is 0.5mm. Thus,

$$\text{Space} = L - BW$$

$$= 1.6 - 2(0.5) = 0.6\text{mm}$$

4.3 Draft Layout:

Figure 4.4 shows draft layout of SPDT switch. The circuit layout is designed using 50-ohm transmission line with appropriate gaps for SMD component and PIN diode. The DC biased network is connected through the radial stub. The arrow pointing into circuit represents input signal named as port 1 while arrows pointing out are the two output ports referred to as port 2 and port 3. Port along with indicating arrows are shown in Figure 4.4.

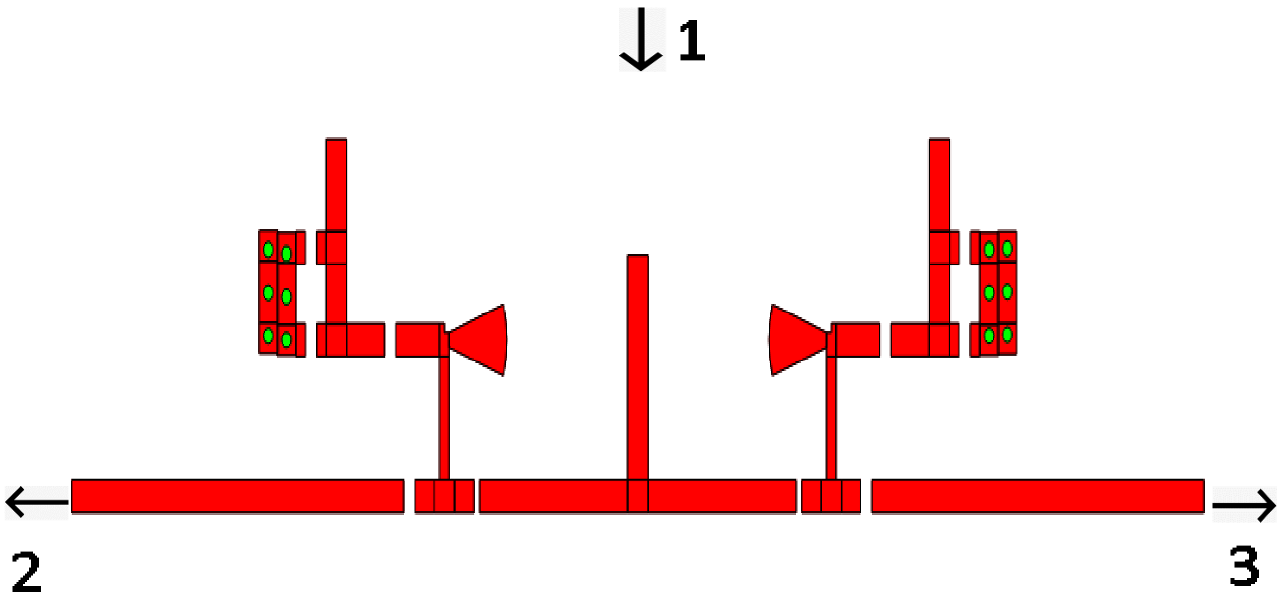


Figure 4.4 SPDT Draft Layout

Although, the length of all the microstrip lines are symmetric on both sides, they are arbitrarily selected. RF performance of a single transmission line is a function of its length. Varying the length, an open transmission line can behave as a short circuit. Thus, we need to select lengths of all the transmission lines to get the desired result from our switch. Some simplifications can be done before moving any further.

4.3.1 Simplified Draft 1:

Although, a perfect bias tee was not achieved (discussed in previous Chapter). Let us assume that it is perfect, and it does not let any part of RF signal through. It is like an open circuit and thus can be removed from the layout. The new layout is shown in Figure 4.5.

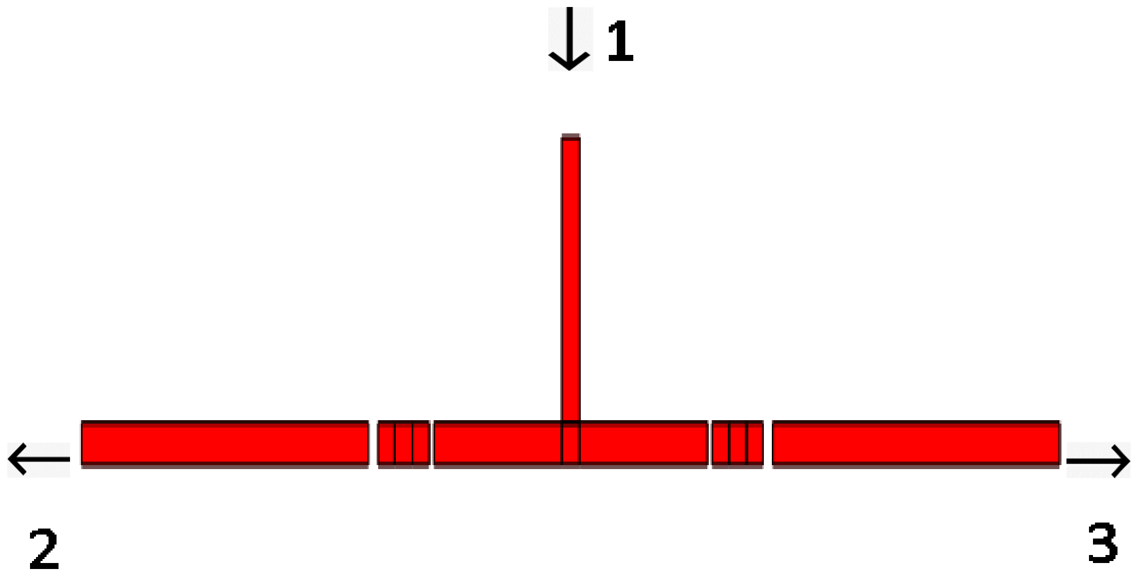


Figure 4.5 Draft SPDT without Bias TEE Network

4.3.2 Simplified Draft 2:

Port 2 and 3 which are output ports of SPDT are shown in Figure 4.5 on which load is expected to be connected. When the load impedance and intrinsic impedance of line are matched, the load impedance does not transform along the transmission line and input impedance remains equal to the load impedance. As a 50-Ohm system is being made, the line is 50-ohm and it expected from the user to terminate output ports into 50-Ohm load. So, the load along with line feeding it can be replaced by an impedance of 50-Ohm.

This 50-Ohm comes in series to 10nF capacitor. New Z_L is:

$$Z_L = 50 - \frac{j}{10\text{nF}} * \pi * 20\text{GHz}$$

$$= 50 - j0.001$$

Which is approximately 50-Ohm.

There is again a matched line for this 50-Ohm. Thus, a 50-Ohm comes in series with pin diode. This part of circuit is replaced with the schematic containing diode and termination as shown in Figure 4.6.

In conclusion, lengths after diode are a random choice to be done by designer. We used these lengths to set the total dimensions of device. New simplified layout is shown in Figure 4.6.

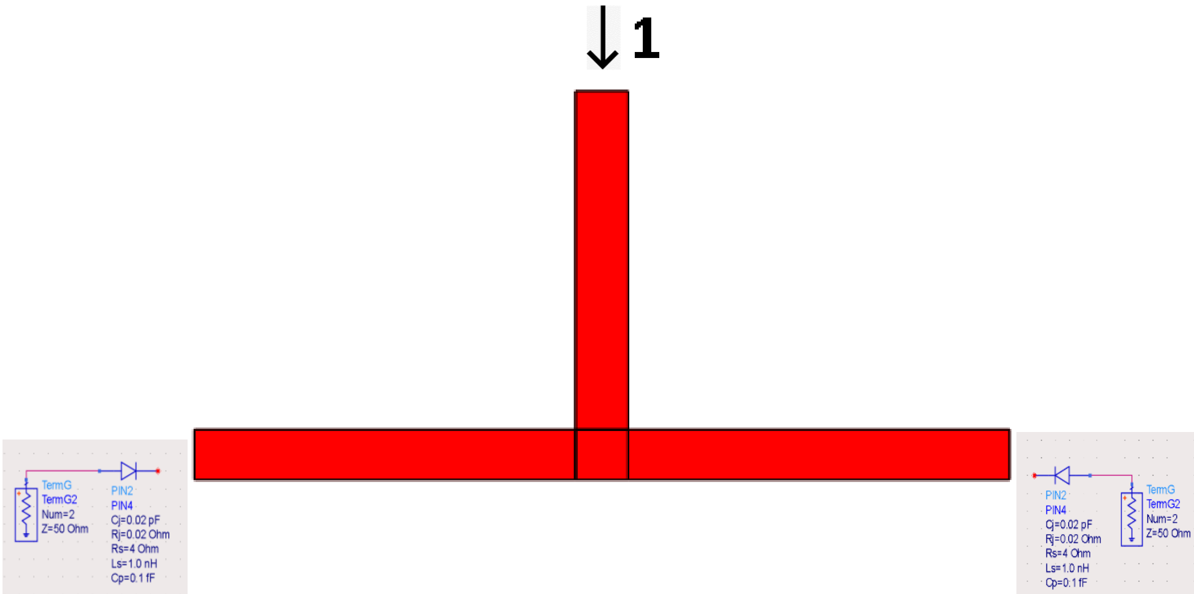


Figure4.6 Simplified Draft SPDT

4.4 Parallel loads:

Referring to Figure 4.6 again both output sides are parallel to each other. Assuming two states of diode, their parallel combination will make three configurations.

Table 4.2 Switch Modes

S No	Diode 1	Diode 2	Mode
1	Off	Off	Isolator
2	On	Off	Switch
3	Off	On	Switch
4	On	On	Divider

Since a switch is desired, let us assume one side is on and one is off.

4.5 Diode On State:

When diode is forward biased, it shows a low impedance to RF signal. The combined input impedance shown by pin diode and load is simulated, with the schematic as shown in Figure 4.7. Simulated results are shown in Figure 4.8.

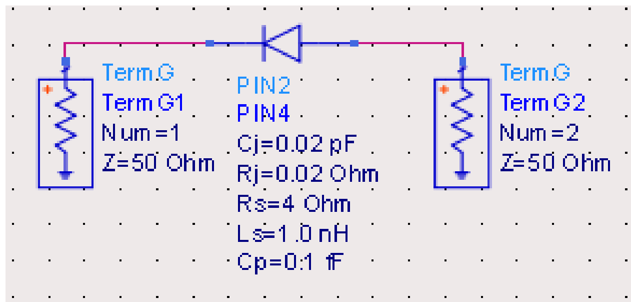


Figure4.7 Schematic for determining the On-State Diode impedance

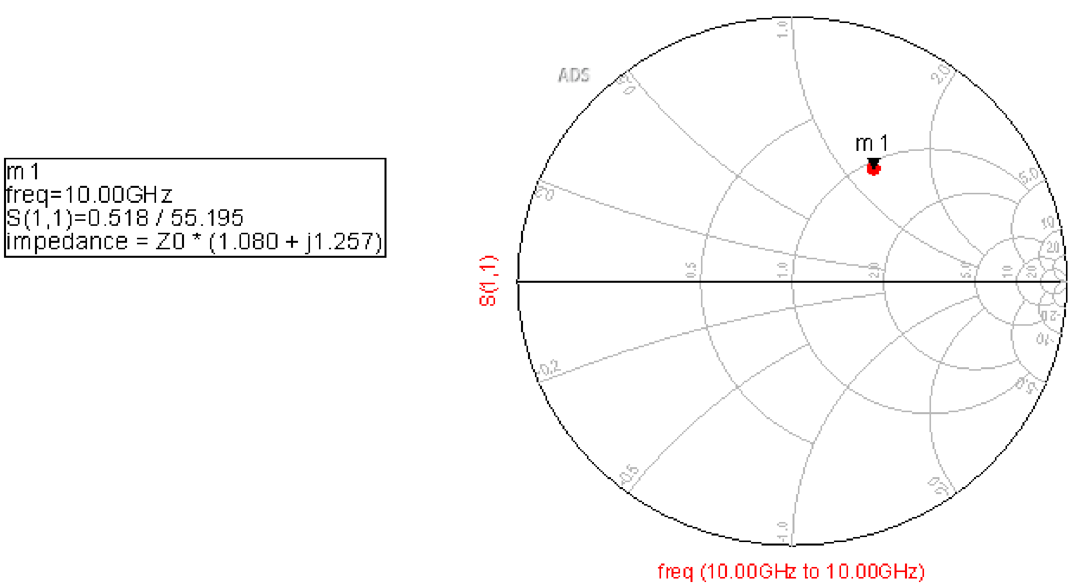


Figure4.8 Impedance of On-State Diode (Z_o=50 Ohm)

Series combination of diode and 50-ohm load is named as Z_{in} and it must be matched to 50-Ohm line. It can be matched by placing a single open stub at some distance from this load-diode combination. The matching can be done by writing a Matlab script, mathematical formulae or using parameter sweep in ADS. A Matlab script was written to make a guess for values of stub length and distance. Setup shown in Figure 4.9 was done in ADS by placing two variables for stub length and stub distance.

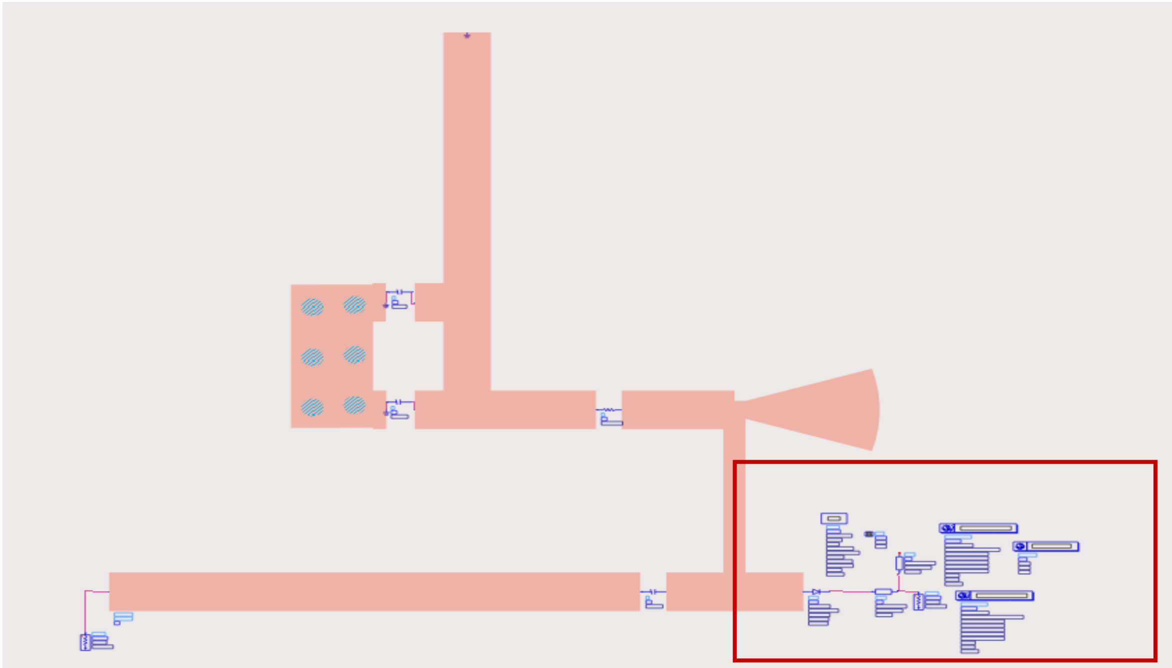


Figure4.9(a) On-State Single Stub Sweep

A zoomed screenshot of rectangular portion in Figure 4.9(a) is shown in Figure 4.9(b):

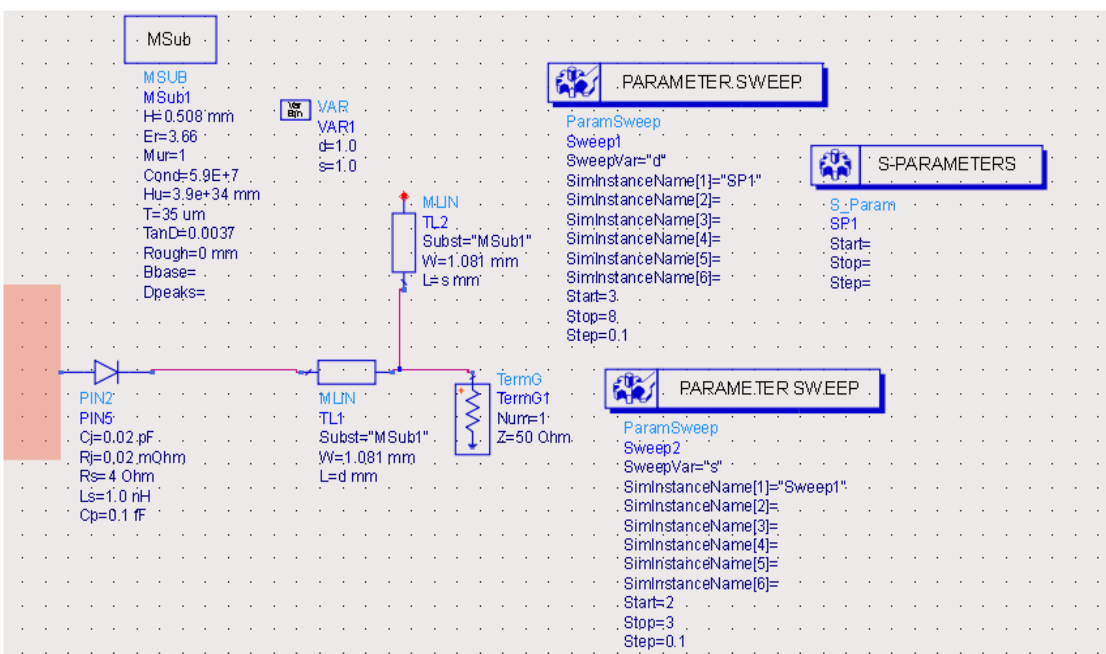


Figure4.9(b) Zoomed screenshot of On-State Diode

After sweeping both variable of stub length and distance, results are shown in Figure 4.10.

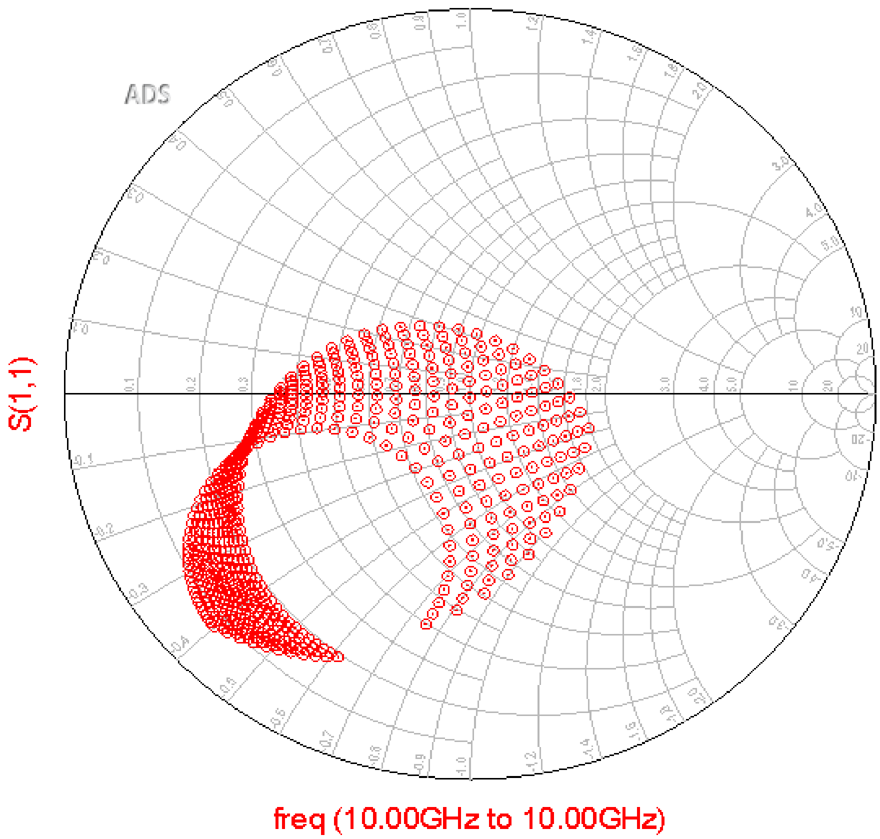


Figure4.10 Simulated Results of Single Stub Sweep to match Z_{in}

From above Figure 4.10, the point closest to normalized impedance of one on smith chart is selected. At this point, value of single stub length is 2.5mm and distance from load is 7.1mm. By adding this single stub, on-state of switch is matched to 50-ohm line.

4.6 On-State Matched Layout:

After placing the designed open stub in series, new layout is shown in Figure 4.11. Once again, simulation was run to confirm that newly placed open stub matches Z_{in} to transmission line.

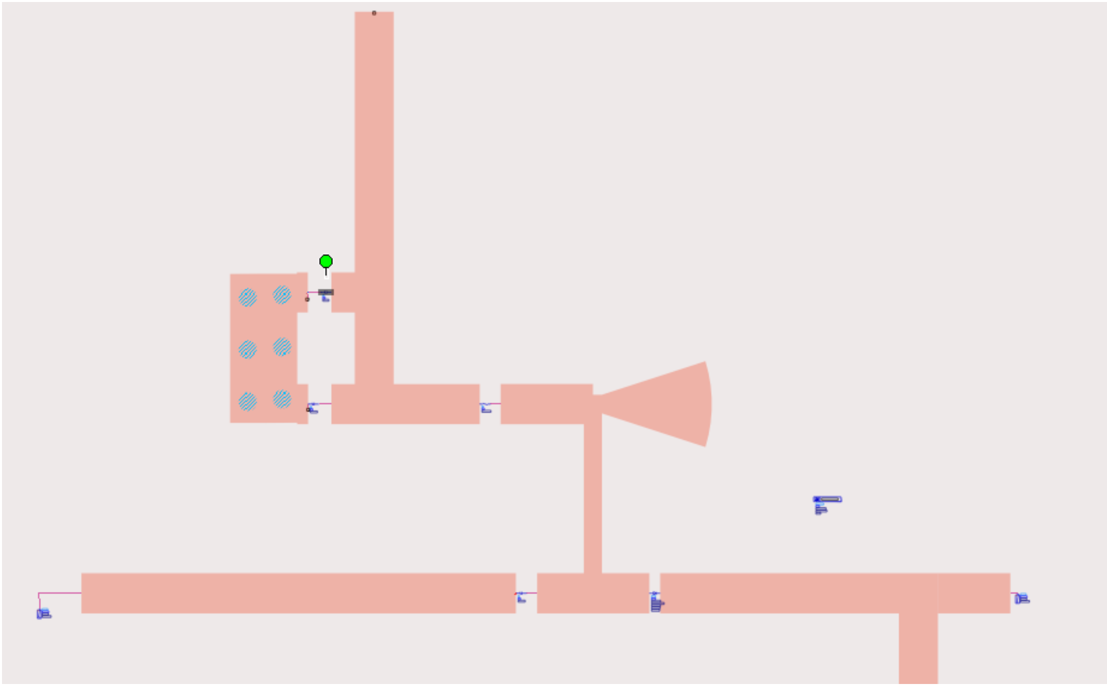


Figure 4.11 On-side after matching

By placing the open stub, good matching is achieved. It is visible in return loss graph of Figure 4.12. At 10GHz, return loss is approximately -15dB.

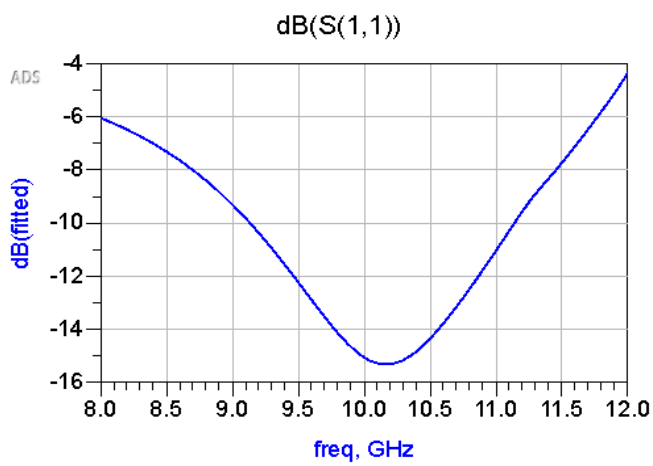


Figure 4.12 Stimulated Return loss of On-side

4.6 Off-State Diode:

For switch application, the other diode must be reverse biased. During reverse bias, diode is mainly a capacitor of 0.02pF. Its impedance to 10GHz signal is:

$$Z = \frac{1}{(20*pi*0.02\ m)}$$

Z = 800 Ohms

In previous section 4.5, on-side impedance has been matched to 50-Ohms by placing an open stub in front of it. This stub matching has changed the off-state impedance of diode to some new value. Off-side must ideally be open or at least should present maximum possible impedance. Figure 4.13 show the impedance of off-state diode simulated in ADS after placing off-state value in PIN diode packaged model.

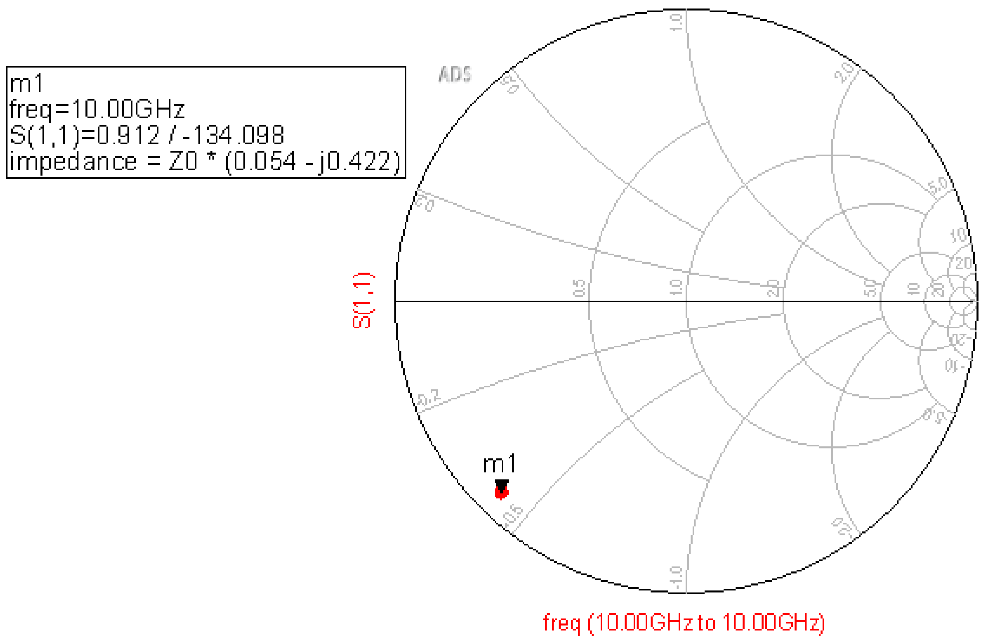


Figure 4.13 Impedance of Off-State Diode

It is evident from Figure 4.13 that reflection coefficient is very good and close to 1. Reactive impedance is not desired since it causes power storage and hence should be minimized. A new open stub cannot be added as it will transform impedance of on-state which has just been matched.

The issue can be solved by controlling the length of line feeding to diodes. This length does not change the on-state impedance because it is already matched. Whereas a length can be selected to transform off-state impedance to a purely resistive one. This real impedance will also be highest possible value of impedance. Thus, both objective of high and real impedance can be achieved.

Schematic shown in Figure 4.14 was made in ADS.

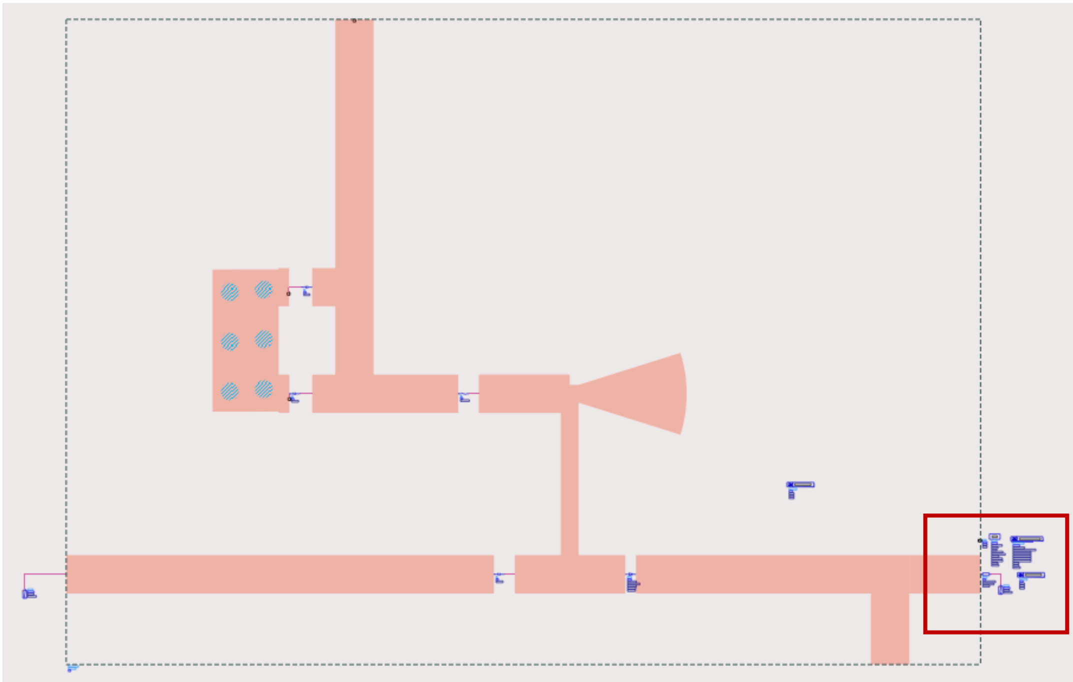


Figure4.14 Off-side impedance maximization

A zoomed portion of right side of Figure 4.14 is shown in Figure 4.15. A transmission line was placed before the off-state diode. Varying length of this line will change off-state impedance Z_{in}. Whereas on-state impedance will not change as it is already matched. A length that maximizes the off-state impedance and minimizes reactance will be chosen.

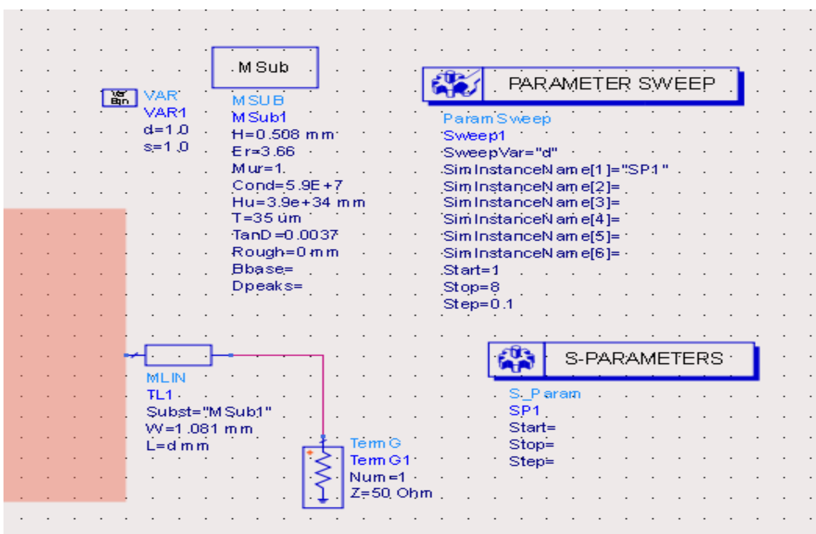


Figure4.15 Zoomed portion ofFigure4.14

The length that connects the single stub to central feed line was swept in ADS over a range equal to half quarter wavelength. Length that produces maximum impedance and lowest reactance is chosen from the resulting smith chart shown in Figure 4.16.

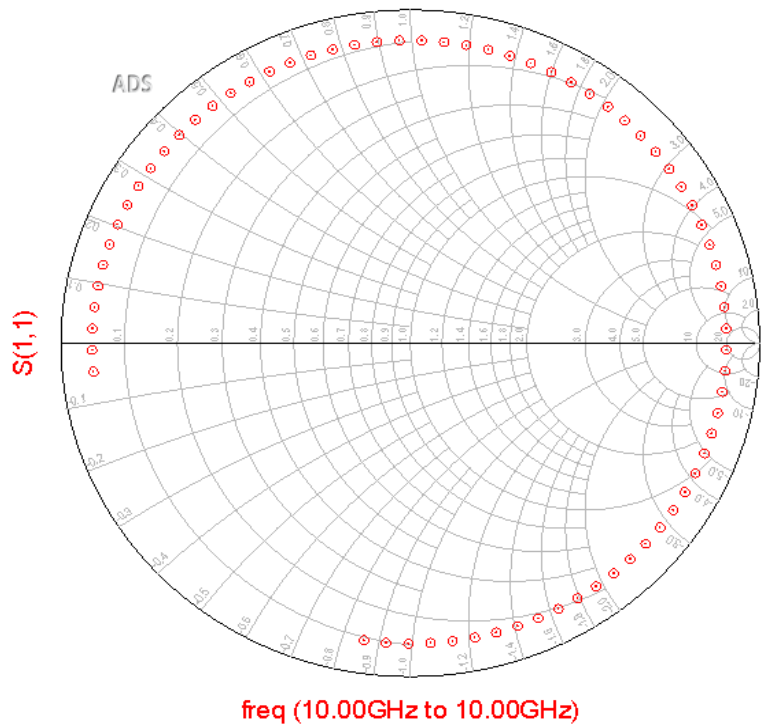


Figure4.16 Simulated results of Off-side impedance maximization

Maximum impedance occurs at d=5.1mm. Off-State impedance at this point is approximately 1kOhm.

4.7 Parallel Combination:

Thus, on and off states of diode will present an impedance of 50 Ohms and 1kOhms. If both sides are in same state, power will get divided. In case of switching, most of power will be directed to matched side (on-side).

Thus this method followed makes this diode multifunction device.

4.8 Return Loss Minimization:

Return loss at this point is not very bad but we need a short circuit to provide ground for dc bias. So, it will be advantageous to use this short-circuited stub to further reduce return loss.

After doing a similar single stub setup for matching as done in section 4.5, results are shown in Figure 4.17 were obtained.

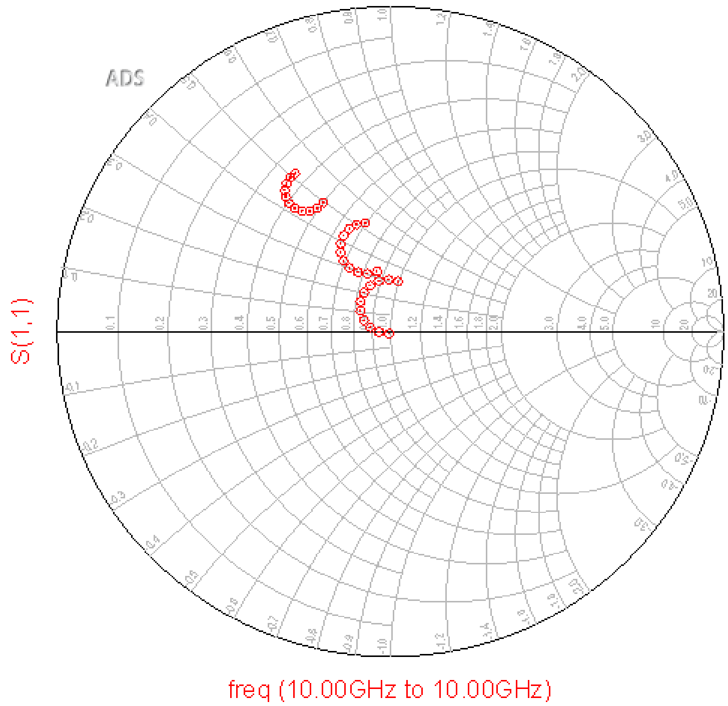


Figure4.17 Simulated results Return Loss Minimization

Optimal values are the ones close to 1 or center of smith chart. Selected stub Length is 4mm and distance is 1mm. But, as we have space available to the edge of whole substrate, a half wavelength can be added to 1mm. This makes it 7.03mm.

4.9 Final Layout:

All the lengths have been optimally selected. Combining all the part, the final layout is ready. The diameter of all the holes is 0.5mm.

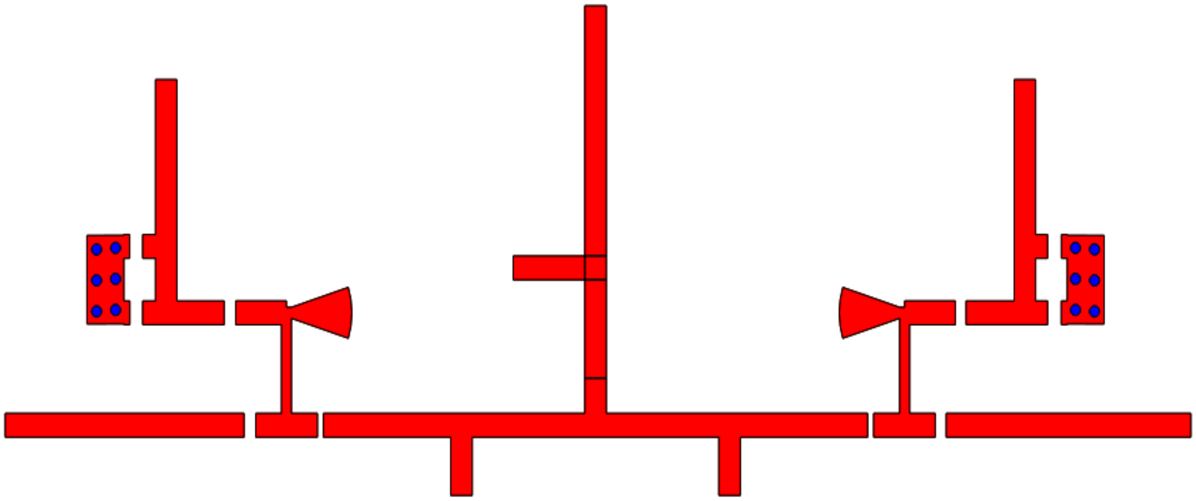


Figure4.18 Final SPDT Layout

4.10 Simulation Results:

Placing all components in schematic and turning one diode on and the other diode off, plots are simulated for insertion loss, return loss and isolation. A priority was given to insertion loss during design. So, a better insertion loss graph is expected.

4.10.1 Return Loss:

At 10GHz, a return loss of -13dB is attained. Most importantly, dip of graph around designed frequency is clearly recognizable.

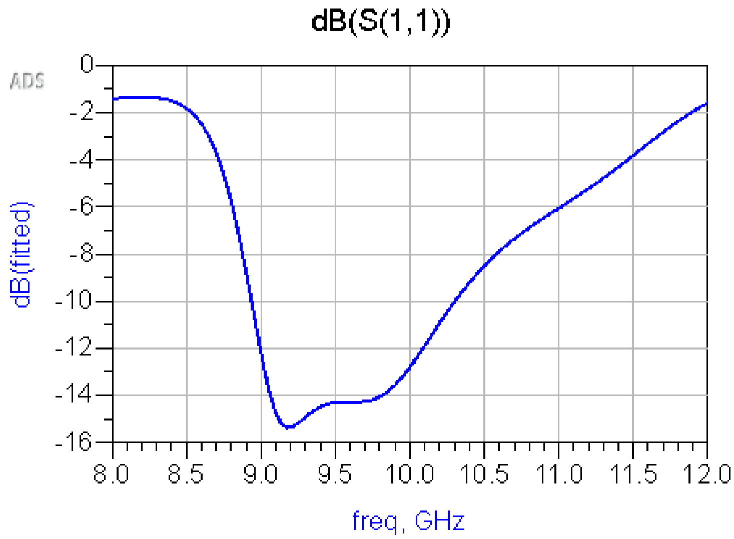


Fig4.19 Simulated Return Loss of SPDT Switch Design

4.10.2 Insertion loss:

From 9 GHz to 10.6 GHz, Insertion loss is pretty close to 1.5dB. Thus, a large band of frequency is available with good insertion loss.

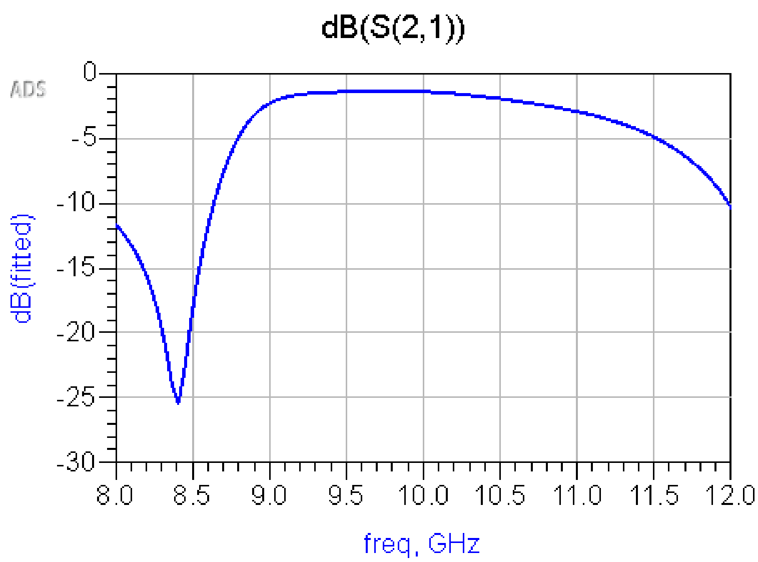


Figure4.20 Simulated Insertion Loss of SPDT Switch

4.10.3 Isolation:

The isolation remains less than -10dB throughout the X-band.

Bandwidth is not very great as this the compromise made during designing to improve insertion loss.

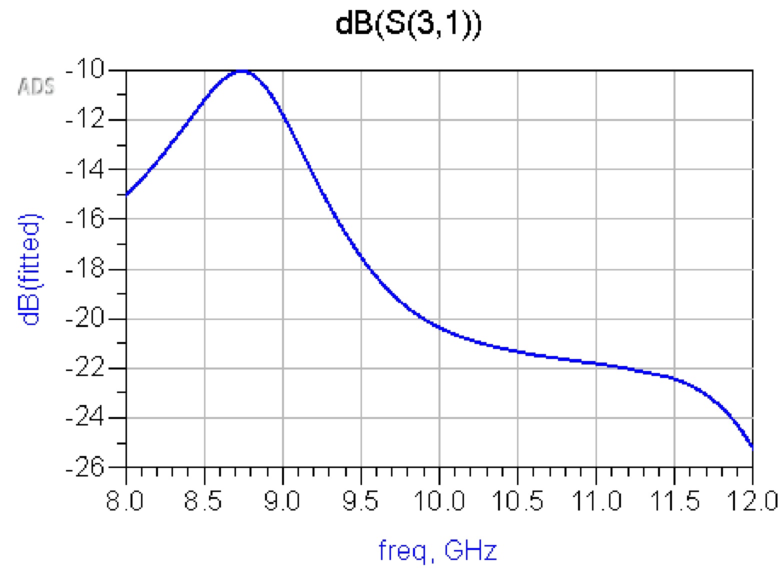


Figure4.21 Simulated Isolation curve of SPDT Switch

A switch is successfully designed that gives excellent results. All the lengths are set logically by following the theory of Microwave Engineering. Above all, results are explainable and expected.

Time domain analysis is not possible as diode approximate models are being used that only model the impedance characteristics. Switching time cannot be performed until a spice model of diode is available.

CHAPTER 05 Fabrication and Results

The fabrication of project was initiated after design of SPDT was completed. Holes for M2 screws were placed at four locations to hold the substrate on a metal plate. The fabrication process is completed in certain steps. We will discuss in detail in this chapter. Measured results will also be presented.

5.1 Layout Printing

The layout of SPDT switch is etched on substrate of RO4305B whose thickness is 0.508mm or 20mils.The Figure 5.1 shows the printed layout of our design. There are certain techniques for RF layout printing. LPFK milling machine at RWR, Rawalpindi etched our layout.

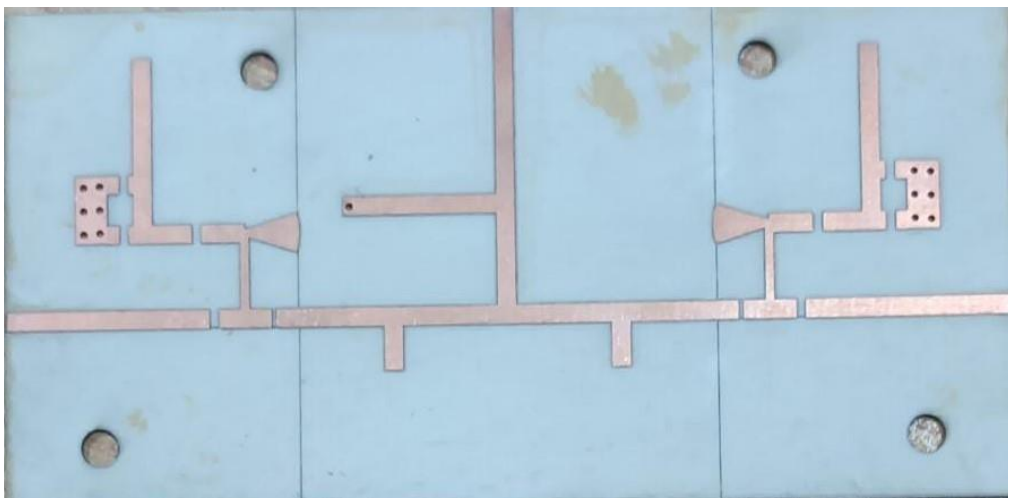


Figure5.1 Printed Layout on RO 4350B substrate

5.2 Ground Plate

The plate has been designed for SPDT switch. It is designed on the same dimension of substrate layout. The designed also includes the holes for DC ground and also the SMA connector ports. The height of plate is 0.7cm.

The 3D model has been designed in SOLIDWORKS CAD. The model was fed into a CNC machine to obtain a physical product. The dimensions of plate and holes will be discussed later.

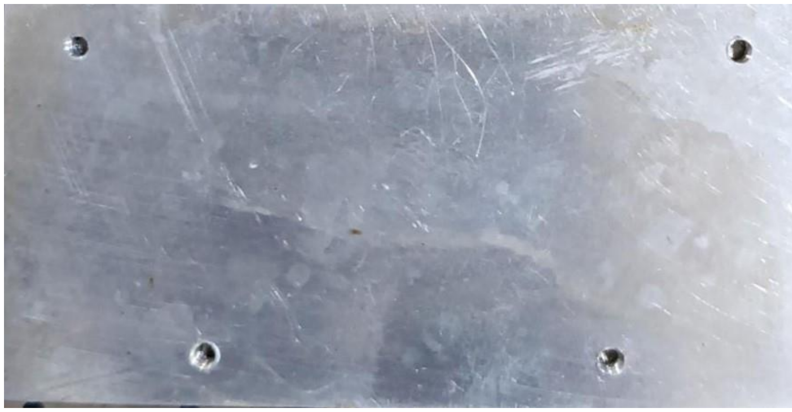


Figure5.2 Ground Plate

The dimensions of plate are 6cm x 3cm x 0.7cm to fit the printed circuit on to it. M2 screws were used to hold the substrate on plate. The diameter of hole is 1.1mm

5.3 SMA Connectors and Screw

SMAs used in practice are manufactured by local brands. They are not very reliable but do the job for educational projects. They will definitely produce some losses and reflections.

Fig5.3 SMA Connector

Screws need a hole of 1.1mm diameter. Their heads are roughly 4mm wide. Holes and threads were made on the metal plate by CNC machine.

5.4 COMMONENTS SOLDERING

Two Beam Lead diodes, six capacitors, two 43 Ohm resistors and three SMA connectors are to be soldered on the substrate. Soldering at such small dimensions is in itself a skill that we had to learn. We were helped by MERL lab staff at CEME, Nust.

5.4.1 PIN DIODE SOLDERING

The beam lead pin diode is a very critical part of our project. The dimension of beam lead is 0.28mm which is very small number. It is hardly visible by naked eye. The holding of diode from package is first task. The diode got destroyed couple of times due to its structural weakness.

Procedure of diode soldering:

With use of tissue and adherence fluid propanol, we held the device and placed it on required area with help of microscope. The adjusting of diode process is done with help of toothpicks and tweezer.

The orientation of diode is in such a way that tapered corner is cathode and flat end is anode. The cathode should face towards the RF input for both diodes.

The solder paste is applied on both legs of diode. The amount of solder paste should be equal on both sides otherwise during soldering the orientation can be off-track.

The assembly is now placed on hot plate and is heated till 230degree Celsius. The solder paste melts and diode legs get attached to RF path.

DC Testing of diode:

One cannot be sure about this procedure of diode soldering as standard practice to solder this diode is by using a specialized machine that is not available to us. The diode test is important before the soldering of other components. The test is conducted without providing RF signal, the DC biased is applied. Table 5.1 shows the bias points obtained experimentally.

Table 5.1 DC characteristics of Diode

Experiment No	Voltage(V)	Current(mA)
1	0.5	0
2	0.7	0.3
3	0.8	2.8
4	0.9	30
5	1	50

5.4.2 SMD Soldering

SMD components are relatively bigger with length 1.5mm. Solder paste is placed at both sides of gap where SMD is to be placed. SMD of required value is picked with a tweezer and placed on the solder paste. A microscope can be used to better do the job. After verifying the placements, whole assembly is placed on a hot plate and heated to 230 degrees Celsius.

After soldering all the components and wires, the final SPDT switch snapshot is attached in Figure5.4:

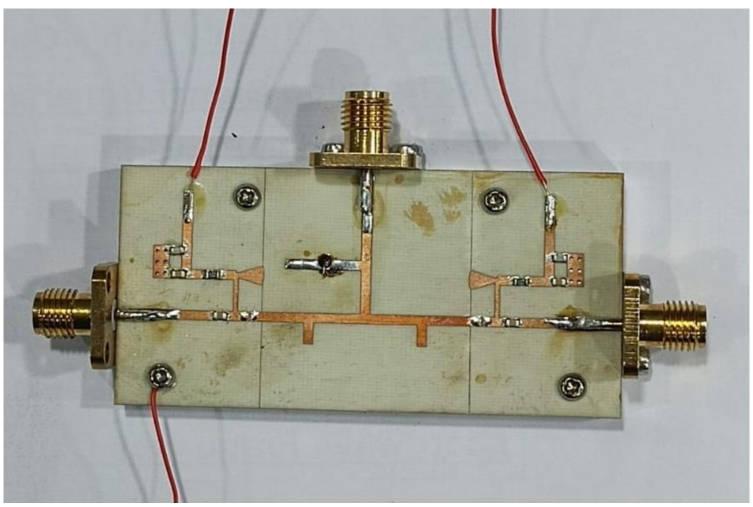


Figure5.4 Fabricated SPDT Switch

5.5 TESTING Setup

PNA E8363B (Agilent Technologies) was used to obtain s-parameters of Fabricated switch.

Figure5.5 Network Analyzer PNA E8363B

PNA is calibrated using a calibration box given by the company. Box uses TRL calibration technique.

Input of switch is connected to port 1, one output side is attached to port 2 of network analyzer and other output side is terminated into 50-Ohm impedance.

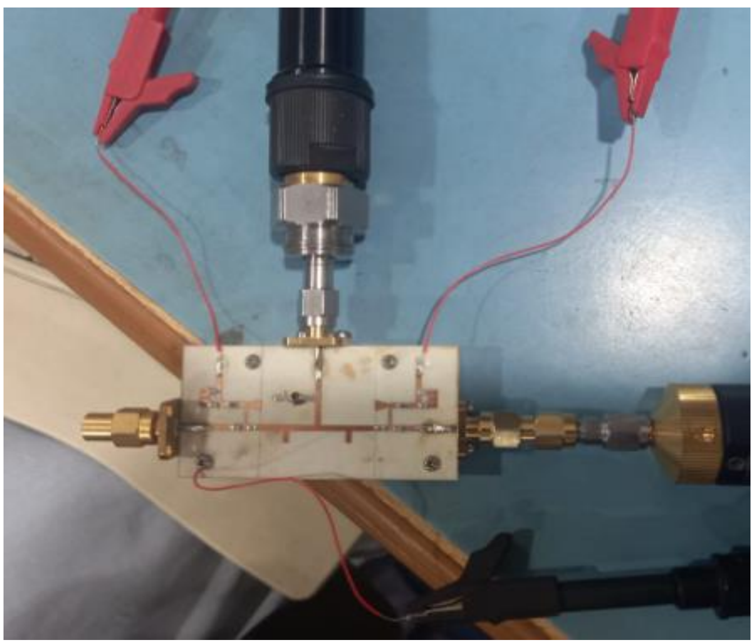


Figure16 S-parameter Testing Connection of SPDT Switch

Dc bias is applied. One diode is given positive voltage and other is reversed biased by a negative voltage. Ground is common for both diodes.

5.6 Measured Results

On state performance is shown in Figure 5.7. Diode is forward biased at 44mA by positive dc voltage (V = 4.2V) at room temperature. Insertion Loss of SPDT switch is -3.8dB. Return loss of port 1 is -13.96dB as shown in yellow and insertion loss is in blue.

Figure5.7 Measured S-parameters of ON- state of SPDT switch

For measurement of isolation in Off state, the diode is reversed biased at -20V at room temperature. S-parameter results are shown in Figure 5.8. Measured isolation is -18.8dB at 10 GHz. Return loss of port 1 is -16.03dB as shown in yellow and isolation is in blue.

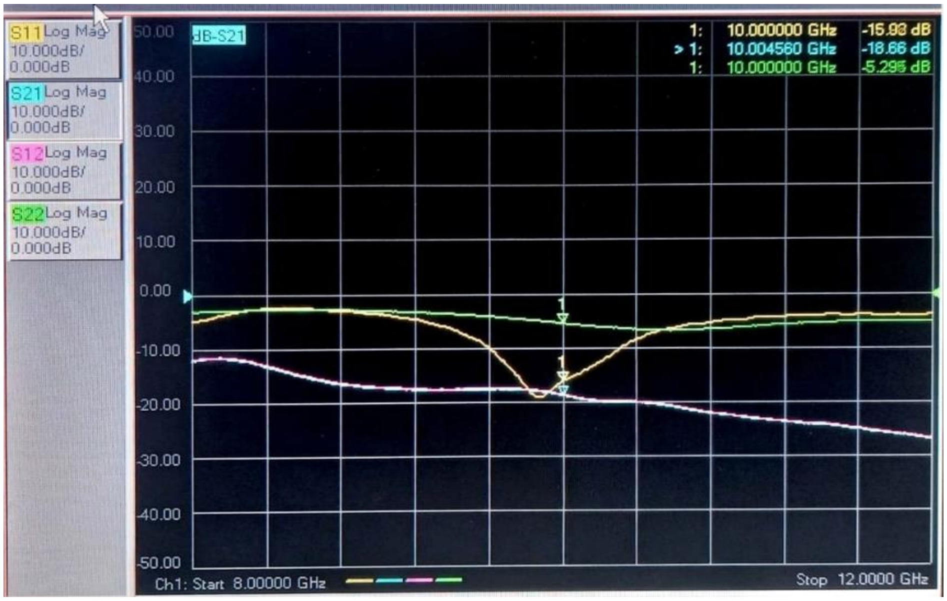


Figure5.8 Measured S-parameters of OFF-state of SPDT switch

Table 6.1 provides the result comparison between the simulated and measured results of the SPDT.

Table 6.1 Comparison of simulated and measured results of SPDT

Parameter	Simulated	Measured
Return Loss	-15 dB	-13.9 dB
Insertion Loss	-2.5 dB	-3.848 dB
Isolation	-19.2 dB	-18.6 dB

CHAPTER 6: CONCLUSION AND FUTURE WORK

In this project an SPDT switch at 10 GHz was designed, fabricated and tested. The switch uses a series configuration and a Silicon planar beam lead PIN diode, implemented in a circuit made of microstrip transmission lines. The switch was designed using Keysight ADS and implemented on Rogers RO4350B low loss substrate. The final device dimensions are 6 cm x 4 cm.

The SPDT switch was measured on an Agilent Network Analyzer E8363b. Measured isolation is approximately -18.8dB and insertion loss is -3.8dB at 10 GHz. Although the switch provides reasonably good performance at 10 GHz, however there is slight variation in simulated and measured values. These variations in values are a result of imperfect soldering process, non-standard SMA connectors and small radiation losses. Moreover, the simulation is based on package PIN diode model, which is an approximation.

In future, the circuit layout of the switch can be improved to develop a compact circuit and the circuit should be enclosed in a metallic box. Moreover, the switch needs to be characterized for its Turn-on and Turn-off switching speed, and the circuit optimized to achieve very small turn-on and turn-off switching speeds on the scale of few nanoseconds.

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