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NUST COLLEGE OF ELECTRICAL AND MECHANICAL ENGINEERING

Exploring Negative Group Delay in Passive Circuits

A PROJECT REPORT

DE-40 (DEE)

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BACHELORS

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NUST COLLEGE OF ELECTRICAL AND MECHANICAL ENGINEERING

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DEDICATION

This project is dedicated to our parents, their efforts and all the prayers were with us during the project. It is also dedicated to our teachers and all the technical staff who really helped us for the completion of this project.

CERTIFICATE OF APPROVAL

It is to certify that the project "**Exploring Negative Group Delay in Passive Circuits**" was done by **NC Ali Raza Mustafa, NC Bilal Khalid, PC Samia Noor and NC Subas Muhammad** under the supervision of **Dr. Mojeeb bin Ihsan.**

This project is submitted to **Department of Electrical Engineering**, College of Electrical and Mechanical Engineering (Peshawar Road Rawalpindi), National University of Sciences and Technology, Pakistan in partial fulfilment of requirements for the degree of Bachelors of Engineering in Electrical engineering.

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DECLARATION

We hereby declare that no portion of the work referred to in this Project Thesis has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning. If any act of plagiarism found, we are fully responsible for every disciplinary action taken against us depending upon the seriousness of the proven offence, even the cancellation of our degree.

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ACKNOWLEDGEMENTS

It is with immense pleasure that we write this report and acknowledge the efforts of many people whose names may not appear on the title page, but their hard work, friendship, cooperation, and understanding was with us to the production of this report.

Here we would like to mention the support and guidance given by our supervisor Dr. Mojeeb bin Ihsan. His availability and prompt responses to our issues aided us in successfully finishing this job. Our department (Department of Electrical Engineering) is responsible for enabling us to complete this project and produce outcomes.

Abstract

Group delay is an important factor of consideration while designing a circuit with minimum signal distortion. There have been various attempts to minimize this group delay using different techniques, one of such techniques is to introduce Negative Group Delay (NGD) in the circuit to compensate for the positive group delay and to reduce group delay variability in pass band. In this project, in order to explore and study NGD phenomenon, we studied and implemented, based on published work, two passive circuits having negative group delay characteristics. First circuit having NGD characteristics is O=O shaped circuit which consists of a power divider and a power combiner. It produced an NGD of -0.995 ns and S_{11} of -18.6 dB. The circuit produced NGD without using any resistors while operating at 1.2 GHz.

Second circuit is a power divider operating at a center frequency of 1.8 GHz. The PD circuit incorporates a resistor and coupled line structure that provides matching and NGD characteristics. This circuit was designed using the technique reported by Girdhari Choudhary et. Al. [18] but for operation at a different frequency and using a different substrate. The PD was implemented on FR-4 substrate with a height of 40 mils and it produced excellent matching with S_{11} = -21 dB and NGD was measured to be -2.6ns at 1.8 GHz frequency. In order to investigate the effect of substrate height, another Power Divider was designed and implemented on a substrate of height 31 mils. For this circuit, the measured NGD was -0.8ns and S_{11} = -26 dB. These results show that an increase in the height of substrate results in a higher value of NGD which may be attributed to higher losses suffered by the circuit fabricated on a substrate of larger height.

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Chapter 1: Introduction

1.1 Introduction:

With the development in the communication systems such as ultra-wideband communication system, 5G technology, multiple-input/ multiple-output technology demands better quality of the transmission of the signal, and it is always the major concern in the communication technology. To achieve better quality of transmission, the focus should not only be on amplitude characteristics of the signal but also on phase characteristics as well. This is because of the distortion in the signal and long phase delays experienced by it are due to the positive group delay in the transmission lines. There were many methods to reduce the positive group delays in the signal transmission but out of all the methods, the most effective one is Negative Group Delay.

In microelectronic devices, some of the main problems include transistor latency and propagation delays in the interconnections between the transistors. As the circuits are getting smaller and the switching time of one transistor to the other is also becoming faster, the propagation delay can become significant. This propagation delay is caused by the resistivity of the inter-connecting evaporated metal wire and the insulator's dielectric constant which supports that wire. One of the contemporary solutions include using copper wire in place of traditionally used aluminum or by using those insulators that have less dielectric constant to reduce the propagation delays but still, these methods do not remove the delays completely. So, one of the effective approaches is to use negative group delays to remove the propagation delays efficiently. A well-known effect called ‘clock-skew’ is present in microelectronic chips which is related to the time synchronization. In these chips, different signals have different paths between the transistors due to which some of the signals reach early on time and some experience delays in their propagation which stops us to apply high clock frequencies because all signals must be delayed because of already delayed signals to make them harmonized. Compensation techniques can make signal routes independent of each other and eradicate the need to incorporate delays in the paths of the signals to synchronize them.

Because of the effective compensation of the positive group delay, Negative Group Delay (NGD) circuits are widely used in microwave circuits such as in feedforward amplifiers to improve efficiency, in phased- array antennas to minimize the flatness in beam-squint delay, in phase–shifters to reduce phase variation due to frequency, and in power dividers and couplers to eliminate PGD.

1.2 Group Delay:

Brand and Nyquist presented the idea of Group Delay to explain phase linearity. Group delay is defined as the delay of a whole signal when it is passed through a system of transmission.

$$\tau_g(\omega) = -\frac{d\phi(\omega)}{d\omega}$$

Where φ (ω) is the phase, defined as φ (ω) = ∠ S_{21} where S_{21} is the s-parameter of the system and is known as the transmission coefficient of any 2-port system. Group delay is defined as the negative derivative of the phase response with respect to frequency and the given equation can be derived as:

$$\tau_g(\omega) = -\frac{d\angle S_{21}}{d\omega} = -\frac{d}{d\omega}\left[\arctan\frac{\mathrm{Im}(S_{21})}{\mathrm{Re}(S_{21})}\right]$$

This equation describes the phase-frequency curve, and it is shown in **Figure 1.1** that when the slope of the system is negative then the group delay is positive and when the slope is positive then the group delay is negative.

One thing which must be noted about the group delay is that it is not the delay of a signal of single frequency as it is the delay of the entire signal envelope that's why group delay is also known as envelope delay.

1.3 Group Velocity and Phase Velocity:

Before going towards what negative group delay and its superluminal effects, one should know about the terms, phase velocity and group velocity.

1.3.1 Group Velocity:

To understand the concept of group velocity, let us take an example of a group of signals. Each signal is travelling at its own velocity but the velocity at which all the signals are moving in a group is the group velocity.

Coming to wave mechanics, group velocity is related to wave packets and a wave packet is made up of different waves. In a wave packet, each wave is moving differently and has its own velocity which is different from other waves. This wave packet acts as a particle and the velocity

of the wave packet represents the velocity of the particle, this means the velocity of all the waves constitute the velocity of the particle and this velocity is called the group velocity which is represented as:

$$v_{\mathrm{g}} \equiv \frac{\partial \omega}{\partial k}$$

Where ω is the angular frequency and k is the wave number.

For the transmission of information, superposition of the number of waves is required which all constitutes a wave packet.

1.3.2 Phase Velocity:

Contrary, velocity at which any constant phase point of the wave travels is called the phase velocity

$$v_{\mathrm{p}} = \frac{\omega}{k}$$

Carrier wave moves with phase velocity in a wave packet, but phase velocity is not important when we talk about wave packets. Phase velocity is important when we are talking about individual waves

1.3.3 Relationship between group velocity and phase velocity:

How both the velocities are related depends upon the properties of the medium in which the wave is traveling.

In the case of non-dispersive medium, phase velocity is independent of wavelength, so this implies:

$v_p = v_g$

In dispersive medium:

$v_p > v_g$

In an anomalous medium:

$v_p < v_g$

1.4 Negative group Delay:

When the slope of the phase-frequency curve of the group delay is positive then the delay is negative group delay, it occurs in that frequency range where signal is mostly attenuated.

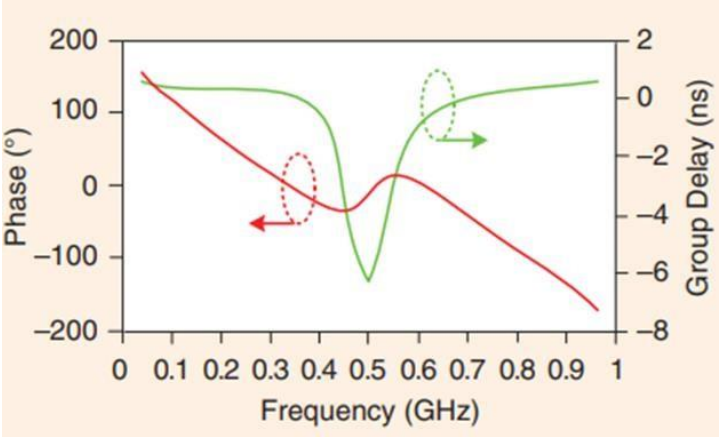


Figure 1.1: Negative Group Delay Curve (taken from [1])

Negative group Delay is used to compensate positive propagation delays in the transmission systems and minimizes the delay time of the signal transmission

1.4.1 NGD and Superluminal Phenomenon:

The phenomenon of the negative group delay is based upon the superluminal phenomenon in which the speed becomes greater than the speed of light. Here the superluminal speed does not mean the speed of the transmission of the signal, but this speed is the group velocity of the signal. One can raise a question that the speed which is greater than the speed of light contradicts the theory of relativity, however it is not the case here and this will be explained shortly.

Many experiments were performed in the initial stages to achieve NGD and how it does not contradict the theory of relativity and the system remains causal irrespective of the casual behavior of the system.

Suppose a Gaussian pulse is fed into a resonant circuit which is lossless then the output pulse will have its peak after the peak of the input pulse and the system has positive group delay and time of output pulse (t_{out}) minus the time of input pulse (tin) > 0. But when loss is introduced in the circuit then the output pulse comes before the input pulse and $v_g > c$ and we have a superluminal effect, $t_{out} - t_{in} < 0$ and negative group delay is produced. For the NGD, it is

compulsory that there is loss in the system and the lossy system produces negative group delay.

One of the many experiments that were performed for NGD was Operational Amplifier with RLC circuit in a negative feedback loop [2]. The RLC network produce negative group delay in the circuit i.e., the output pulse left the output port earlier than the input pulse entered the input port. The system is supposed to be non-causal but that is not the case because there was enough information in early analytic voltage that produced the whole output signal advance in time.

Similar experiment was also performed but with a high gain feedback loop with a passive filter in the feedback [3] which caused a positive propagation delay in the circuit so the amplifier was supposed to produce a signal at the output with negative group delay such that this will cancel out the positive delay. This system seemed to be non-causal, but it is causal, because as soon as the input voltage was set to zero, output waveform also became zero, verifying the principle of causality which depends upon the discontinuities in the system.

In conclusion, to the principles discussed in this chapter, one can incorporate a physically realizable phenomenon of Negative Group Delay even in electronics to enhance circuit performance (as it will be seen in chapter 2). In this project we have utilized NGD phenomenon to reduce the effects of positive group delay in a power divider, which is a fundamental component of microwave systems at frequency 1.8 GHz, an important frequency in the radio spectrum.

Chapter 2: Literature Review

2.1 Literature Review:

As the rapid growth in technology and with the rise of internet, the world is moving towards more devices, smaller circuits, and better connectivity between those devices. This requires development of next generation communication technology for fast data transfer like 5G and 6G technology, at the same time these communication systems need to maintain the quality of signal transmission.

The quality of a signal can suffer due to signals' amplitude as well as its phase. As a result of non-constant positive group delay different frequencies, that make up a signal, can take different time to pass through a circuit or a filter. This dispersion of signal to its constituent frequency can cause signal distortion [4]. Many studies have been carried out to counter the effects of positive group delay. To maintain the integrity of signal waveform a synchronization technique utilizing Memristive elements[1] have been proposed in [5][6], but this comes with the price of increased power consumption. The dispersion effect is reduced in [7][8] with the help of all pass network, but the reduction in group delay is not obvious.

These procedures lessen propagation delays, but they don't eliminate them completely. It is possible to eliminate these types of delays by using a new strategy that utilizes negative group delays to make up for the time lost due to the original delay. It is feasible, for example, to eliminatethe interconnect's positive propagation delay by precisely compensating with a negative group delay that is equivalent but opposite.

Delays in signal can also cause problems in computer chips, an effect known as "clock skew," where different pulses arrive at different times due to being routed through different paths. As a result, this prevents the use of higher clock rates, because extra delays must deliberately be added to early arriving pulses to force all pulses to arrive simultaneously at the final gate [9]. So, one can utilize a negative group delay scheme viable for integrated circuits to cancel the effects of positive group delay. From this example one can see that positive group delay can affect not just communication technology but it can also cause problems in many other domains of physical science. But throughout this project we limit our discussion to microwave circuits only.

As was shown in the previous chapter, it is not the peaks in the voltage waveform but the presence of discontinuities in the signal, such as "fronts" and "backs," that lead to causality. A conventional Negative Group Delay (NGD) circuit can be realized with the help of series or shunt RLC resonators [13], it operates at low frequencies ranging from few MHz to 100MHz at the same time it suffers from high insertion loss. Narrow bandwidth of NGD and the performance degrades due to the temperature-dependent resistive variations.

It was shown in section 1.4 that the relationship between group delay and the amplitude of S_{21} (insertion loss) i.e., greater attenuation of S_{21} will introduce greater NGD. This can be considered a major disadvantage of NGD circuits because of more power consumption required by their large signal attenuation. While designing an NGD circuit one should focus on the parameters like NGD time, bandwidth, signal attenuation and matching. One can design a NGD circuit based on a Band

[1] Memristor (memory-resistor) controls the amount of current flow through circuit and holds the amount of previously flowed charge i.e., they retain memory without power

stop filter [11] because of their similar signal attenuation characteristics. However, one cannot achieve good overall performance of the NGD parameters. Signal attenuation can be achieved by introducing defects in the microstrip line as a result one can achieve a negative group delay, this approach is used [12] where multiband negative group delay is achieved with adjustable center frequency.

The effect of signal attenuation can be made up by introducing an active circuit after the NGD stage. Amplifiers were used [13] [14] to compensate for the loss and to operate in higher frequencies. It was found that these active NGD circuits would suffer from design flexibility due to variable component values and increase the design difficulty due to bias network in the microwave band. Due to the increase in difficulty and the fact that we are unequipped with the knowledge of active microwave circuits at undergraduate level, we fix our attention towards achieving NGD in passive microwave circuits.

All the methods of achieving NGD discussed above focused only on achieving better NGD performance. However, if one wishes to include a NGD circuit along with other microwave circuits then matching should be cared about. Therefore, later efforts were made to achieve NGD without compromising on the matching of the circuit. The impedance transformer can be used to make a matched NGD circuit, however the matching transformer makes the circuit larger and the NGD characteristics become more unpredictable and may eventually decrease in the overall circuit [15].

NGD can be achieved by signal interference, where the loss in signal is introduced due to partial destructive interference. For S_{11}, it is reduced considerably because of the use of coupled lines for matching and achieving negative group delay. To improve the stability of microwave terminals and reduce their susceptibility to SWR and stability concerns, pair lines are often used. Combining both techniques i.e., signal interference for introducing Negative Group Delay (NGD) and coupled lines for matching is utilized in [16]. The resultant circuit consists of Wilkinson power dividers; the first divides two signals with unequal power while coupling lines produce phase shift and provide matching, and the second combines the two signals with equal power division ratio.

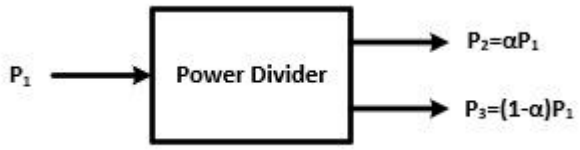
In the start of this section, we focused on the effect of negative group delay on communication technology. Carrying the same example, we can think of a signal through a transmitter that can experience distortion due to positive group delay. To cancel that positive group delay one can, incorporate negative group delay in the already present sub circuits of the transmitter block, one such circuit is a power divider. A Power Dividers is a basic circuit used extensively in the field of radio technology like radar [17] or transmitter (the functionality of power divider is covered with more detail in chapter 4). In this project we wish to achieve Negative group delay in a power divider circuit, with the help of [18], centered at 1.8 GHz an important frequency in the radio spectrum. Since negative group delay is achieved by introducing losses like attenuation, as established earlier, we plan to study the effects of other losses, like substrate height, on the performance of NGD.

All designs present in this work were simulated using Keysight ADS while for extracting the parameters MATLAB was used. The circuits were fabricated on microstrip structure and tested using Vector Network Analyzer (Model: Agilent E8363B).

Chapter 3

3.1 Power Dividers:

Power dividers are passive components that are used in microwave technology for purposes of power division & power combining. A simple power divider consists of a T-junction that is usually a 3-port network with one input and two outputs. In a simple Power Divider, input is applied to one port which splits the applied power into two power outputs at the other two ports. Power Dividers are usually designed to have the same power division ratio which are in phase with each other. But there are other methods available for designing a power divider with an unequal power division. Power dividers can behave as a power combiner if operated in reverse order. An illustration of the power divider and power combiner is shown in **Figure 3.1**.



(a)

(b)

Figure 3.1: (a) Power Division & (b) Power Combining

Figure 3.1(a) represents the power division in two equal parts and **Figure 3.1 (b)** represents the power combining.

3.2 Wilkinson Power Divider:

A simple T-junction can be lossless and lossy. The lossy T-junction is made by inserting the resistors among transmission lines. Isolation is not achieved in a resistive divider though it provides matching at all ports. From chapter 7 of [19], we know that a three-port network can be realized in two ways

- If any of two ports of a 3-port network are matched, then a reciprocal and lossless three port network can be made.
- The network is non-reciprocal, so a lossless and matched three port networks can be realized.

A Wilkinson power divider is such a device that provides lossless and reciprocal condition, but it also solves the problem of isolation faced in the simple resistive T-junction power divider. The matching condition in all ports is solved by adding a resistor in between port 2 and 3. The resistor not only provides the matching but also provides isolation between port 2 and 3. WPD (Wilkinson Power Divider) uses two quarter-wave transformers to divide input power in equal and in-phase signals at output ports. Due to reciprocity, the WPD can also be used to combine two equal and in-phase signals in one single signal. A Wilkinson power divider is given below in **Figure 3.2**.

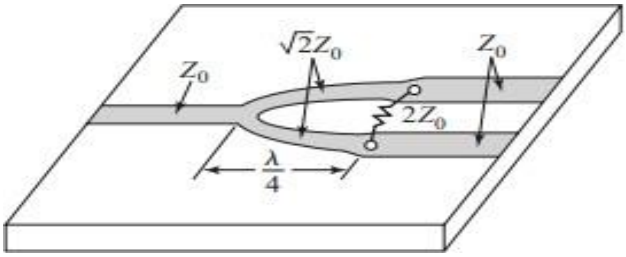


Figure 3.2: The Wilkinson Power Divider (taken from [19])

In the following sections of this chapter, we familiarize ourselves with the ADS environment.

3.3 ADS Familiarity:

The main purpose of this step was to get familiar with the working of ADS and its tools like

- Linecalc
- Layout Design
- Port Modeling
- Parametric Analysis
- Substrate Design
- EM Simulation Setup
  - Momentum Setup
  - Cosimulation Setup

3.3.1 Linecalc:

Linecalc is used to calculate the length and width of the port or different transmission lines of a certain characteristic impedance at a specified frequency. Parameters(length and width) for different types of Transmission Lines(like microstrip, strip line and coaxial line etc.) can be calculated along with different shapes like coupled lines. Linecalc takes specified design frequency, specifications for coupled lines or Transmission lines (T/Ls) like their coupling coefficient and electrical length respectively and equivalent characteristic impedances. Substrate parameters like relative permittivity ε_r, thickness, T of substrate, thickness of copper H and loss tangent (tanD) of the substrate are also inserted as input in Linecalc. The GUI (Graphic User Interface) of ADS Linecalc is given in **Figure 3.3**.

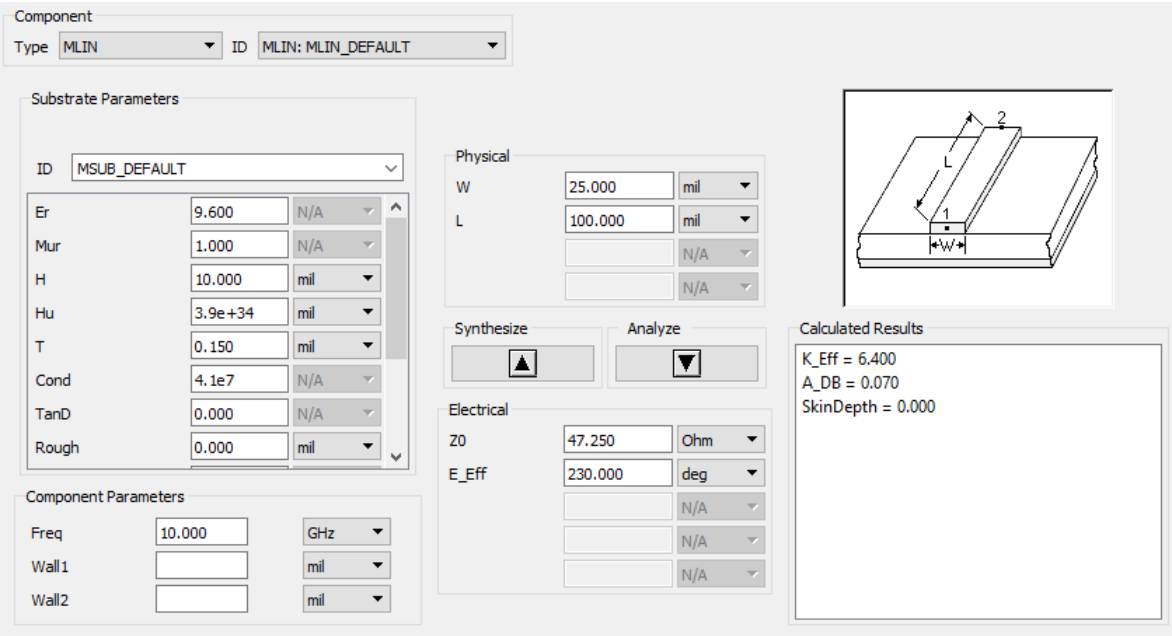


Figure 3.3: Linecalc GUI

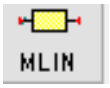
W and L represent the length and width of the transmission line. After substituting all relative parameters, the Synthesize button is used to calculate the length and width. Moreover, the units can be changed from mils to others such as cm, mm, inch, ft and meter.

3.3.2 Layout Design:

For designing the circuit or network there are a variety of options in the ADS Layout Design Window. Some of the most commonly used parts are given below. The diagram of each component is taken from ADS software. The details of common parts are:

MLIN:

It is used to make transmission lines of a certain length and width obtained from Linecalc.



MTEE:

It is used to connect three different transmission lines in which two of them are at 90 degrees from horizontal T/L and vice versa.

Mclin:

It is used to make coupled lines of specific width, length and spacing obtained from Linecalc.

Mcorn:

It is used to shift one T/L connection with another T/L at 90 Degrees.

Mcurve:

It is used to shift one T/L connection with another T/L at any specific degree.

3.3.3 Port Modeling:

Port modeling can cause errors in the simulation if not done correctly. ADS layout has many options for different port shapes as shown in drop down menu of Figure 3.4:

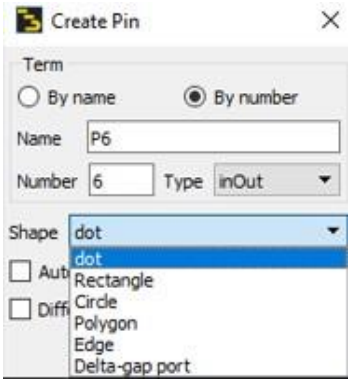


Figure 3.4: Pin Selection Menu in layout

But using the default dot port can be problematic because when it is connected to T/L it takes the entire length along that side of T/L as a port which we do not want. So, we must change the shape of the port into a rectangle as the width and length of the rectangle can be adjusted as we desire so that it takes less area on the T/L. This rectangle will be considered as a port instead of the entire length of T/L. If there is a resistor in design it becomes difficult to do correct momentum simulation. To avoid this a differential port is used. It takes two ports as one which can be assigned the value of resistance for accurate momentum simulation results.it can be made in the port editor or you select the differential port box in the create pin in the above **Figure 3.4**. The feed type should be direct for a differential port.

3.3.4 Parametric Analysis:

Parametric Analysis is especially useful for design optimization. If one wants to check the behavior of the circuit at different lengths and width it becomes difficult to change it manually every time as it is time consuming. So, to avoid this ordeal parametric analysis is used. It is done by making the length and width as variables in the ADS design layout. The method for that is to go to toolbar then select **EM >Component>Parameters**, and a window, as in **Figure 3.5**, opens up.

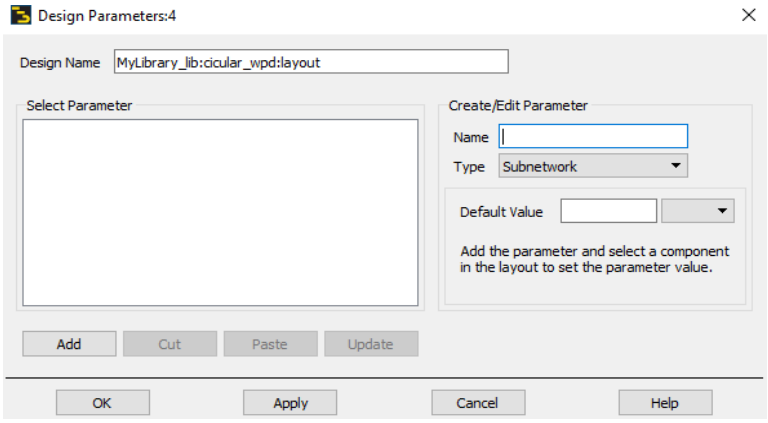


Figure 3.5: Defining parameters in Layout

The parameter can be defined in the above window of **Figure 3.5** with some default value in mm. To assign the parameter to T/L length and width, simply replace the w and l of the T/L window with the parameters you want to assign. Then open the EM simulation and set the frequency without pressing the Simulation button on the simulator. Then the EM setup model is created by selecting **EM >Component>Create EM model and Symbol** form toolbar**.** With generated symbols, create a schematic and use **PARAMSWEEP** block to give the minimum and maximum values you want to change for the specified length or width with variable declaration in SweepVar as shown in **Figure 3.6**.

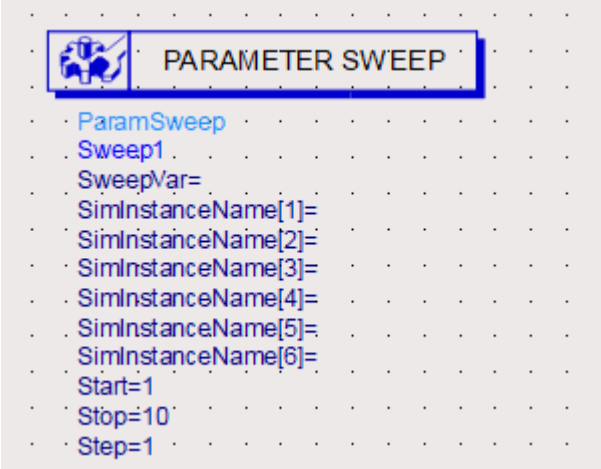


Figure 3.6: Parametric sweep setup in schematic view

3.3.5 Substrate Defining:

For simulation it is particularly important to define the substrate. ADS has many substrates available in the database but if you want substrate that is not present in the database you can also add manually. The substrate design layout in ADS is shown in **Figure 3.7**.

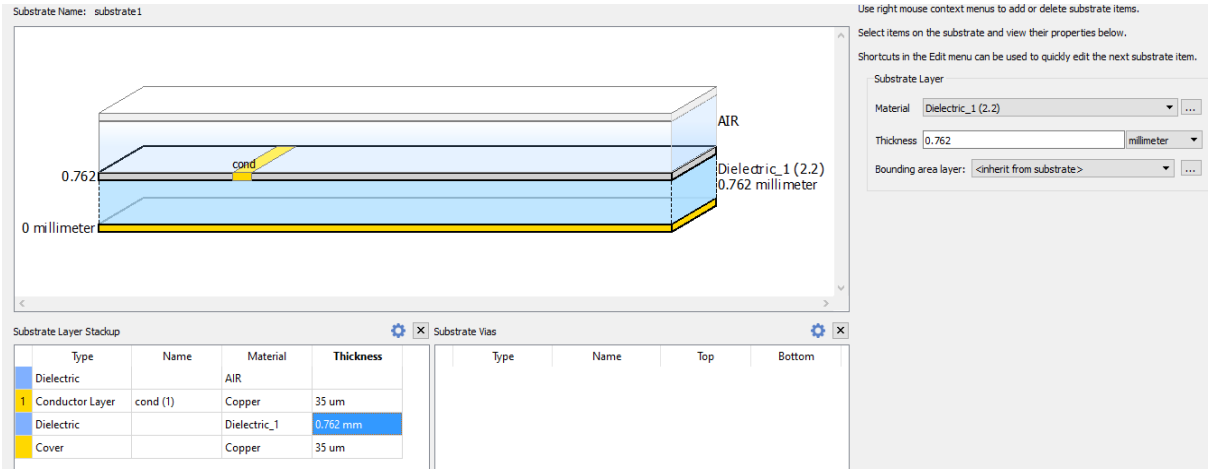


Figure 3.7: Substrate Design Layout

In order to add a substrate manually, the values of relative permittivity ε_r and loss tangent(tanD) of the desired substrate are added along with the conductivity of a conductor (cond) and dielectric thickness of substrate according to design requirements. These values are added to ADS substrate design layout to make desired substrate.

3.3.6 EM Simulation Setup:

The major things to mention while correcting the settings of EM setup are

- The frequency plan selected should be **Linear** instead of **Adaptive.**
- For Momentum Simulation
  - Make sure the edge mesh is on from options (Options>Mesh>Edge Mesh)
  - Ensure the EM model exists when simulation is launched

A simple EM model layout is given in **Figure 3.8**.

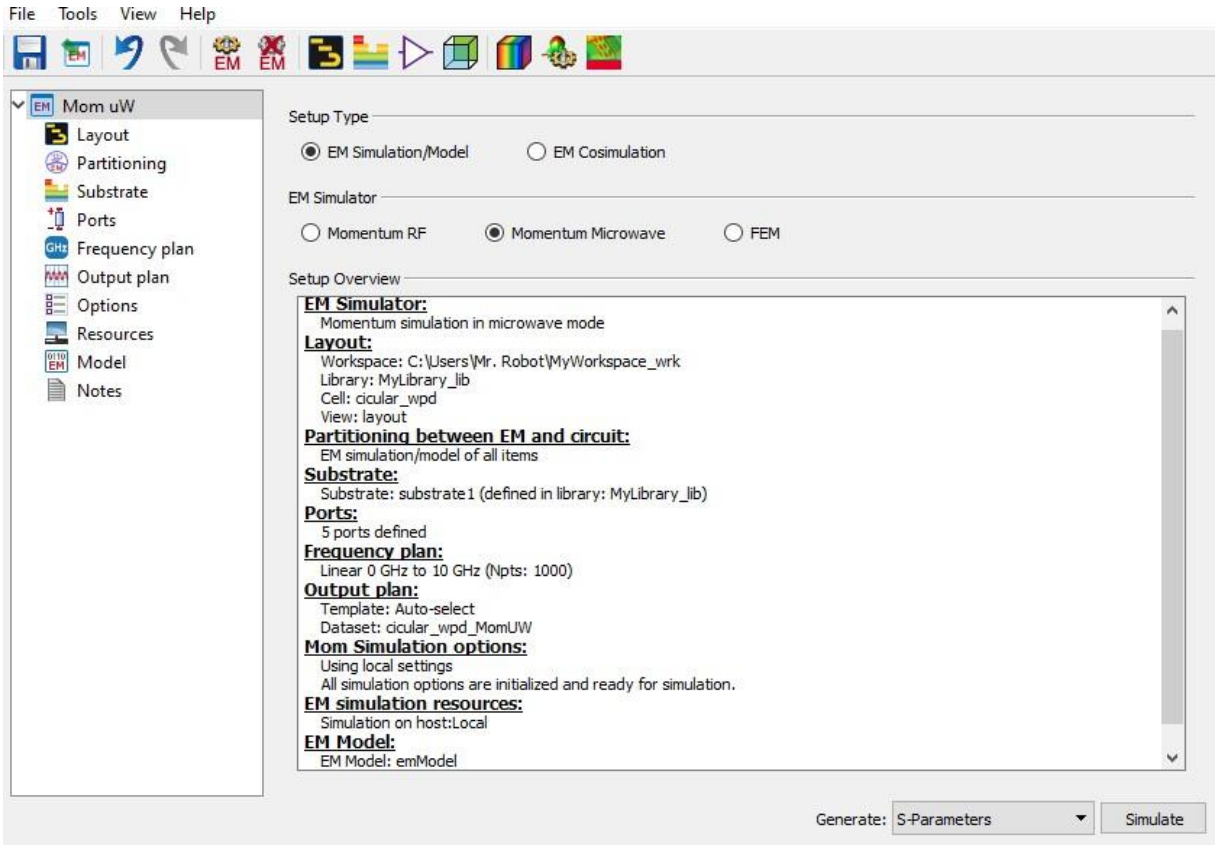


Figure 3.8: EM Setup Layout (Momentum and Co-simulation can be selected from select type)

3.4 WPD Design, Simulation and Results:

The power divider is designed at 5GHz on the Rogers_RT_Duriod_5880 substrate which has an E_r of 2.2, thickness T = 0.762mm and tanD=0.0009. The transmission port has a characteristic impedance of 50Ω. The quarter wave T/L has the characteristic impedance of $\sqrt{2}Z_o$=70.7Ω. After carefully inserting all the values of substrate and design frequency, the length and width for corresponding impedances was found. It was made sure that during calculation of length and width of 70.7Ω transmission line, E_{eff} [2] in Figure 3.3 was set to 90^0 to calculate parameters of $\pi/4$ Transmission Line[3].

[2] In ADS Electrical length is given by E_{eff} .

[3] $E_{eff} = \beta l$, where $\beta = 2\pi/\lambda$. For $l = \lambda/4$ E_{eff} comes out to be $\pi/2$ i.e., 90^0.

3.4.1 Layout Design:

The layout design was created using MLIN, MTEE, and MSABND after obtaining the values of length and width from Linecalc. After connecting the components, the final circuit created in ADS layout is shown in **Figure 3.9**.

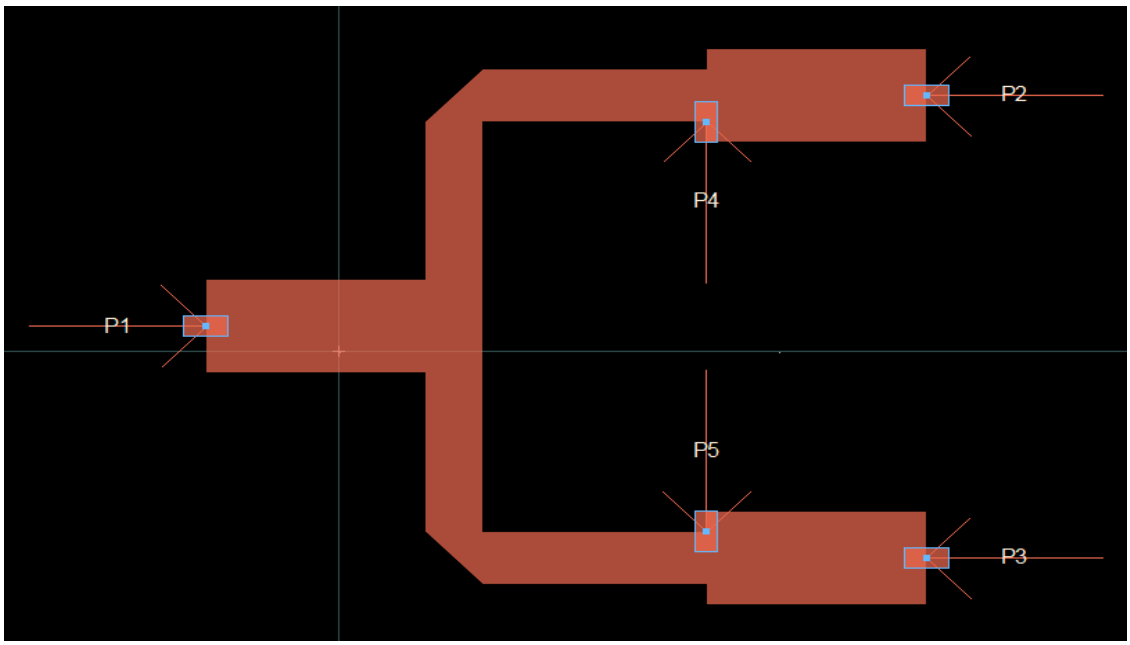


Figure 3.9: WPD Layout designed at 10GHz

For momentum simulation purposes, P4 and P5 are made as a differential port so that together they act as one port with a value equal to the isolation resistor. P4 and P5 were made as differential ports in the port editor as shown in **Figure 3.10**.

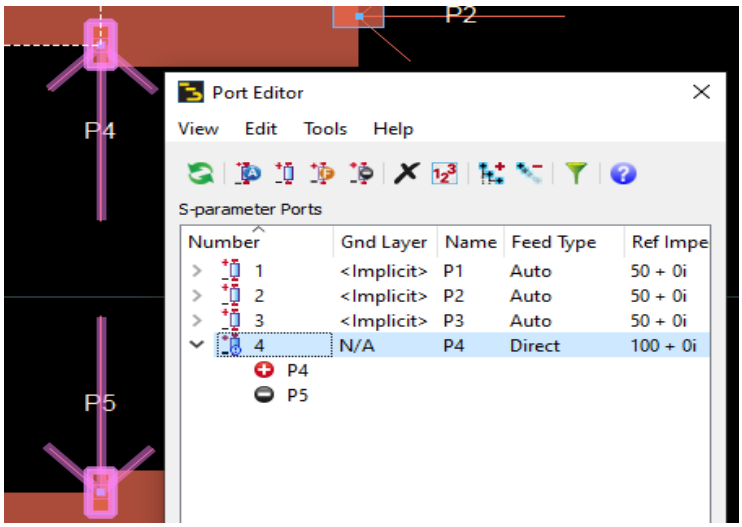


Figure 3.10: Port editor setup for differential ports

3.5 Simulation Results:

The designed circuit of the layout is simulated using both the momentum and cosimulation setups. In this section we focus on the momentum simulations

3.5.2 Momentum Setup Simulation Results:

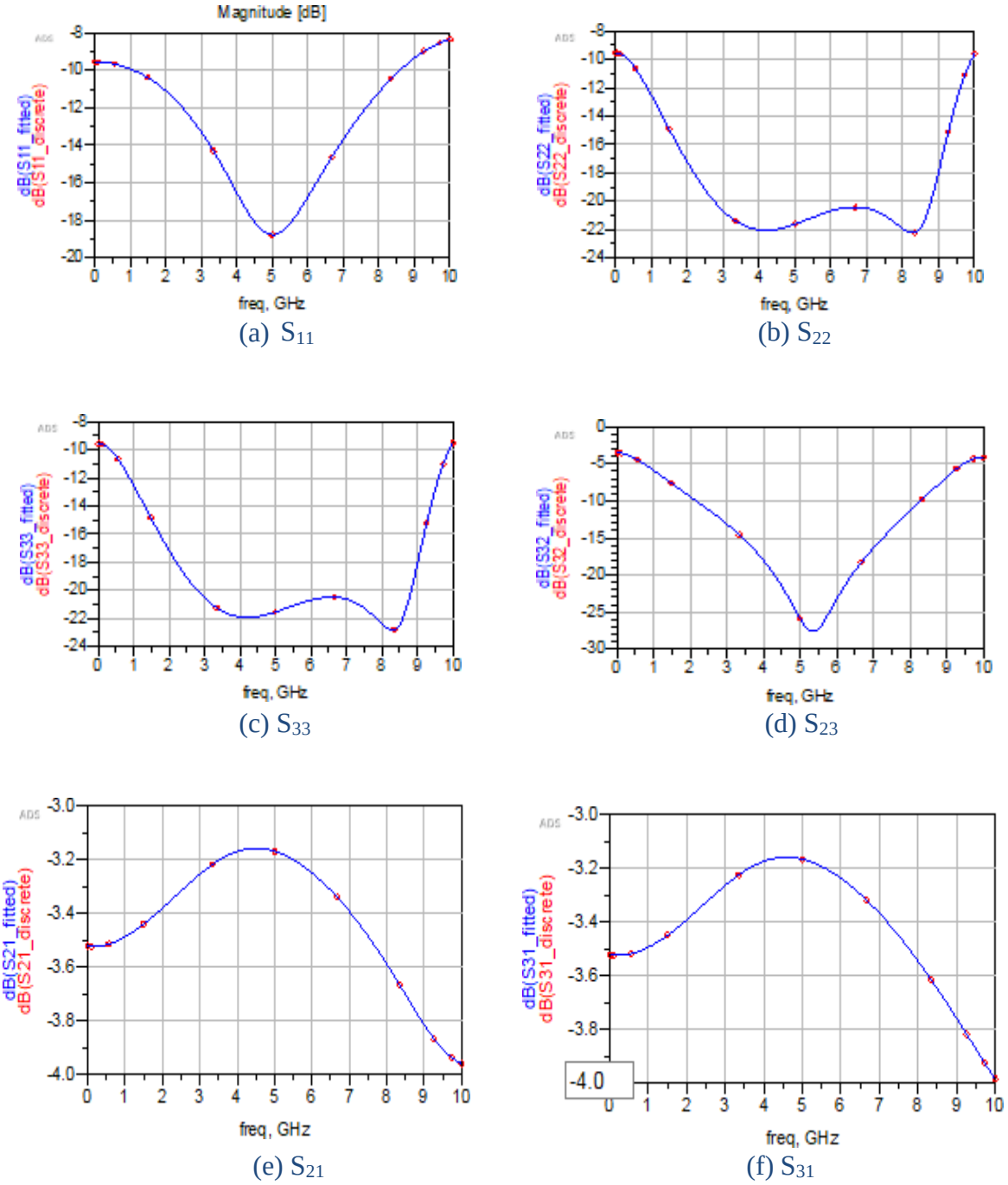


Figure 3.11: Momentum Simulation Results of each S parameter for WPD at 5GHz

3.5.2 Comments on Momentum Setup Simulation Results:

As it is seen from the above graphs of **Figure 3.11** the results are quite satisfactory because in practical cases, return loss(S_{11}) is acceptable if its value is closer to -15dB. In our case, it is evident from the graph (a), (b) and (c) of **Figure 3.11** that the S_{11}, S_{22}, and S_{33} are at roughly -22dB, -22dB and -19dB**,** respectively for the proposed WPD circuit**.** These results are promising because momentum simulation is considered to give more practical results than the cosimulation results.

For a WPD having the same power division ratio, the output power transmitted should be **-3dB (50% in linear scale)** so that both output ports have -3dB (50% power at the output). From the graphs (**e) and (f)** of **Figure 3.11 S_{21} and S_{31}** are at **-3.16 dB** respectively, which are close to the ideal behavior which is **- 3dB.**

For any microwave circuit, it is desired to have a higher value of isolation among the ports. For our case, the isolation among the port two and port three i.e., **S_{23}** is less than **-25dB** at 5GHz, as seen from **Figure 3.11** (d) which is a good value of isolation to achieve.

3.6 Cosimulation Setup Results:

For cosimulation setup, the EM_Cosim setup was selected from the EM setup layout as mentioned in Section 3.3.6. Then a schematic was created in which the symbol of the EM_Cosim was created. TermG is connected to the input (port 1) and the output ports (port 2 & 3) as shown in **Figure 3.12**.

The isolation resistor is connected between the port two and port three after λ/4 T/L. Then **S_Param simulator** from the basic component library is used to generate the S-parameters of the designed circuit. The **S_Param** block start and stop frequencies are set with a certain step size which plots S-parameters. The smaller the step size, the smoother the graph will be. A Cosimulation setup Schematic with all above steps is given in **Figure 3.12**:

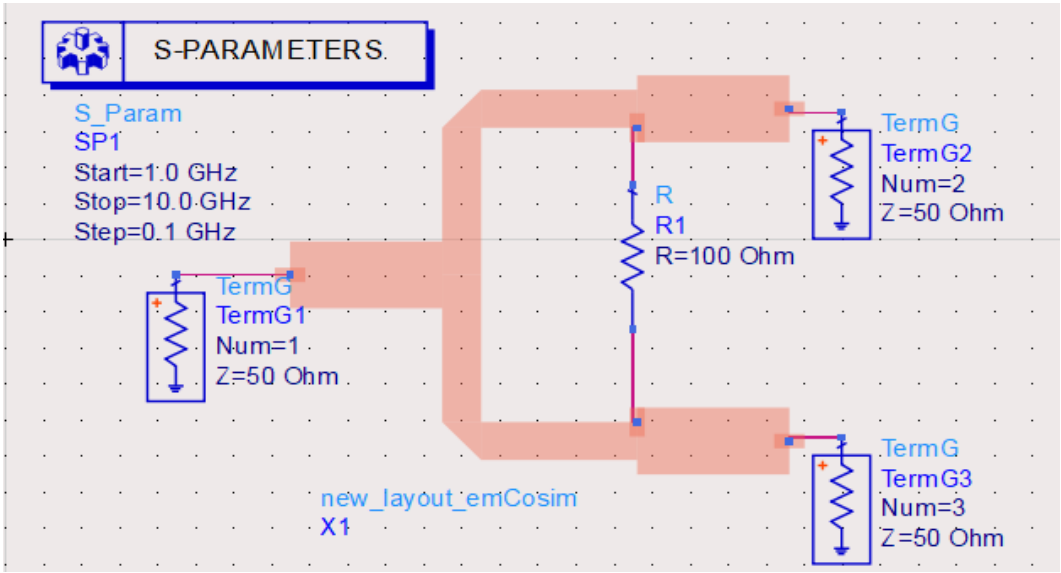
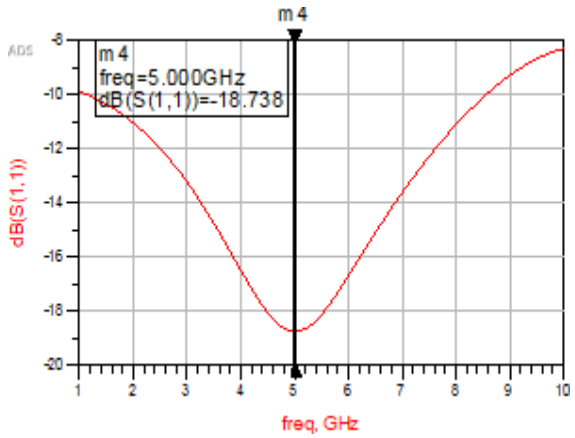
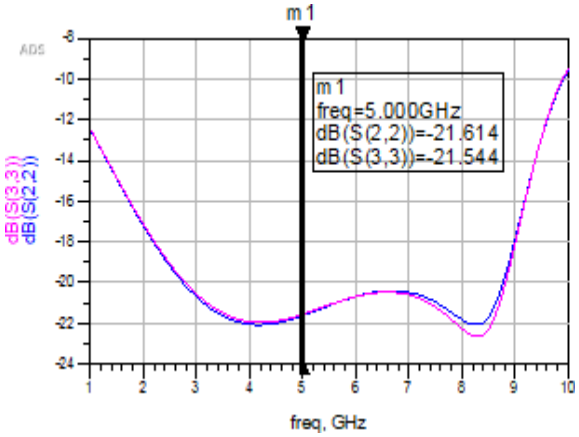


Figure 3.12: Cosimulation Setup Schematic for WPD at 5GHz

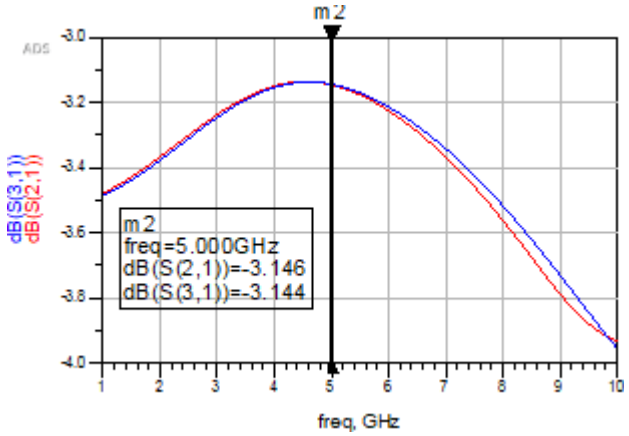
3.6.1 EM Cosimulation Results:



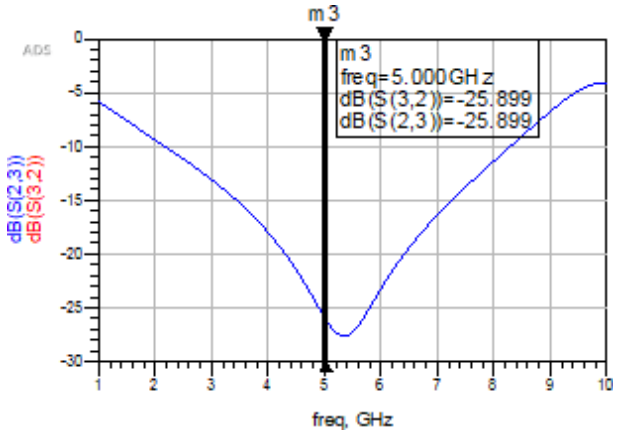
(a) S_{11}



(b) S_{22} & S_{33}



(c) S_{21} and S_{31}



(d) S_{23} and S_{32}

Figure 3.13: Cosimulation Setup Schematic Results of WPD at 5GHz

3.6.2 Comments on Cosimulation Results:

One can make following observations from the Cosimulation Setup Schematic Results:

- **Figure 3.13** (**a)** shows that S_{11} is **-18.7dB**
- **Figure 3.13 (b)** shows that both the S_{22} and S_{33} are **-21.614 dB** and **-21.544 dB,** respectively.
- **Figure 3.13 (c)** represents the parameters S_{21} and S_{31} which are **-3.146** and **-3.144 dB,** respectively.
- **Figure 3.13 (d)** gives the isolation of ports 2 and 3 which is **-25.889 dB.**

3.7 Comparison of Both Simulation Results:

Sections 3.5.1 and 3.6.1 clearly show that there is a very slight difference between momentum and cosimulation setup results.

All the parameters have equal values at the same frequency. The only difference is that the momentum simulations are considered more accurate than cosimulation setup simulation. The reason is that the momentum simulation is more practical than cosimulation setup as it includes the effects of coupling radiation etc. by use of Maxwell equations.

Chapter 4

Objective:

As discussed previously, the main objective of this project is to study negative group delay and fully understand it's working. For this we studied several research papers regarding this topic, and we focused on the following two papers,

1. O=O shaped microstrip line structure [16]
2. Power Divider topology along with coupled lines [18].

We designed, simulated, and fabricated both these circuits and our desired NGD and better S-parameters were achieved. The detailed analysis of both these circuits is given below.

4.1 O=O Shaped Low-Loss NGD Microstrip Circuit [16]:

The main purpose of this paper was to study how NGD is achieved in passive circuits. It consists of a simple power divider and a combiner which were connected using a coupled line. A block diagram for the given topology is given below:

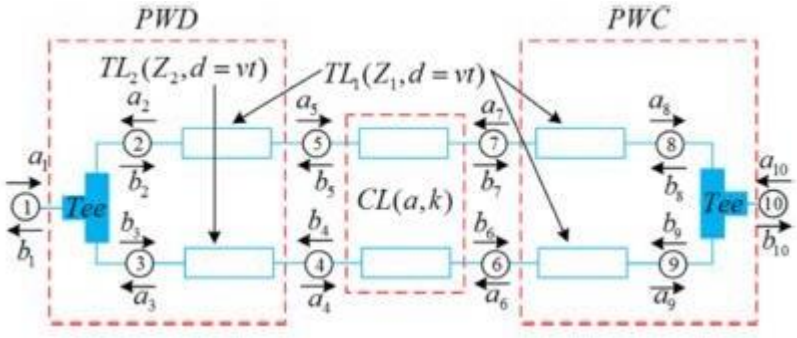


Figure 4.1: O=O shaped Circuit Diagram (taken from [16])

The above NGD circuit topology consists of Wilkinson Power divider (left side) and Wilkinson Power Combiner (right side). Both the divider and combiner are connect using parallel coupled lines. The power division of Wilkinson Power Divider is kept unequal.

In this paper the losses and the delay of coupled lines were studied and NGD was achieved using that. Parametric analysis was performed to find the effect of characteristic impedance of TLs and CL on NGD by changing the length and width of TL as well as spacing of coupled lines in Figure 4.1.

For simulation and fabrication, we used the same optimized dimensions that were already given in the paper.

4.1.1 Substrate Selection and Physical Dimensions:

The substrate selected for the implementation of the circuit in Figure 4.1 is FR-4 with the following parameters:

- ❖ Thickness (T) = 35 um
- ❖ Height (H)= 1.6mm
- ❖ Loss tangent (tanD) = 0.01

The center frequency for this circuit is kept at 1.2GHz

.

Physical Dimensions:

The dimensions are given in **Figure 4.2**.

Constituting element	Description	Value
TL_1	Length d	20 mm
	Width w	3 mm
	Characteristic impedance Z_1	50 Ω
	delay t	0.12 ns
TL_2	Width w_0	2.15 mm
	Characteristic impedance Z_2	60 Ω
CL	Length	20 mm
	Width w	3 mm
	Interspace	1 mm
	Coupling coefficient k	-14 dB
Tee_1	Length	6.5 mm
	Width w	3 mm
Tee_2	Length	7 mm
	Width w	3 mm
Access line	Length	7 mm
	Width w	3 mm

Figure 4.2: Physical Dimensions for O=O shaped circuit from Paper (taken from [16])

4.1.2 Layout Design:

The physical dimensions given above were used to construct the circuit on an ADS layout following the steps discussed in chapter 3 with great detail. The layout is given in **Figure 4.3**.

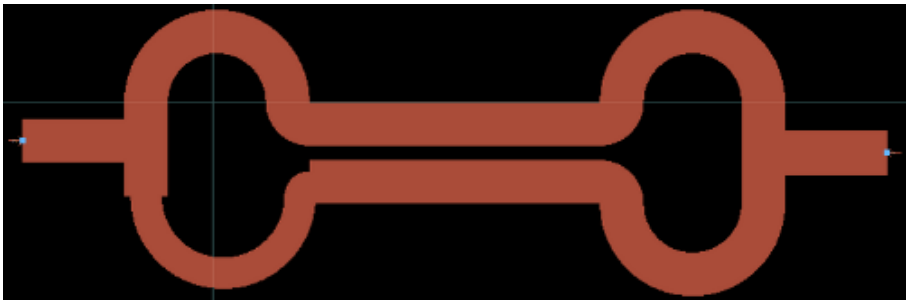


Figure 4.3: Layout Design for O=O shaped NGD Microstrip Circuit

4.1.3 Simulation Results:

The simulation results are given in **Figure 4.4**. The results are somewhat shifted from the original design frequency of 1.2 GHz.

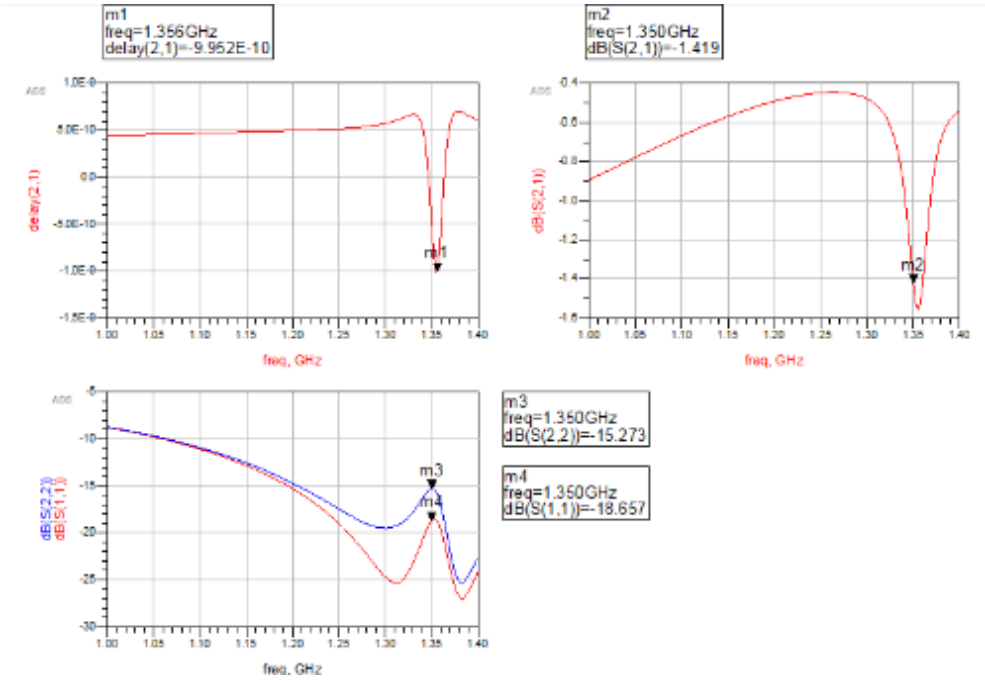


Figure 4.4: Simulation Results of O=O shaped Microstrip Circuit

The above simulation results show that the

- NGD = -0.995 ns
- S_{11} = -18.657 dB
- S_{12} = S_{21} = -1.419 dB
- S_{22} = -15.273 dB

4.1.4 Measured Results:

The fabricated circuit was tested on Agilent E8363b Vector Network Analyzer (VNA) and data files were exported to MATLAB, the procedure for which will be discussed more in chapter 5. The results are plotted in **Figure 4.5**.

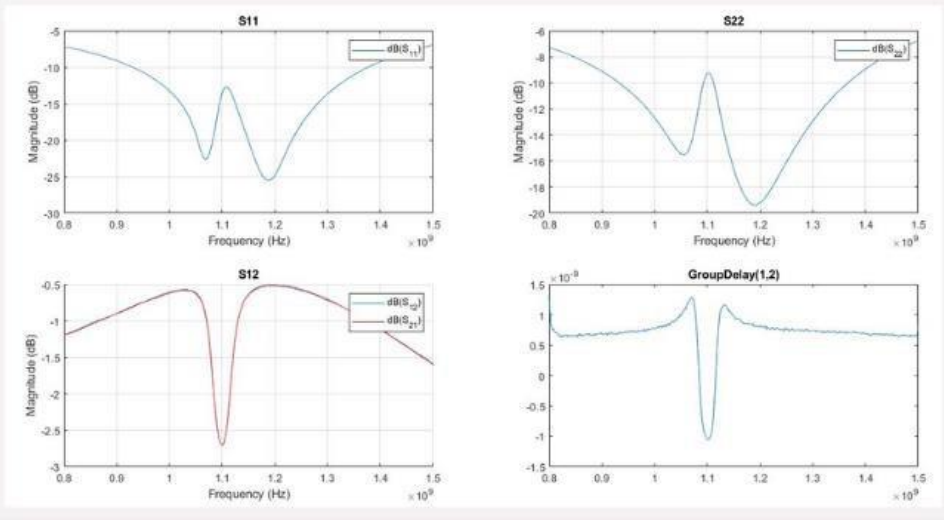


Figure 4.5: Measured Results of O=O shaped Microstrip Circuit

It can be seen from the above plots that the measured results are:

- NGD = -0.97ns
- S_{11} = -16 dB
- S_{12} = S_{21} = -2.6 dB
- S_{22} = -10 dB

4.1.5 Comments on Simulation and Measured Results:

Sections 4.1.3 and 4.1.4 show both values of parameters for simulation results and measured results. The results were measured using Vector Network Analyzer(Model: Agilent E8363B) . The measured results of S_{11} and S_{22}, return loss, are -10dB and -9dB, respectively. These results are relatively acceptable as they are in acceptable range of less than then -10dB. The insertion loss, S_{12}, for measured results is -2.7dB and for simulated results it is, $S_{12=}$ -1.41dB. The insertion loss, S_{12},is slightly higher for measured result. However, The center frequency is shifted about 0.25GHz for simulated results. So, it can be said that our first attempt to achieve NGD by replicating a circuit was successful.

4.2 Power Divider [PWD] with NGD Characteristics:

As discussed in the literature review, there are many different methods to achieve NGD. At the initial stages, the major purpose was to achieve NGD but there was a significant disadvantage of mismatching. To avoid mismatching, many techniques were discovered to achieve NGD while maintaining the matching at the same time. In this and the following section, NGD Power Divider with coupled lines as reported by [18] provide better matching in the circuit. The circuit diagram of the PWD is given below:

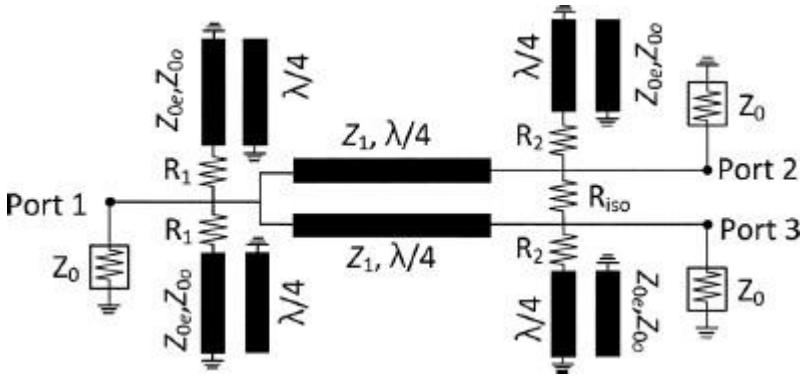


Figure 4.6: PWD with NGD characteristics circuit diagram (taken from [18])

Resistors along with coupled lines introduce NGD and also provide matching (as explained by Girdhari Chaudhary in [18]).

4.2.1 How NGD is achieved in the Circuit:

The circuit consists of λ/4 T/L, coupled lines and resistors. First, we will see the mathematical analysis to gain the understanding that how the different components in the circuit diagram, of [18], are going to affect the NGD. The mathematical equations after the even and odd mode analysis, as explained in [18], is given below:

$$\tau_{21}|_{f=f_0} = \tau_{31}|_{f=f_0} = -\frac{3}{4f_0}\left\{\frac{Z_c}{2RC_{eff}} - \frac{\begin{bmatrix}(R+Z_0)(2RC_{eff}Z_0 + Z_1Z_c)\\ Z_1 + 2RZ_0^2Z_c\end{bmatrix}}{C_{eff}\begin{bmatrix}2R(2Z_0+R)Z_1^2\\ +2Z_0^2(Z_1^2+2R^2)\end{bmatrix}}\right\}, \quad (1)$$

From (1) it is evident that the NGD is dependent on R (resistor values), Zo is the characteristic impedance of the input and output T/L, Z_c is the equivalent characteristic impedance of CL (Coupled Lines), C_{eff} is the coupling coefficient of the coupled lines, Z_1 is the impedance the λ/4 T/L and f_o which is the design frequency. The relation of Z_c with C_{eff} is given by (2),

$$Z_c = \frac{2Z_{0e}}{\frac{Z_{0e}}{Z_{0o}} - 1} = Z_{0e}\frac{1 - C_{eff}}{C_{eff}} = Z_{0o}\frac{1 + C_{eff}}{C_{eff}} \quad (2)$$

The NGD is achieved by introducing losses in the circuit. In the PWD circuit under consideration here resistors are being used for introducing losses in the circuit to produce NGD. The models of CL (Coupled Lines) are used to improve matching in the circuit. Whereas isolation among Port 2 and 3 in circuit of **Figure 4.6** is achieved by selecting the appropriate value of isolation resister R_{iso}. The resistors R_1 and R_2 also influence Z_1 as according to the mathematical model Z_1 is dependent on the values of R_1 and R_2 resistors. The relation of Z_1 with respect to resistors according to even and odd mode analysis for circuit is given below.

$$R_1 = 2R_2$$

$$Z_1 = \sqrt{\frac{2R_1R_2Z_0^2}{(R_1 - 2R_2)Z_0 + R_1R_2 - 2Z_0^2}} \quad (3)$$

The above equation, (3), represents that the Power Divider is not behaving as a typical Wilkinson Power Divider. Because for simple Wilkinson Power Divider Z_1 is dependent only on Z_o and it should be $\sqrt{2}Zo$ whereas in this case it is determined by the relation given above which is dependent on both Z_o and resistors (R_1 & R_2). Next, we are going to see how all these little parameters will affect the NGD.

4.3 Implementing the Mathematical Model:

To ease the calculations and to avoid repeating the steps of the procedure in [18]. We coded the whole procedure into the following MATLAB function.

```
function [R1,R2,Riso,Z1,NGD]= NGD_calculation(R,Z,Ceff,Zc,f)
% R is a vector containing Resistor value
% Z is 50 ohms
% Ceff is Coupling Coefficient in dBs
% Zc is the Equivalent characteristic impedence
% f is the frequency
% Change the coupling coefficient from dBs to linear scale
Ceff=10^(Ceff/20);
R2=R;
R1=2.*R2;
% Calculate Z1 using equation 2b
Z1=sqrt((2.*R1.*R2.*(Z^2))./((R1-2.*R2).*Z+R1.*R2-2.*(Z^2)));
% Calculate Riso using equation 2c
Riso=((R1+2.*Z).*Z1.*Z1)./(Z.*R1);
%Calculate NGD using equation 3b
A=(R+Z).*(2.*R.*Ceff.*Z+Z1.*Zc).*Z1+2.*R.*Z.*Z.*Zc;
B=Ceff.*(2.*R.*(2.*Z+R).*Z1.*Z1+2.*Z.*Z.*(Z1.*Z1+2.*R.*R));
C=Zc./(2.*R.*Ceff);
NGD=(-3/(4*f)).*(C-A./B);
```

Figure 4.7: MATLAB Code of the equation 1

To see how NGD is changed with respect to different parameters, we take help of the function shown in **Figure 4.7**. For microwave circuits characteristic impedance is generally set to 50 ohms therefore we set Z = 50 for all cases. The center frequency is kept at 1.8 GHz in all variations of code. The main goal is to input these parameters for FR-4 (ε_r = 4.6 and TanD=0.01) for two different heights (h=40 mils and h = 31 mils). For the cases discussed in sections 4.3.1 and 4.3.2, the substrate height is set to 40 mils. Same procedure is repeated for the power divider of substrate height of 31 mils.

4.3.1 Effect of Resistance on NGD:

We can vary R from 0 to some high value (say R=1k ohms), but for values R<Z, Z_1 comes out to be a complex number having both real and imaginary components. Whereas, for the value R=Z, Z_1 comes out to be infinite. Therefore, we varied the resistance value (R) from 55 to 1000 and passed the following parameters of Figure 4.8 to the function and plotted the graph of NGD vs Resistance values. As discussed earlier, the code in **Figure 4.8** runs the function named NGD_Calculation when different circuit values are fed as functions parameters to it.

```
R=55:5:1000;
f=1.8e9;
Z=50;
Zc=400;
Ceff=-20;
[R1,R2,Riso,Z1,NGD]=NGD_calculation(R,Z,Ceff,Zc,f);
plot(R,NGD);
grid on;
title('Achievable NGD Vs Resistance');
xlabel('Resistance R (Ohms)');
ylabel('Group Delay (ns)');
```

Figure 4.8: MATLAB Code for passing parameter to the function

When the code of **Figure 4.8** is run graph in **Figure 4.9** is plotted. It shows how NGD varies with respect to variation in Resistance (R).

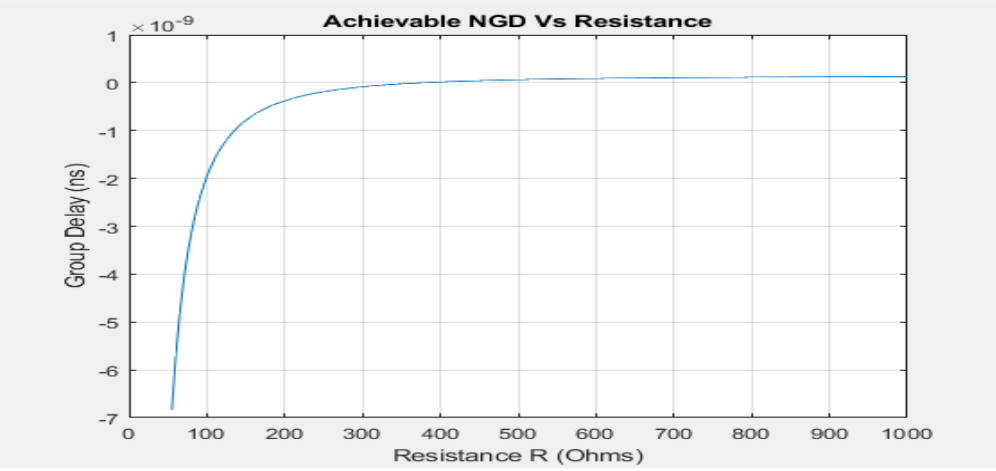


Figure 4.9: Achievable NGD Vs Resistance Curve

From **Figure 4.9** it can be seen that at low value of R (R ≈ 50 Ohms) one can achieve maximum NGD, but it comes with a drawback as explained in the following. E.g. if we choose R =55 Ω, Z_1 comes out to be 169.733 Ω at frequency 1.8 GHz for FR-4 substrate of height 31 mils. For Z_1 = 169.733 Ω, width of the transmission line is 0.043 mm as shown in **Figure 4.10**.

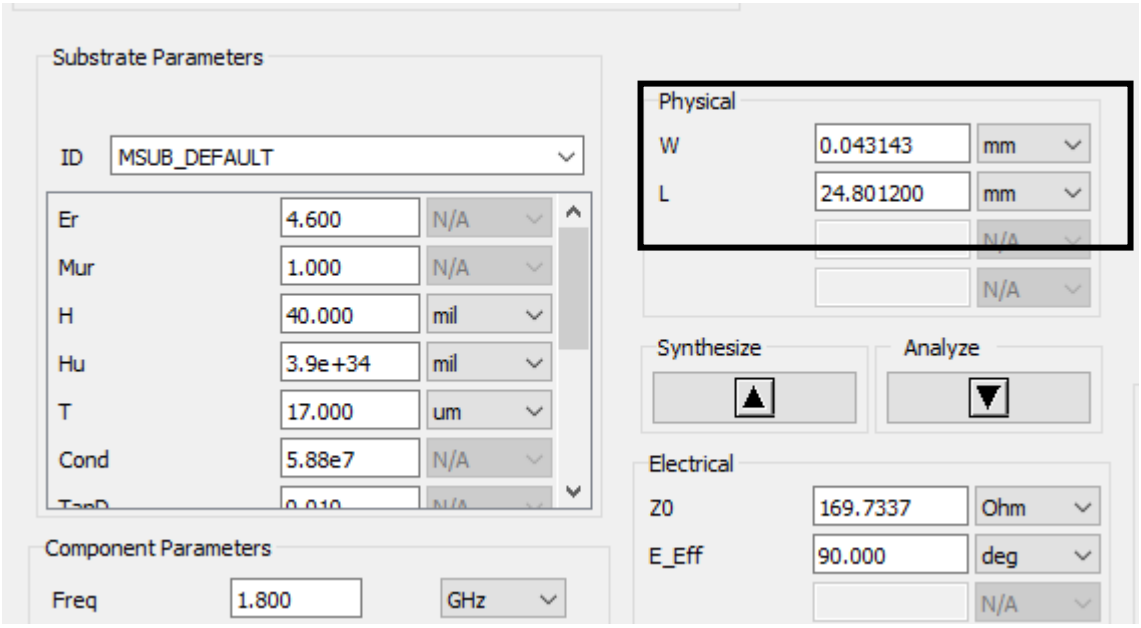


Figure 4.10: Linecalc results for width of T/L for Z_1 169.733 Ω and R=55 Ohms

Regardless of the achievable NGD for R=50 Ohms, the width for such a value of characteristic impedance (Z_1) is not realizable, as it so small and one has to solder SMD resistors on this line, therefore we must compromise on the maximum achievable NGD so that we can have a physically realizable circuit. In this regard we chose the value of R to be 100 Ohms where Z_1 comes out to be 81.64 Ohms, which gives a somewhat realistic width as shown in **Figure 4.11**. Using the code in **Figure 4.7** the theoretical achievable NGD comes out to be -2.9984 ns.

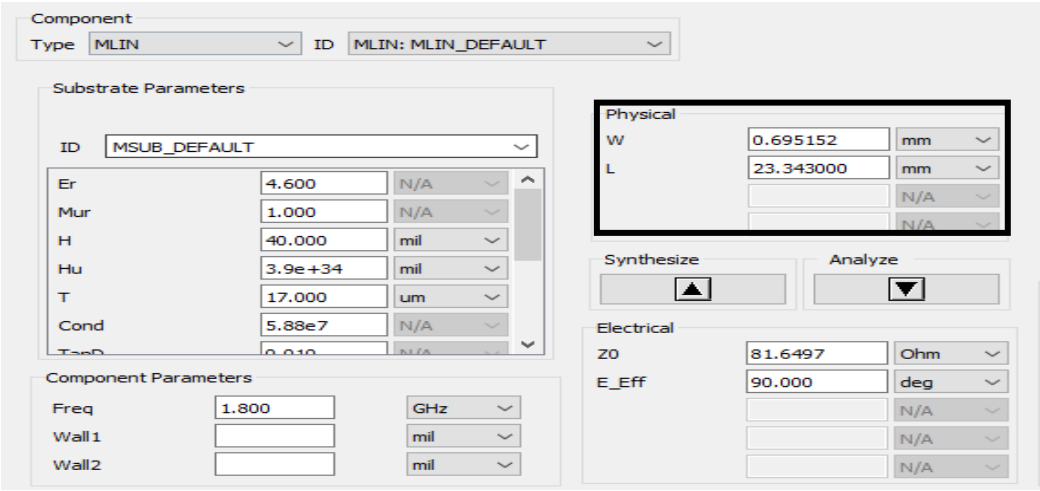


Figure 4.11: Linecalc results when R=100 Ohms

The width is 0.695152 mm which is realizable using the available fabrication techniques and one can easily solder SMD components on it.

4.3.2 Effect of C_{eff} and Z_c on NGD:

Using the following code, we vary the Equivalent Characteristic impedance (Z_c) from Z_c= 10 ohms to Z_c = 1000 ohms while fixing R = 100 ohms, because of the reason discussed in the section 4.3.1.

```
R=100;
Zc=10:10:1000;
[R1_1,R2_1,Riso_1,Z1_1,NGD_1]=NGD_calculation(R,Z,Ceff,Zc,f);
figure;
grid on;
plot(Zc,NGD_1);
title('Achievable NGD Vs Eq Characteristic Impedence (Zc)');
xlabel('Characteristic Impedence (Zc) in Ohms');
ylabel('Group Delay (ns)');
```

Figure 4.12: MATLAB Code 4-3

The relationship between Zc and NGD is plotted in **Figure 4.13**

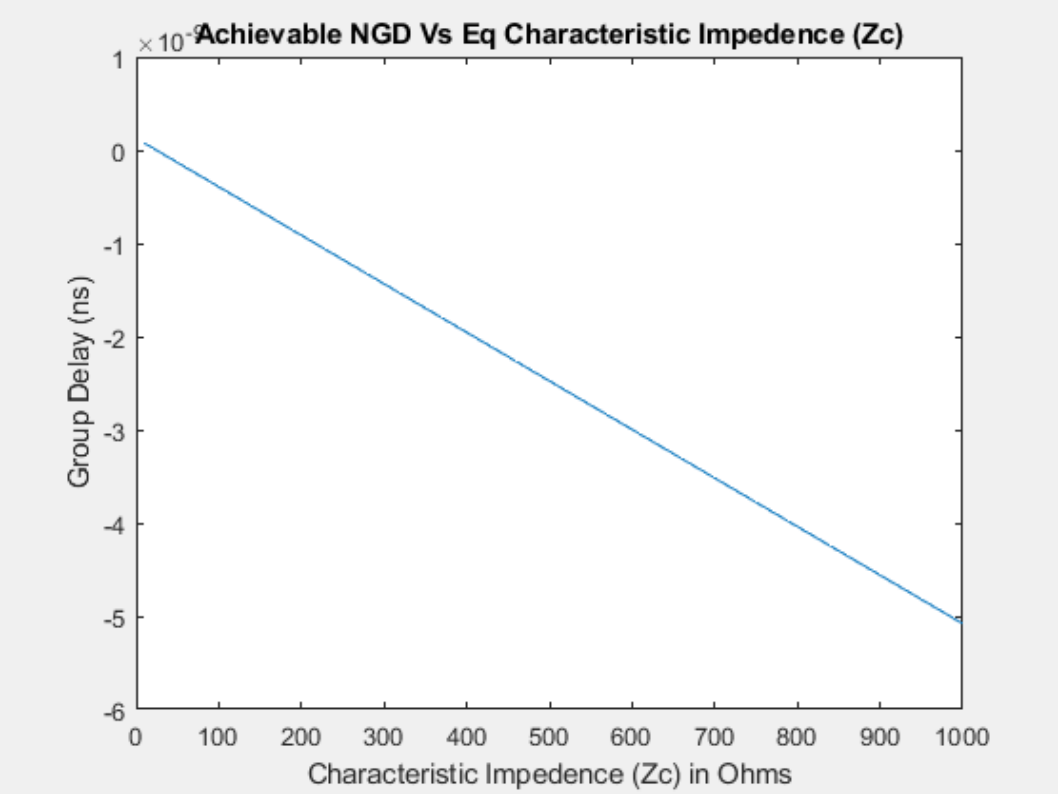


Figure 4.13: Achievable NGD Vs Characteristic Impedance (Zc)

In Addition to the above code of **Figure 4.12**, we also want to see how NGD varies by varying C_{eff}, which is changed from 0 to -100 dB using the following code of **Figure 4.14**.

```
Ceff=0:-5:-100;
R=100;
Zc=40;
[R1_2,R2_2,Riso_2,Z1_2,NGD_2]=NGD_calculation(R,Z,Ceff,Zc,f);
figure;
grid on;
plot(Ceff,NGD_2);
title('Achievable NGD Vs Coupling Coefficient (Ceff)');
xlabel('Coupling Coefficient (Ceff) in dBs');
ylabel('Group Delay (ns)');
```

Figure 4.14: MATLAB Code 4-4

The graph of **Figure 4.15** shows the Variation of NGD with respect to Change in Coupling Coefficient.

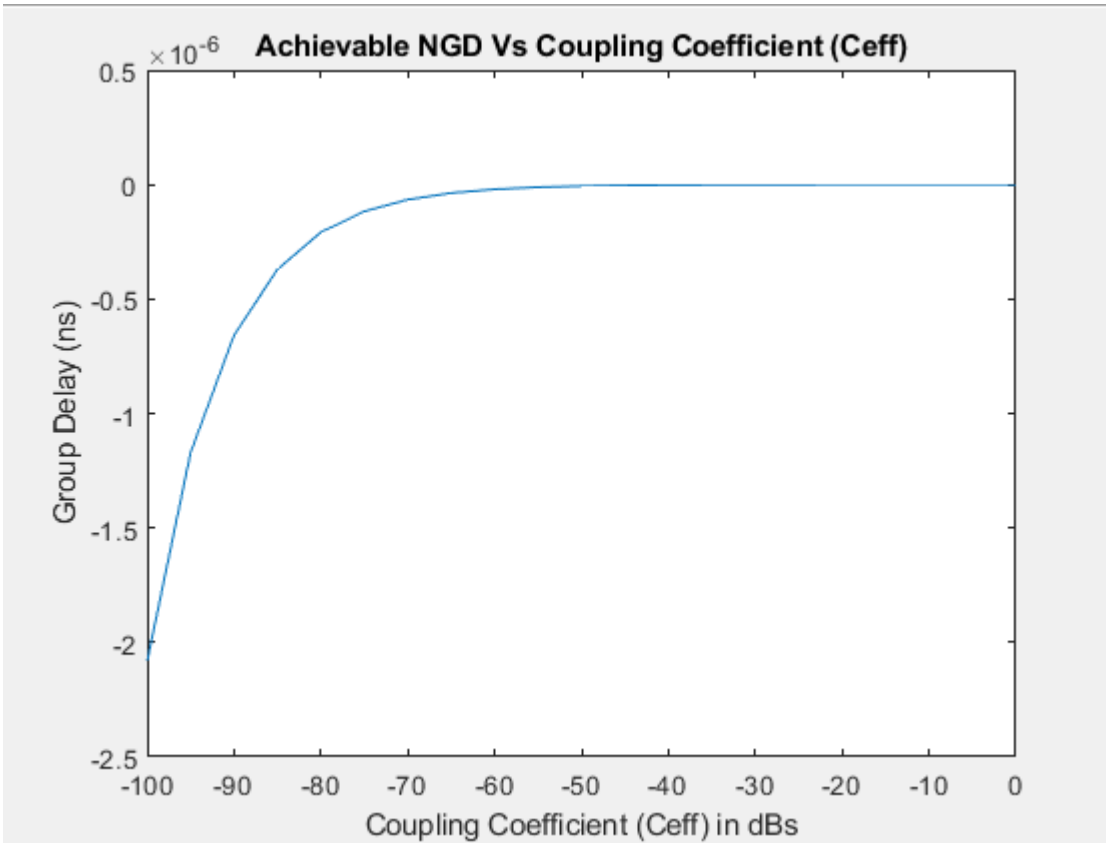


Figure 4.15: Achievable NGD Vs Coupling Coefficient

It shows that when coupling coefficient is less, we can achieve more NGD and from **Figure 4.13** we can see that, the greater the value of Z_c the greater the value of NGD can be achieved. The values of even mode impedance (Z_{even}) and odd mode impedance (Z_{odd}) can be calculated using (2). When the values of Z_{even} and Z_{odd} are used in line calc, circuit physical parameter become much greater to fit in the circuit with respect to other circuit components, as shown in **Figure 4.16**.

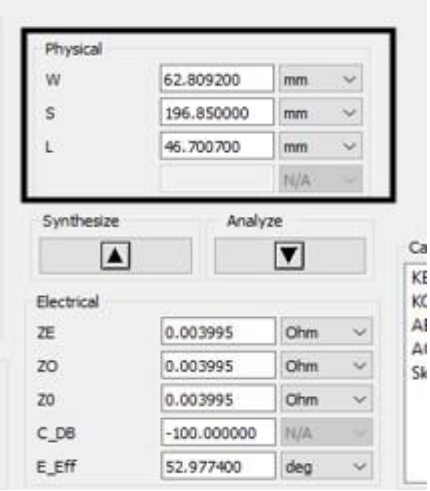


Figure 4.16: Linecalc Results for Zc=600 Ohms and Ceff=-100 dB

Therefore, we compromised and the values were changed to Z_c = 400 and C_{eff} = -20 degrees. Consequently, the calculated parameters of the coupled lines are w = 2.557990, s = 1.204800 and L = 22.189100 as shown in **Figure 4.17**.

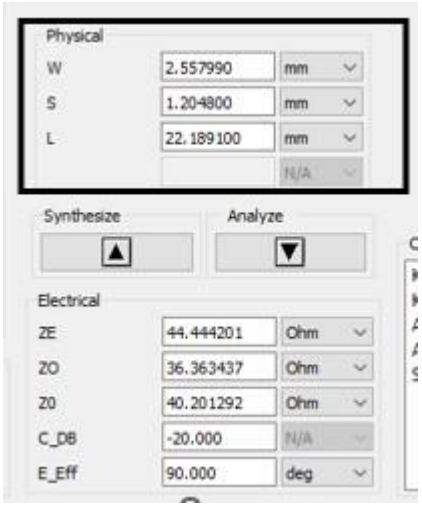


Figure 4.17: Linecalc Results for Zc=600 Ohms and Ceff=-20 dB

4.4 Circuit Implementation on ADS:

After studying the relationship between different parameters affecting the NGD, following parameters were analyzed.

Z= 50 Ohms, f = 1.8 GHz, R =100 Ohms, Z_c=600 ohms, C_{eff}=-20 dB

When these parameters are fed to the NGD_calculation function, using the following code.

```
R=100;
Zc=600;
f=1.8e9;
Z=50;
Ceff=-20;
[R1,R2,Riso,Z1,NGD]=NGD_calculation(R,Z,Ceff,Zc,f);
display (R1)
display (R2)
display (Riso)
display (Z1)
display (NGD)
```

We get the following results

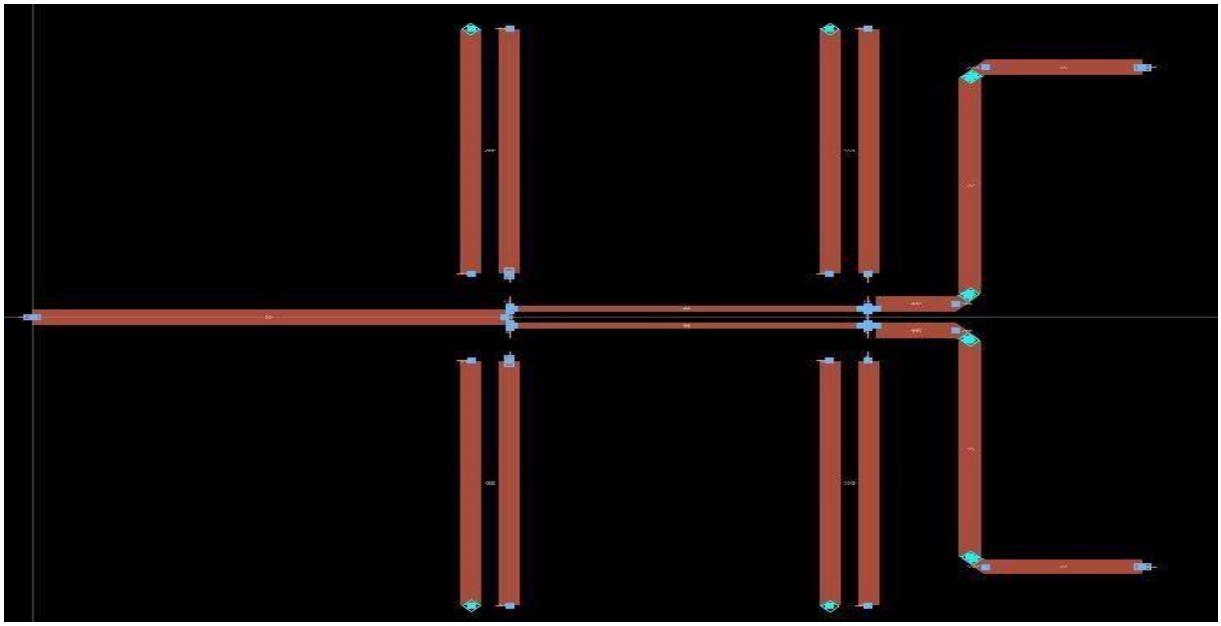
```
R1 =

   200


R2 =

   100


Riso =

  200.0000


Z1 =

   81.6497


NGD =

  -2.9974e-09
```

Figure 4.18: MATLAB Code Returned Values

These are the theoretically achievable results. Maximum NGD that can be achieved using theoretical calculation by (1) is -2.9984 ns.

4.4.1 Using Linecalc Values:

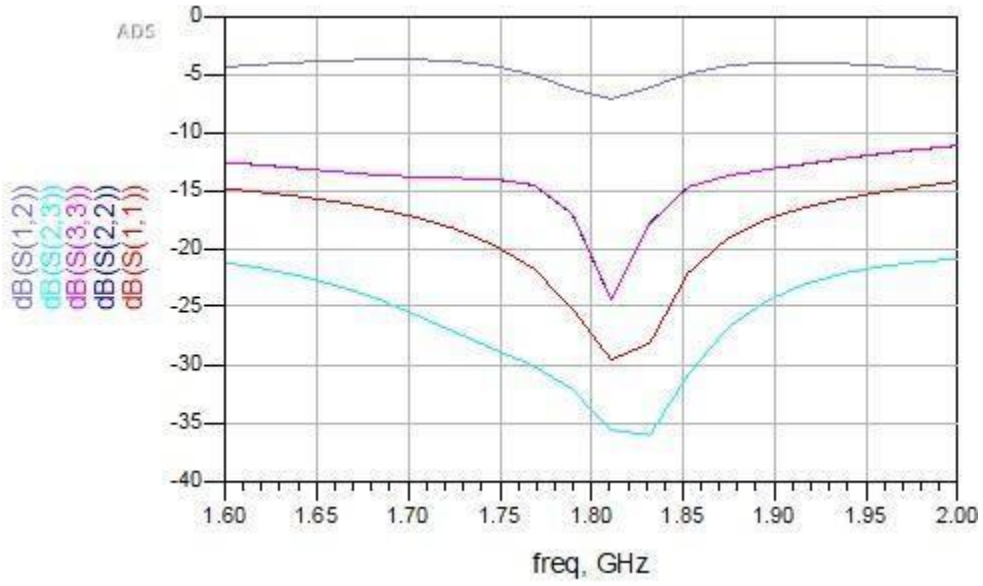
Using the values obtained in the previous section 4.4, we feed the values to the Linecalc and obtain physical dimensions of the microstrip transmission lines and coupled lines as shown in **Figure 4.11** and **Figure 4.19** for Z= 50 ohms. Then using these values and repeating the procedure as discussed in chapter 3, we get the layout of the circuit in ADS as shown in **Figure 4.19 (a)**.



(a)

(b)

Figure 4.19 (b) gives the group delay of the simulated circuit consisting of the components whose values were found using the calculated result of section 4.3. The group delay is equal to -0.6 ns which is not equal to the one found using calculation.



(c)

Figure 4.19 Schematic and Simulation (a) Layout of power divider circuit on 40 mils substrate using Linecalc values. (b) Group Delay. (c) S- Parameters

At the same time, the matching of the circuit was good, and were below -20 dB at center frequency, as depicted in **Figure 19 (c)**.

4.5 Parametric Sweep:

To further enhance the group delay characteristics of the circuit, we do the parametric sweep of different components in the circuit.

4.5.1 Parametric Sweep of Coupled Lines:

First, we apply the parametric sweep on the coupled lines as given in below mentioned steps:

- Create Parameters in layout from EM -> Component -> Parameters as shown in **Figure 4.20**.

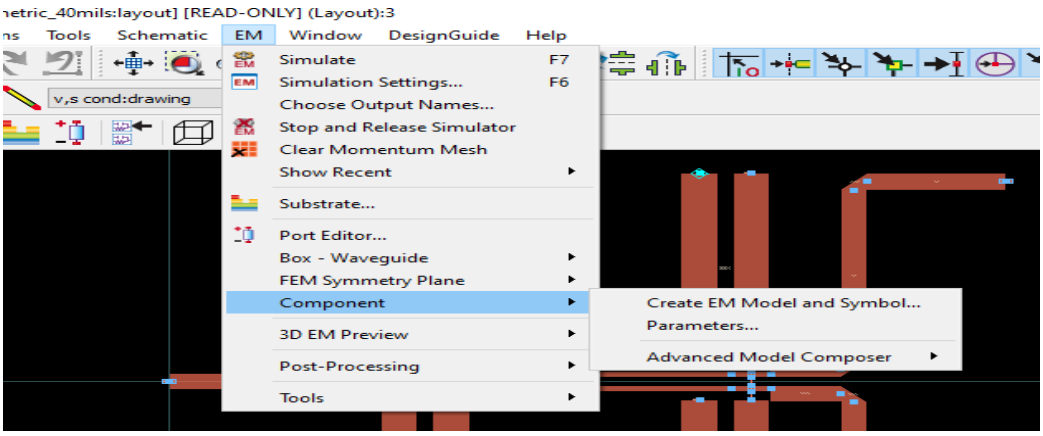


Figure 4.20 layout option to open EM model parameters

❖ Define the default parameters of w (width) and s (separation) for coupled lines.

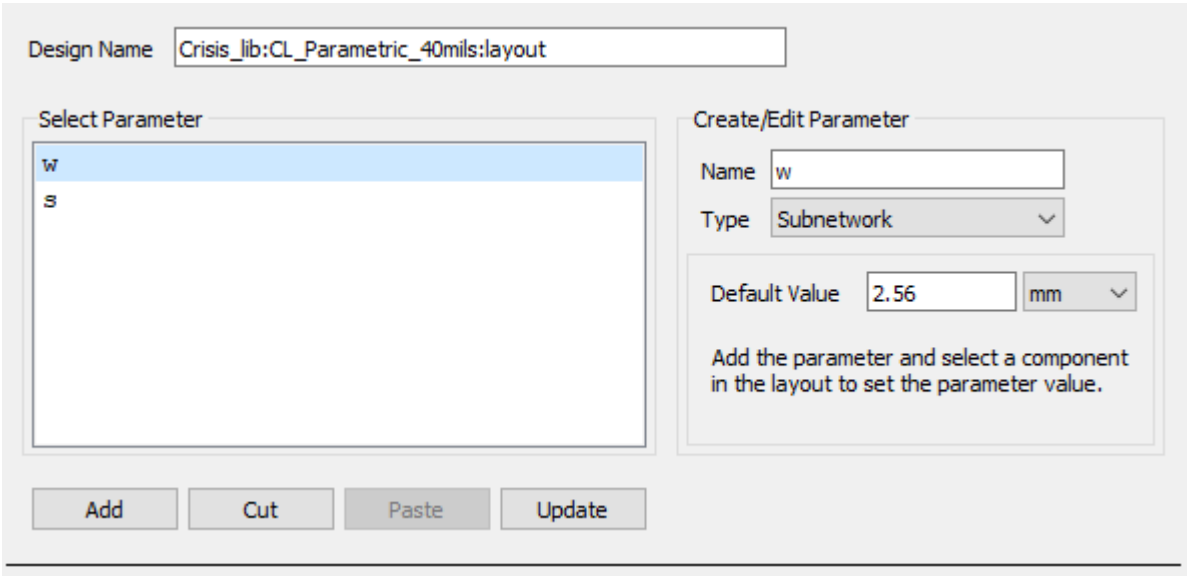


Figure 4.21 Setting for EM model parameters menu

❖ Insert these parameters in the properties of coupled lines as shown in **Figure 4.22**.

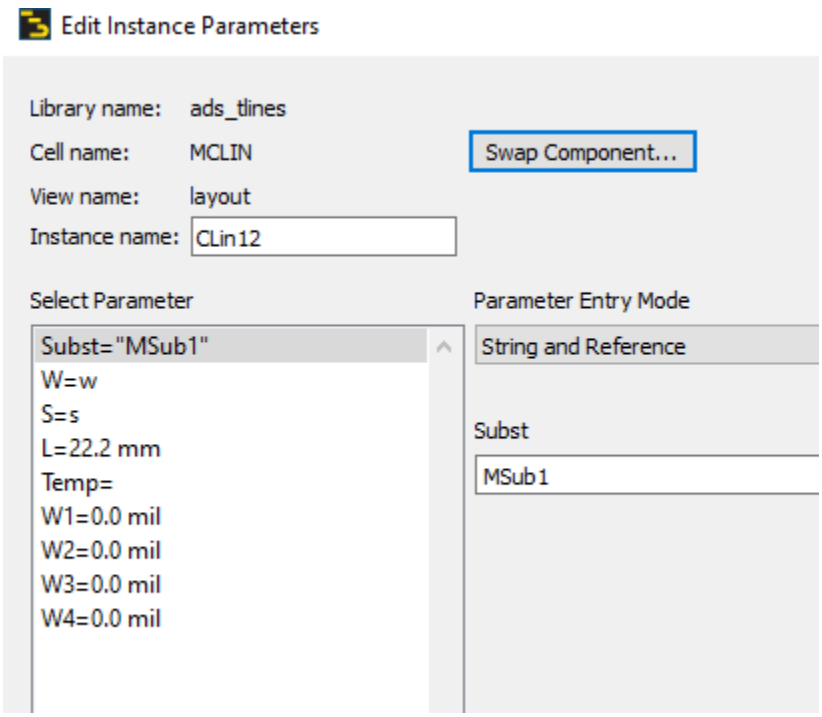


Figure 4.22 Setting for properties of Coupled lines

❖ Then simulate the circuit using EM co-simulation and make a symbol and EM setup of it, to use in Layout. Import the symbol of layout in the schematic as shown in **Figure 4.23**, the created parameters will be on the left bottom side of the imported symbol.

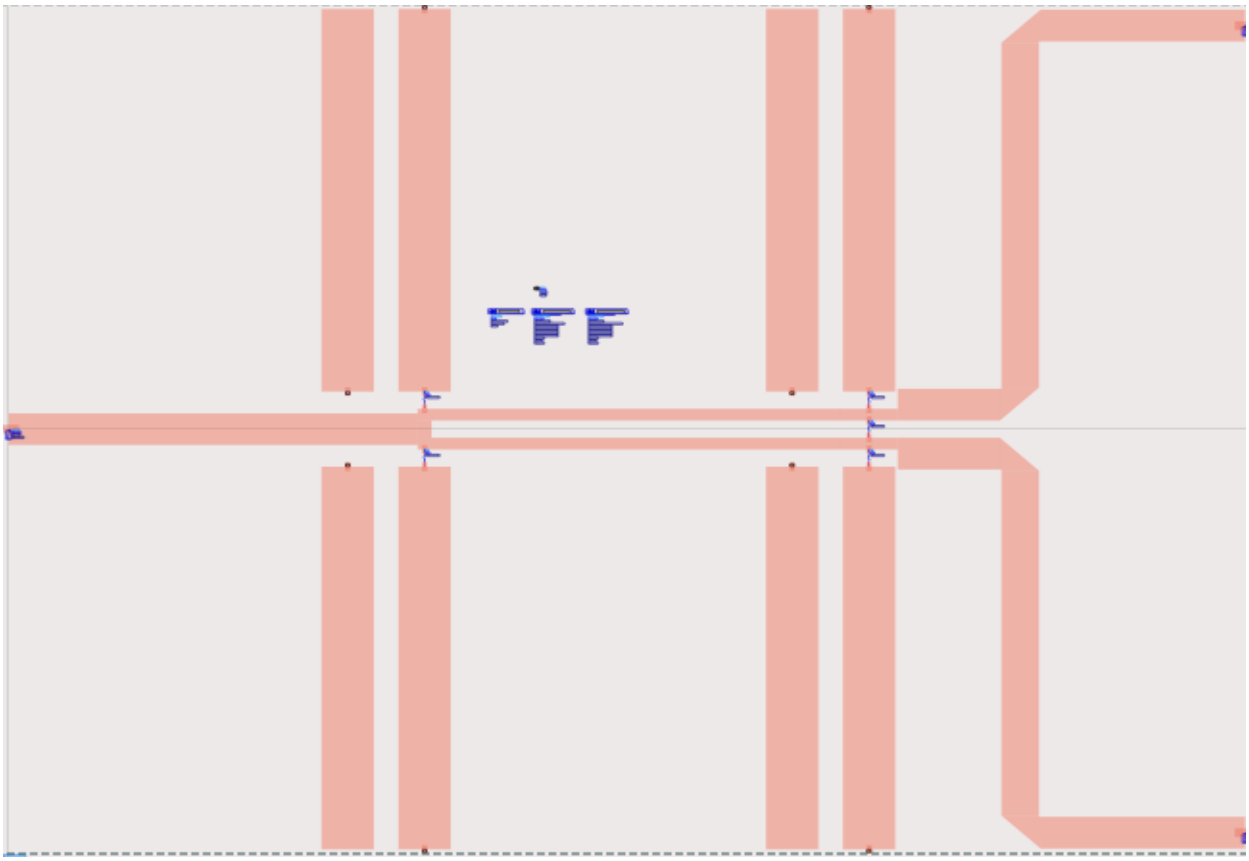


Figure 4.23: Schematic Setup for Parametric Sweep Circuit

❖ Go to insert -> var to define two variables w and s, both unitless, and initialize them with the values from which you want to start the parametric simulation as shown in **Figure 4.24**.

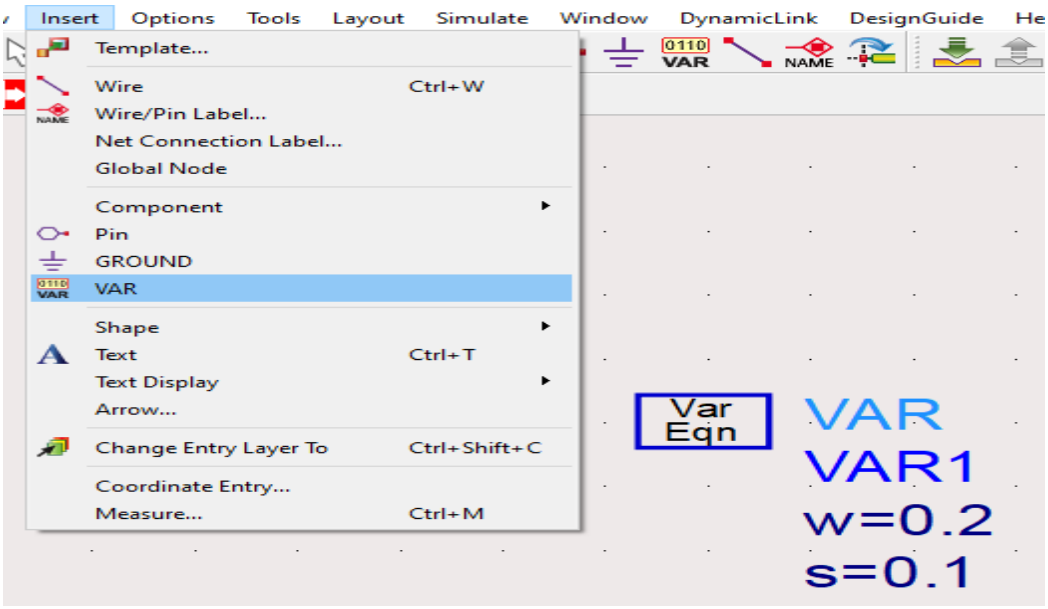


Figure 4.24: Variable setup in schematic view

❖ Insert these variables as the values of the parameters in lower left corner of the symbol as shown in **Figure 4.25**.

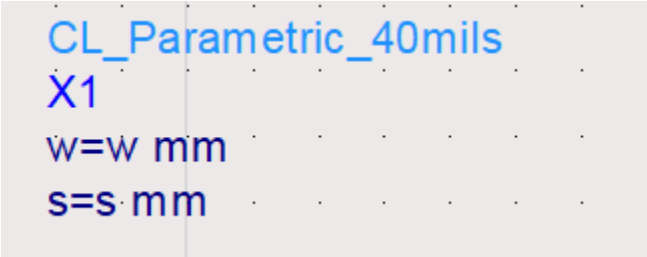


Figure 4.25: Changing parameters of symbol to variables

❖ Now setup the parametric sweep controller by mentioning the start, stop, and step of the variable and the simulation you want to sweep over i.e., S – Parameter controller as shown in **Figure 4.25**.

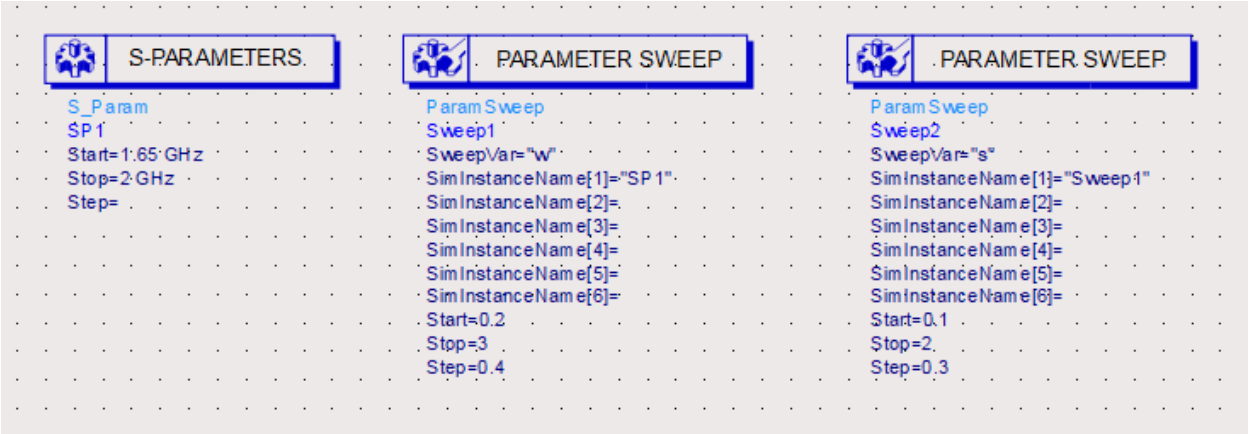


Figure 4.26: Parametric sweep Setup in the schematic view

❖ After running doing the parametric simulation of S parameters along with the group delay, we get the result in **Figure 4.27** with red line representing the chosen values of separation s and width w of the coupled lines

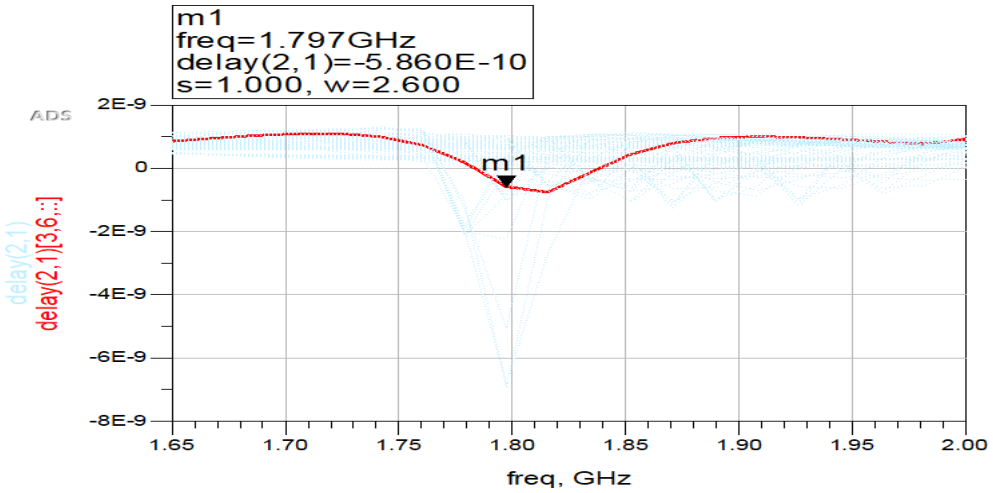


Figure 4.27: Group Delay for symbol circuit with Parametric Sweep

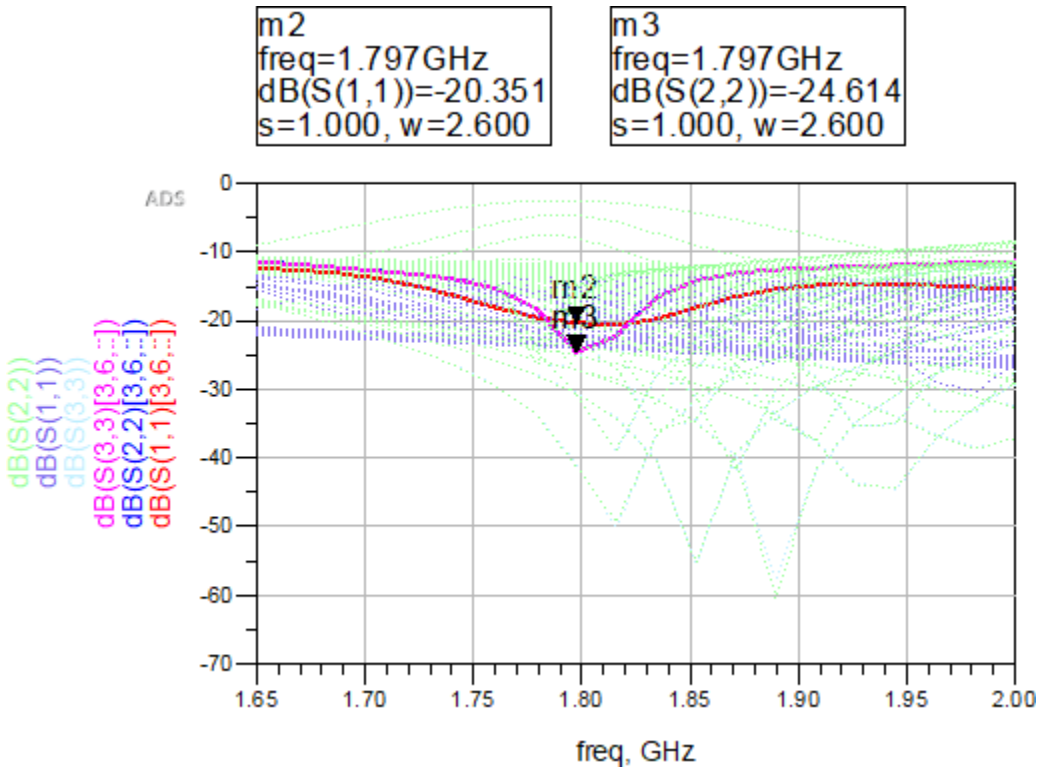


Figure 4.28: S parameter for circuit with Parametric Sweep

The dotted lines in **Figure 4.27** and **Figure 4.28** represent all the simulation results of the group delay and S parameters respectively, whereas the solid line represents the values we chose to enhance the performance of the circuit to have better matching and negative group delay. We chose the values of separation s= 1 mm and width w = 2.6 mm of coupled lines, because for all other values although the NGD was improved, the matching suffered a lot. As we will later see, integration of these updated values along with updated values of other parameters collectively improved the overall characteristics of the circuit.

- ❖ We update our layout according to the chosen w and s values.

4.5.2 Parametric Sweep on Z_1 Transmission line:

Now we repeat the same steps as discussed in the previous section 4.5.1 to sweep over the width and length of the transmission line with impedance Z_1, parameters w and l are the width and length of the transmission line, respectively. We used L_Gap_h as another parameter for the mgap (microstrip gap) component to make sure that the coupled lines move in the same manner as the length of the transmission line changes. After doing the parametric sweep of these variables we get the result as depicted in **Figure 4.29** and **Figure 4.30**.

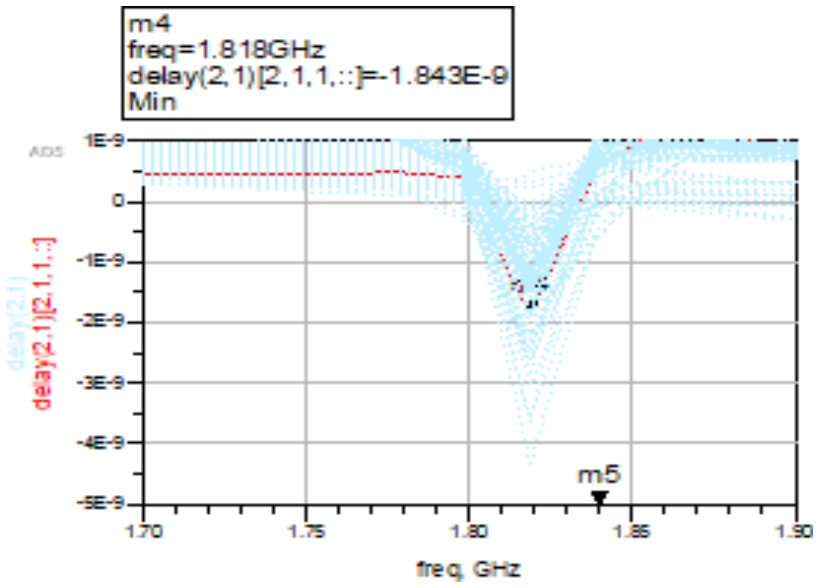


Figure 4.29: Group Delay for circuit with Parametric Sweep applied on T/L of characteristic impedance Z_1

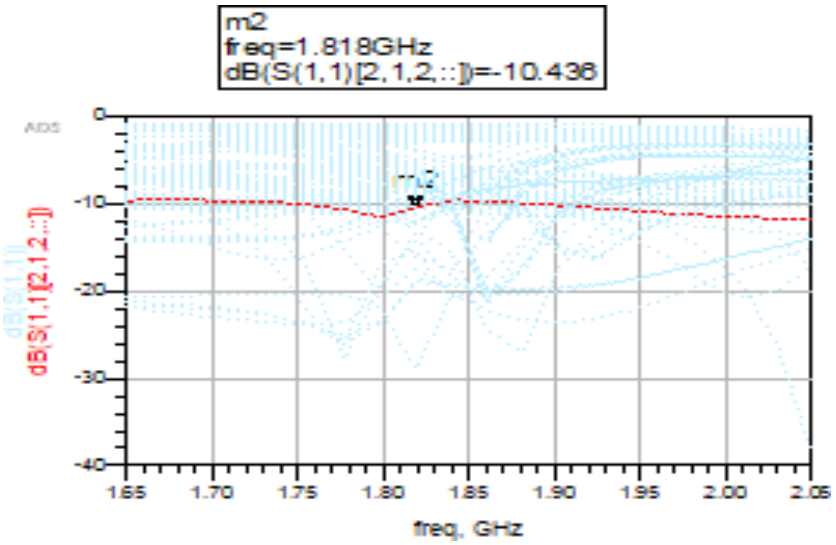


Figure 4.30: S Parameter (S_{11}) for circuit with Parametric Sweep applied on T/L of characteristic impedance Z_1

We chose these above-mentioned values depicted in the solid red lines from the parametric sweep, where h (height of the T – junction) is kept constant because we cannot increase the distance between the transmission line due to unavailability of SMD component height. At these values, the NGD is good enough as it can been seen in **Figure 4.29**, but the matching has suffered as shown in **Figure 4.30**. But once again we will see that collectively both will improve.

4.5.3 Finalized Circuit:

When we update the circuit with these updated results of coupled lines and transmission lines, after integrating both the results extracted from the parametric sweep of the coupled line and the Z1 transmission line, we get the following circuit of **Figure 4.31**.

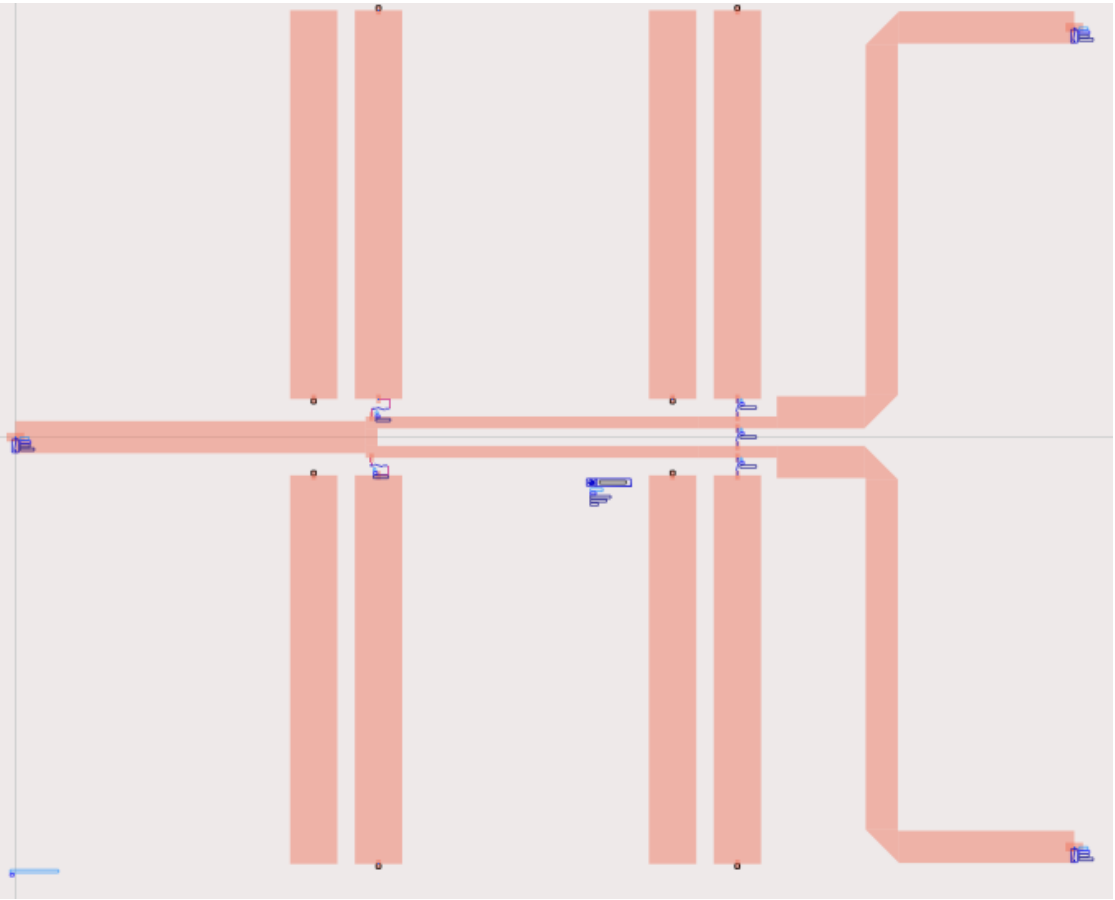
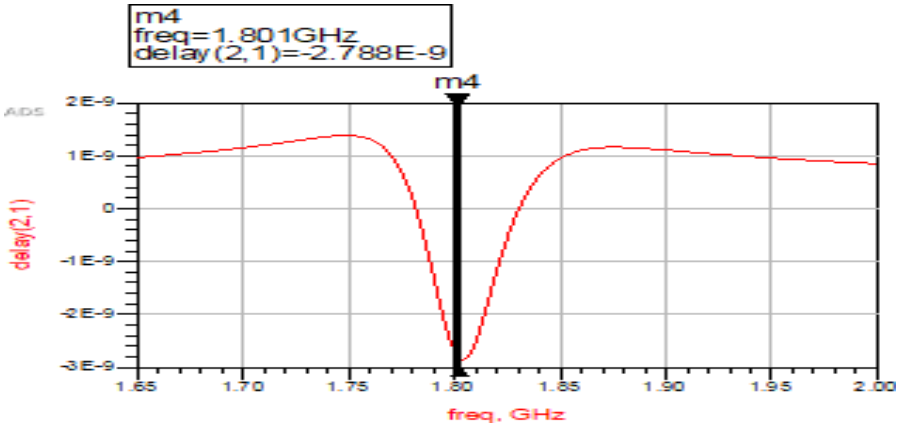
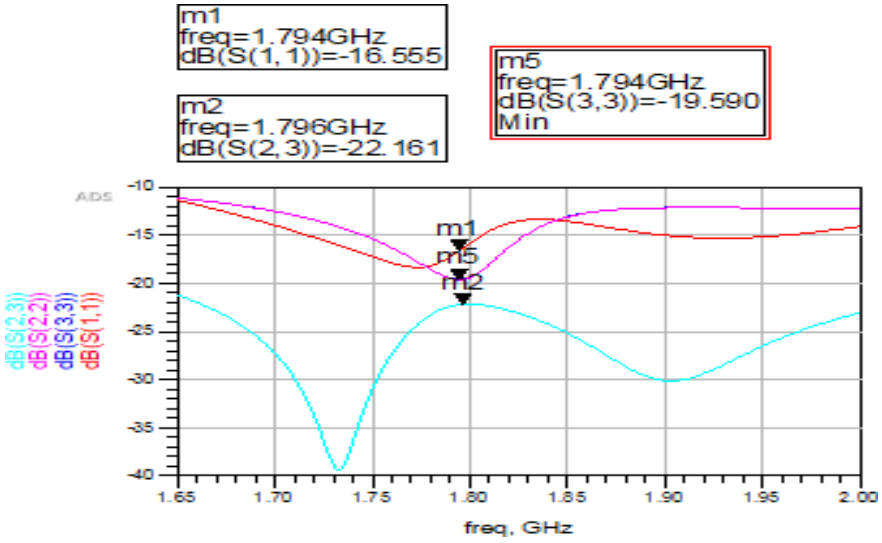


Figure 4.31: Schematics of Updated Circuit

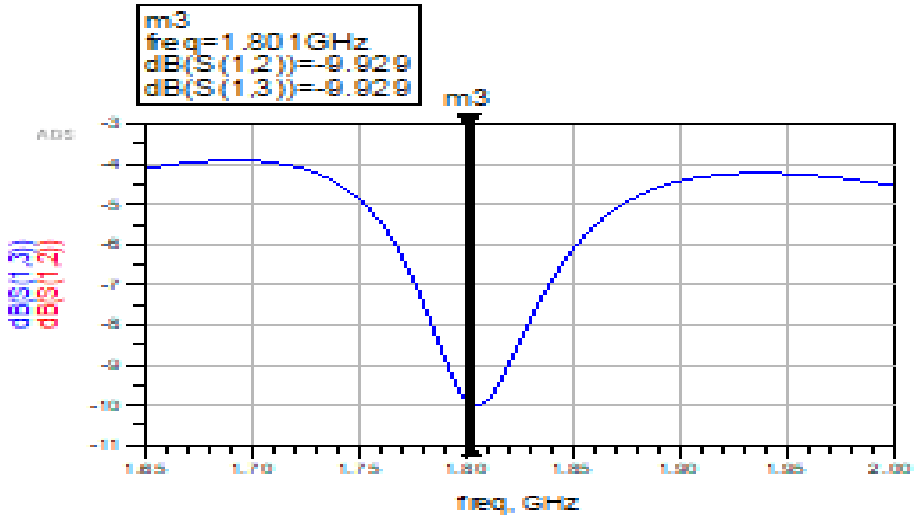
Running the S Parameter simulation in the schematic after connecting all the lumped elements, we get the results shown in **Figure 4.32**.



(a)



(b)



(c)

Figure 4.32 (a) Group delay of the updated circuit. (b) S_{11} S_{22} S_{33} and S_{23} of Updated Circuit. (c) S_{12} and S_{13} of the updated circuit

As seen in **Figure 4.32 (a)**, the group delay of the final simulated circuit came out to be -2.788 ns which is close to the calculated value of -2.9984 ns. The difference between simulated and calculated is because of the adjustments we did to ensure the physical constraints of the circuit like maintaining proper spacing for the resistor (resistor size is fixed) to be soldered. Or to ensure that the circuit does not violate the requirements given by the manufacturer. The S parameters of the circuit also improved as seen in **Figure 4.32** (b) and (c), in comparison to the previous results of section 4.5.1 and 4.5.2.

Just to confirm that these results do make sense, we plot the following momentum results of the circuit because these are the actual results that show how the real circuit will behave in actual setup.

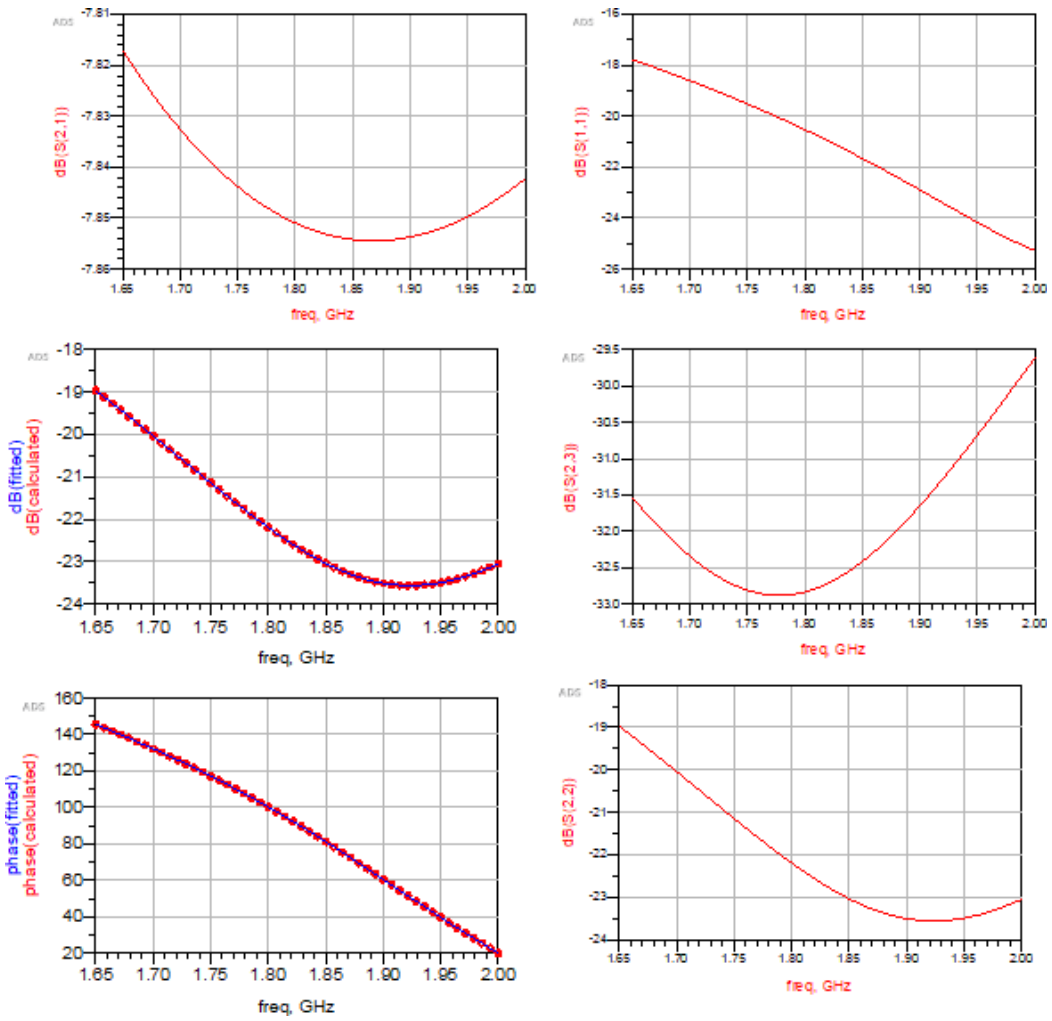


Figure 4.33: Momentum Simulation Results of the updated circuit providing S parameters and Phase response of the circuit

For S parameters the results in **Figure 4. 33** is pretty convincing. However, the momentum results don't provide the actual result because the lumped elements are not connected in the layout, even after that the S parameter results are somewhat promising and are comparable to the schematic results discussed above.

Chapter 5

5.1 Gerber File Generation:

The circuit in **Figure 4.24** is our finalized circuit, now we shift the coupled lines horizontally, so that the resistors are connected easily, and vertically to ensure the distance is not greater than the SMD resistor height. We adjust the circuit to ensure the required physical constraints are met which are provided by the manufacturer, for example for some manufacturers it is required that conductor to conductor distance should be kept greater than 0.2 mm. In Addition to that, we also add two types of vias, one that is placed to provide the ground to the actual circuit (small blue circles on coupled lines in the **Figure 5.1**), and the other via is for the m2 screws (big blue circles outside of the circuit in **Figure 5.1**) to fit the circuit on the aluminum plate. After doing all this, we get the following finalized circuit of **Figure 5.1**.

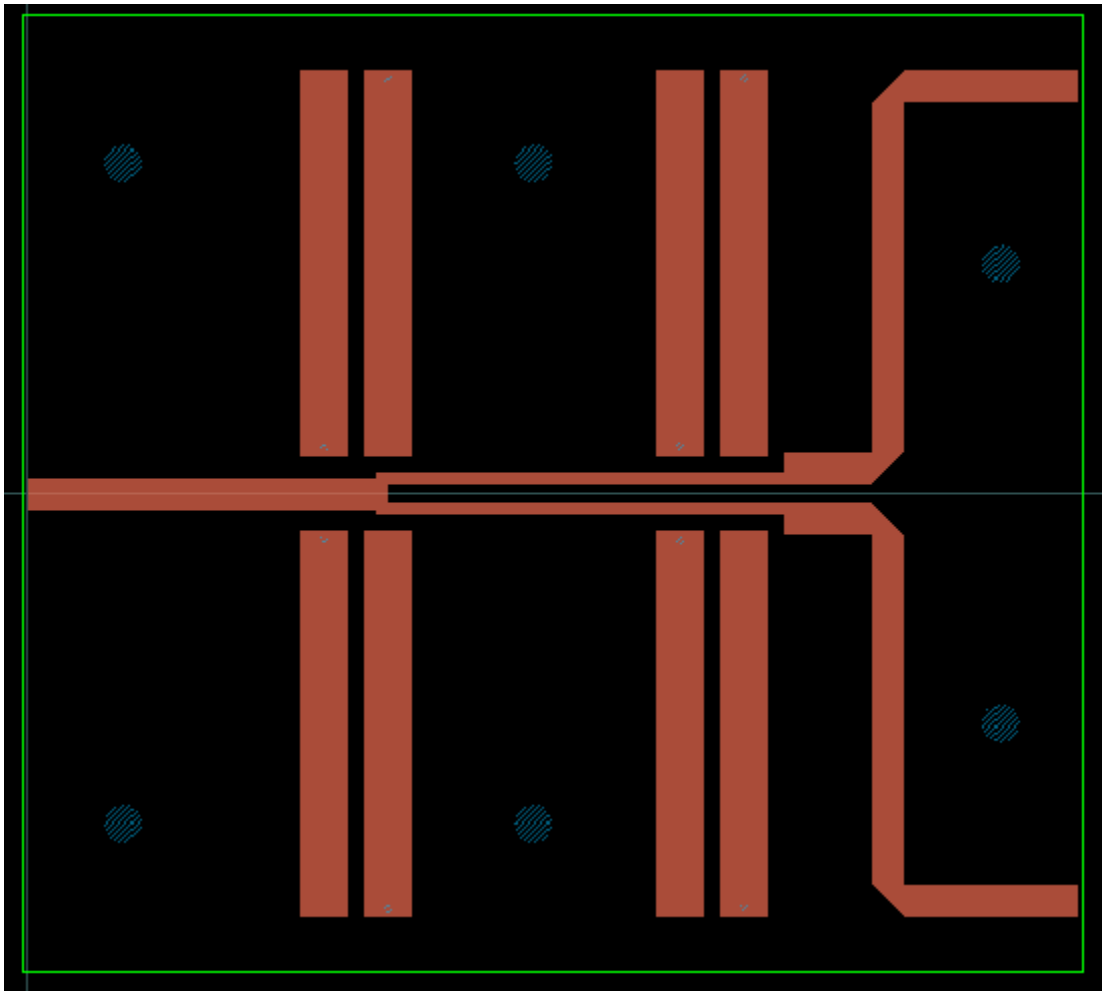


Figure 5.1: Setting layout to generate the Gerber file of final Circuit

The Gerber file of the finalized circuit is generated by

File -> export -> and then select Gerber. This Gerber file was then provided for fabrication and after a few days' wait, we got the circuit which can be seen in F**igure 5.2**.

5.2 Getting to the testable Circuit:

After getting the fabricated circuit, we connect all the components to get the final circuit so that it can be tested. The SMD components needed were 100- and 200-ohms resistors and 3 SMA connectors. We procured both 0603 and 0805 sizes of both resistors just to be careful that we don't run into any problem related to their size, while soldering.

5.2.1 Soldering the components:

SMD resistors were soldered with the help of magnifying glass and Heating Plate. Soldering Paste was carefully put in desired locations and components were placed with the help of magnifying glass. After this, the heating plate was turned ON and when the temperature rose to 190^{o} C, the paste melted, and components were fixed (pasted). SMA connectors were soldered with the help of soldering iron, and it was done in a way that the input pin was connected on copper lines and the ground was connected with the surface of the port.

5.2.2 Testing and Measurement:

After soldering and making the circuit ready for testing. We tested the circuit using a Vector Network Analyzer (VNA) at the Microwave Engineering Research Lab (MERL). The VNA is first calibrated for the frequency range of 1.6 GHz to 2 GHz through an Electronic Calibration module and the number of points is also set during calibration. Then we connect port 1 of our circuit to one port of the VNA and port 2 is connected to the other connector of the VNA whereas the third port is connected with 50 ohms termination as shown in **Figure 5.2**.

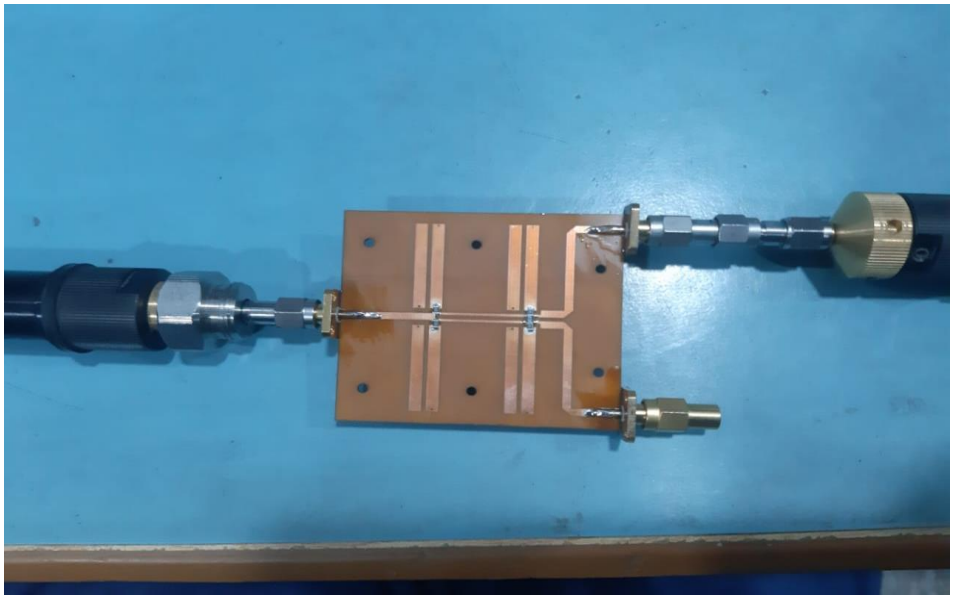


Figure 5.2: Connection scheme to measure S parameters

After that, VNA provides us with the S – parameters of the circuit, on the screen as seen in **Figure 5.3**.

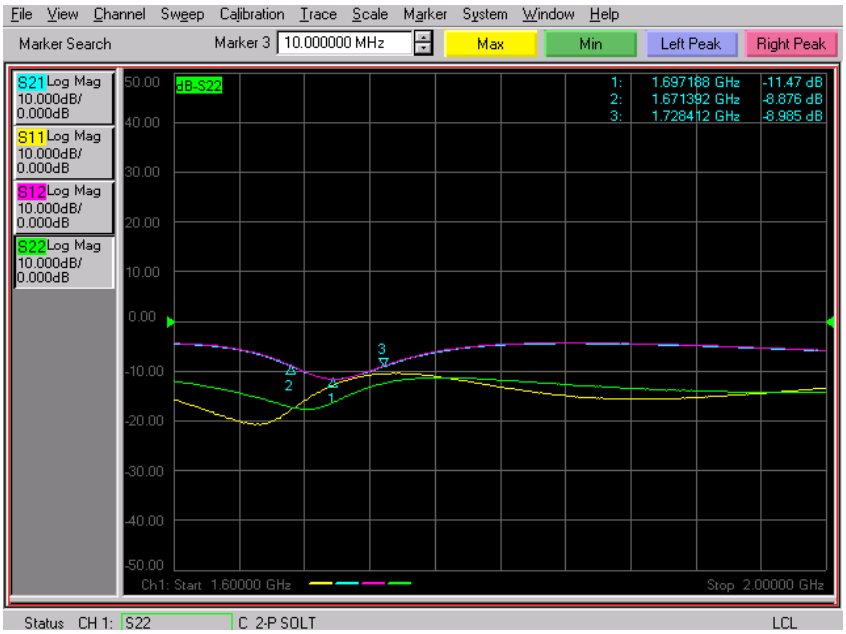
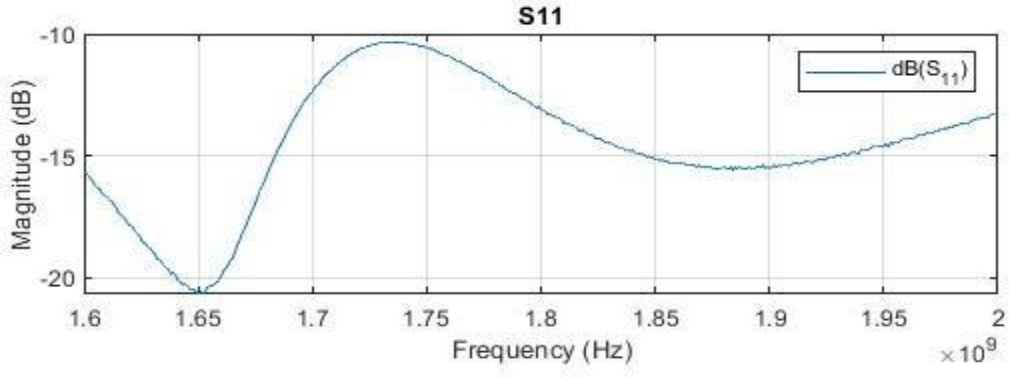
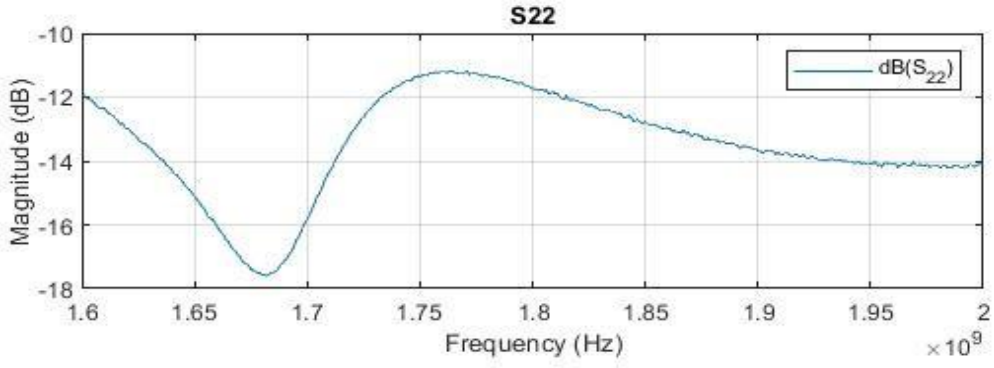


Figure 5.3: Screenshot of the Measured S-parameters displayed on VNA screen

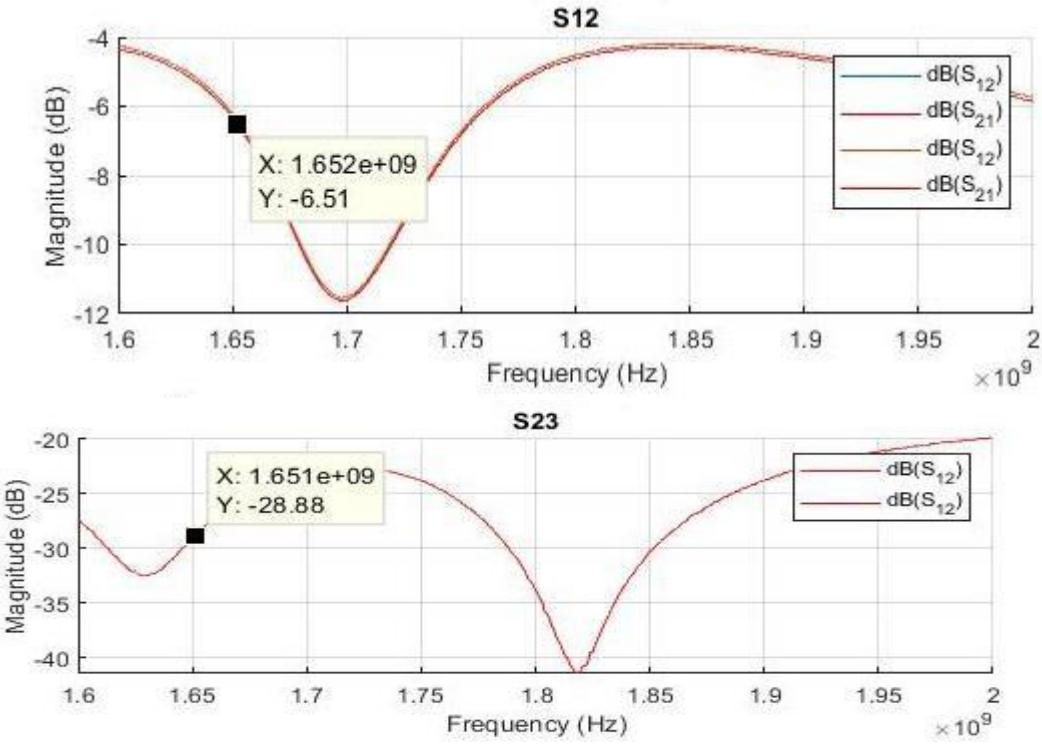
The measured results of the circuit are then exported to MATLAB and plotted as seen in **Figure 5.4**.



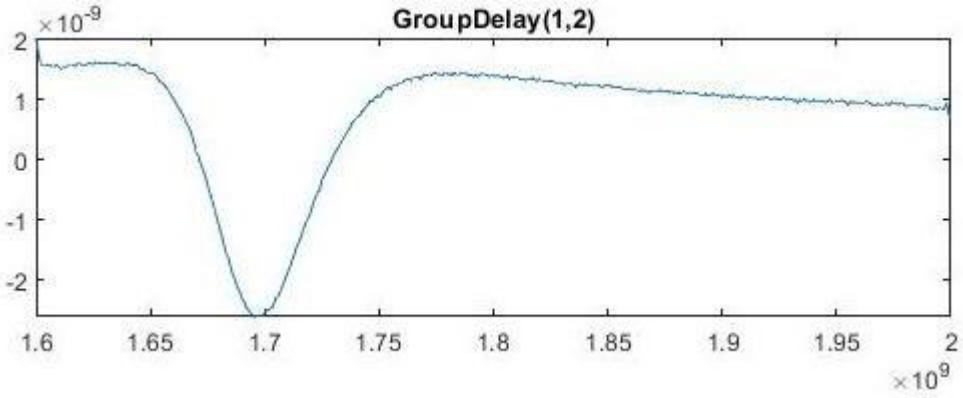
(a)



(b)



(c)



(d)

Figure 5.4 (a) Measured S11 of the circuit. (b) Measured S12 of the circuit. (c) Measured S_{12}, S_{21}, S_{13}, S_{31}, S_{23} and S_{32} of the circuit (d) Measured Group delay (GD_{12}) of the circuit

5.3 Result Comparison:

Table 5.1 provides the result comparison between the simulated and measured results of the Power divider circuit fabricated on FR-4 having 40 mils height.

Parameter	**Calculated**	**Simulated**	**Measured**
Frequency	1.8 GHz	1.8 GHz	1.698 GHz
S_{11}		-15.315 dB	-21 dB
S_{12}		-9.329 dB	-6.51 dB
S_{22}		-19.5 dB	-16 dB
S_{23}		-22.161 dB	-28.8 dB
Group Delay	-2.9974 ns	-2.788 ns	-2.608

Table 5.1

Although the matching i.e., Return loss, Insertion loss and Isolation of the circuit came out to be better than simulated, the Center frequency of the circuit is shifted to 1.7 GHz which can be caused due to the change in the length because of the soldering and SMA connector.

The Group Delay of the circuit came out to be equal to -2.608 ns, which is close to the simulated result that was equal to -2.788 ns and has a percentage error of 6.46 %. So, this result can be considered acceptable with respected to the theoretical and simulation results, and we have achieved our objective of making a Negative Group Delay Power Divider based circuit with center frequency of 1.8 GHz and fabricated on FR-4 substrate of height 40 mils with results close to the calculated as well simulated results.

5.4 Power Divider Circuit with different substrate height:

To study the variation of NGD with respect to changing substrate, similar steps as that of chapter 4 were carried out for the same substrate, Fr-4, with same parameters but different height (h) of 31 mils. After optimization, the circuit was simulated on ADS and the resultant circuit was fabricated and tested as described in section 5.1. Table 5.1 provides the calculated, simulated and measured results of Power divider with NGD characteristics for substrate of height 31 mils.

Parameter	**Calculated**	**Simulated**	**Measured**
Center Frequency	1.8 GHz	1.82 GHz	1.809 GHz
S_{11}		-23.254 dB	-26.96 dB
S_{12}		-6.37 dB	-7.44 dB
S_{22}		-19.599 dB	-19.43 dB
S_{23}		-33.909 dB	-44.32 dB
S_{33}		-19.617	-19.31
Group Delay	-1.6 ns	-1.34 ns	-0.8 ns

Table 5.2

S-parameters of the simulated and measured circuit are within acceptable ranges. S_{11} for both the cases is below -20 dB, which tells us that the circuit suffer from minimum reflection losses and is matched at the frequency of interest, similar comments can be made for S_{22} and S_{33}. S_{12} for simulated and measured results is below -6dB, which is due to the signal attenuation characteristics as mentioned in chapter 1. Isolation between port 2 and 3, S_{23} is better than -30 dBs showing that both the ports are isolated.

From Table 5.1, it can be seen that, at the center frequency, both simulated and fabricated circuits have Group Delay of -1.34ns and -0.8 ns, respectively.

5.5 Comparison of Two Power Divider Circuit

From Tables 5.1 and 5.2 one can see that the variation in height has an effect on the achievable NGD. The measured NGD for the substrate of height 40 mils is -2.608ns whereas the measured NGD for the substrate of height 31 mils is -0.8 ns. From the results it is quite evident that increasing height of the substrate increases the achievable NGD. As established in chapter 1, NGD is achieved by introducing losses in the circuit, a possible explanation can be made that increasing the substrate height increases the substrate losses of the circuit which in turn increases the NGD of the circuit.

Chapter 6

Conclusion and Future Work:

In this report, two types of circuits, based on published work, were designed and fabricated to achieve Negative Group Delay. The first circuit was an O=O circuit, consisting of a power divider and combiner, operating at center frequency of 1.2 GHz. The circuit produced an NGD of -0.97 ns at the center frequency, without any use of lumped component. Moreover, the circuit provided an S_{11} of -16 dB, whereas the attenuation was 1.2 dB.

The other circuit was a power divider with coupled line structure. The circuit was fabricated on FR-4 substrate of height 40 mils and it produced an NGD of -2.608 ns. In order to observe the effect of height of the substrate on NGD of the circuit, we simulated and fabricated another circuit on FR-4 substrate with height of 31 mils. It was observed from the results that when the height of substrate was increased, NGD also increased. At 31mils, circuit had an NGD of – 0.8 ns while the NGD of the 40mils circuit was -2.608ns. Both the circuits had an S_{11} lower than -20 dB, so NGD was achieved without compromising the matching of the circuits.

Regarding future work, we know that frequency of these circuits was low as compared to other microwave circuits so the first task would be to design circuit having NGD characteristics at higher microwave frequencies. Changing substrate also has implications so that also needs to be checked, i.e., the effect of $\boldsymbol{\varepsilon_r}$. Secondly, work should be done to increase NGD for higher frequencies and at the same time minimizing the losses.

These circuits can be utilized in the communication domain to overcome signal distortion by cancelling the positive group delay. One can investigate the domain of Active circuits which are the building blocks in any communication system like receiver and transmitter circuits. Additionally, these circuits are connected with other circuits, and it has its own implications, studying those varying effects should be an immediate task. As a result, one can have a circuit capable of utilizing the negative group delay characteristics as whole to improve the overall performance of the circuit.

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