IMPLEMENTATION OF INTERLEAVE DIVISION MULTIPLE ACCESS (IDMA)

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ABSTRACT

Interleave Division Multiple Access (IDMA) can be considered as a special case of Code Division Multiple Access (CDMA). A key principle of IDMA systems is user separation by means of user defined chip-level interleavers instead of by unique signatures as in conventional CDMA. IDMA inherits many advantages of CDMA in addition to having a detection algorithm of much lower complexity and possessing many desirable features to meet the challenges of future wireless systems.

IDMA system has already been successfully simulated using Visual C++ but the process is time consuming owing to the receiver’s chip by chip iterative detection. The purpose of this research is to optimize the IDMA scheme for deployment in a real time environment by significantly reducing the system’s processing delays.

In this thesis an IDMA system model is implemented in SIMULINK in which dependent iterative loops are removed, processing delays are reduced and a software test bed for IDMA is developed. This test bed can be used to study the performance of IDMA system with varying system parameters and channel conditions. In addition, the model has been successfully compiled in SIMULINK’s Real Time Workshop (RTW) which facilitates the transfer of IDMA model to a variety of compatible hardwares, thus ensuring that the model is ready for deployment in real time environment.

DEDICATION

Dedicated To My Beloved Parents, Teachers and Friends

ACKNOWLEDGMENTS

Praise to **Allah S.W.T.** the All Mighty, the Most Beneficient and Most Merciful for all His blessings and guidance throughout my study.

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Most importantly, I am extremely grateful to my parents for their absolute faith and confidence in me, their unconditional love and dedicated support. It is to them that I dedicate this thesis.

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KEY TO SYMBOLS OR ABBREVIATIONS

AMPS	Advanced Mobile Phone Service
APP	a posteriori Probability
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CDMA	Code Division Multiple Access
CDG	CDMA Development Group
CRE	Chip Reliability Estimator
DAMPS	Digital AMPS
DCC	Digital Control Channel
DEC	Decoder
EDGE	Enhanced Data GSM Environment
ESE	Elementary Signal Estimator
ETACS	Extended Total Access Communication System
E-TDMA	Extended TDMA
EVDO	Evolution Data Only
EVDV	Evolution Data and Voice
FDMA	Frequency Division Multiple Access
FEC	Forward Error Correction
FWA	Fixed Wireless Access
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communication
IDMA	Interleave Division Multiple Access
IP	Internet Protocol

ISI	Inter Symbol Interference
ITU	International Telecommunications Union
LLR	Log Likelihood Ratio
MAC	Multiple Access Channel
MAI	Multiple Access Interference
MC-IDMA	Multi Carrier IDMA
MIMO	Multiple Input Multiple Output
MLD	Multi Layer Detector
MLI	Multi Layer Interference
MMSE	Minimum Mean Squared Error
MRC	Maximal Ratio Combining
MUD	Multiple User Detection
NADC	North American Digital Cellular
NTACS	Narrowband Total Access Communication System
NMT	Nordic Mobile Telephony
OCDM	Orthogonal Code Multiplexing
OFDM	Orthogonal Frequency Division Multiple Access
PAN	Personal Area Network
PLACE	Pilot Layer Aided Channel Estimator
PCS	Personal Communication Services
PDC	Personal Digital Cellular
PN	Pseudo random Noise
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
RTT	Radio Transmission Technology

RTW	Real Time Workshop
TACS	Total Access Communication System
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division Synchronous CDMA
UMTS	Universal Mobile Telecommunications System
WLAN	Wireless Local Area Network
WCDMA	Wide-band CDMA
WiMAX	Worldwide Interoperability for Microwave Access
WLL	Wireless Local Loop
3GPP	Third Generation Partnership Project (3GPP)

Chapter 1

INTRODUCTION

1.1 Introduction

Interleave Division Multiple Access (IDMA) [1] can be considered as a special case of Code Division Multiple Access (CDMA). A key principle of IDMA systems is user separation by means of different chip-level interleavers; unlike conventional CDMA in which users are distinguished by unique signatures. In IDMA, the data of each user is first encoded by a (very) low-rate encoder and then interleaved. No spreading code is used. IDMA inherits many advantages from CDMA, in particular, diversity against fading and mitigation of the worst-case other-cell user interference. A special feature of IDMA is that it makes use of a very simple (and near-optimal) chip-by-chip iterative multi user detection algorithm [2]. The complexity is independent of the number of users. A very large number of users can be processed with modest computing power while maintaining receiver simplicity as well as high performance in multi path environments. Furthermore, the scheme displays high spectral efficiency and near limit performance. This renders IDMA a scheme worth reckoning for the Fourth Generation (4G) of Wireless Communication. 4G communication systems require bandwidth efficiency and low complexity receivers to accommodate high data rates and large number of users per cell. Considering the substantial advantages offered by IDMA, it can be regarded as a powerful scheme to meet the ever-growing challenges of mobile communication by offering key benefits like flexibility for multi-rate services (e.g., mixed voice and IP), higher bandwidth and power efficiency, simple design, and low detector complexity.

1.2 Problem Statement

Simulations of IDMA system have been conducted successfully in Visual C and MATLAB (m-file program) at City University, Hong Kong and Military College of Signal (MCS), NUST, Pakistan. However, the simulation results display a processing delay of three to five hours, a trait not at all desirable in a communication system. These processing delays have to be reduced considerably before the IDMA scheme can be deployed in a real-time environment. This emphasizes the need for investigating an implementation method to ensure fast processing and a simulation environment capable of optimizing IDMA for real time applications.

1.3 Objectives

The primary objective of this research work is the development of an implementation method to prepare IDMA scheme for deployment in a real time environment.

1.4 Thesis Organization

Chapter 2 provides an overview of the history of wireless communication, current trends and the shape of things to come. The discrepancies of each wireless era leading to the subsequent are outlined. A brief introduction to 4G systems is also presented. Chapter 3 is a comprehensive study of Interleave-Division Multiple-Access Systems, a novel approach to spread-spectrum mobile systems. The IDMA detection principles in single-path and multi-path environments are outlined. A low-cost iterative chip-by-chip multi-user detection algorithm is described with complexity independent of the number of users and increasing linearly with the path number. Chapter 4 discusses the advantages of IDMA extensions and their ability to fulfill the requirements of 4G systems. Chapters 2, 3 and 4 are related to literature review, necessary to understand the concepts on which this thesis work is based. One having sufficient background knowledge can skip this portion and proceed directly to Chapter 5. The actual research work starts from Chapter 5 which provides a detailed explanation of the implementation of complete IDMA system in SIMULINK environment. The deployment issues of this SIMULINK model as well as simulation results are discussed in Chapter 6.Lastly, Chapter 7 concludes this thesis and highlights avenues for further research in this area.

1.5 Conclusion

This thesis presents an efficient implementation of complete IDMA system in SIMULINK. The model is designed so as to curtail processing delays and is prepared for deployment in real time environment.

Chapter 2

EVOLUTION OF WIRELESS COMMUNICATION

2.1 Introduction

The wireless landscape is characterized by continual evolution, rapid innovation and technological change. Researches are persistently investigating techniques that make efficient use of available spectrum and offer consumers greater range, quality of service, and data transfer rates. The history and evolution of wireless communication from First Generation (1G) to Fourth Generation (4G) are discussed in this chapter.

2.2 First Generation (1G)

1G systems emerged in the late 1970s and lasted through the 1980s. These analog systems were the first true mobile phone systems, known at first as "cellular mobile radio telephone." The most prominent 1G systems are Advanced Mobile Phone Service (AMPS), Nordic Mobile Telephone (NMT), and Total Access Communication System (TACS).

2.2.1 AMPS

First-generation cellular took off in 1982 with the deployment of commercial AMPS in the United States (U.S). Originally, AMPS operated in the 800 Mega Hertz (MHz) frequency band using 30 kilo Hertz (kHz) wide channels. The frequency bands allocated were 824 MHz to 849 MHz (uplink) and 869 MHz to 894 MHz (downlink).The division of the spectrum into sub-band channels was achieved by using Frequency Division Multiple Access (FDMA). The band accommodated 832 duplex channels among which 21 were reserved for call setup and the rest for voice communication. [3]

2.2.2 TACS

TACS is the European version of AMPS. After its introduction in the United Kingdom (U.K.) in 1985, over 25 countries offered TACS services. TACS was deployed in 25 kHz radio channels with frequency ranges of 890 MHz to 915 MHz (uplink) and 935 MHz to 960 MHz (downlink). An additional 16 MHz of channel bandwidth was added to accommodate more channels to form Extended TACS (ETACS).

Japanese version of TACS was called JTACS. The only significant differences were the frequency bands and number of channels. Another variation of TACS was Narrowband TACS (NTACS) which reduced channel bandwidth from 25 kHz to 12.5 kHz.

2.2.3 NMT

NMT system was developed by the telecommunications administrations of Sweden, Norway, Finland, and Denmark to create a compatible mobile telephone system in the Nordic countries. The first commercial NMT 450 cellular system was available at the end of 1981. Due to its rapid success and limited capacity of the original system design, NMT 900 system version was introduced in 1986.

NMT 450 used a lower frequency (450 MHz) and higher maximum transmitter power level which allowed a larger cell site coverage areas while NMT 900 used a higher frequency (approximately 900 MHz band) and a lower maximum transmitter power which increased system capacity. NMT 450 and 900 could co-exist which allowed the use of a single switching center. [4]

When NMT mobile phones accessed the cellular system, they either found an unused voice channel and negotiated access directly or began conversation without the assistance of a dedicated control channel. Because scanning for free voice channels was very time consuming, NMT 900 system used a dedicated control channel called the calling channel.

NMT 450 system was frequency duplex with 180 channels (except Finland which only had 160 channels). The channel bandwidth was 25 kHz with a frequency duplex spacing of 10 MHz. The NMT 900 system had 999 channels or 1999 interleaved channels. [5]

Numerous incompatible 1G services emerged around the world during 1980s. However, each carrier delivered service to a limited serving area, there were no standards to enable roaming and channel capacity was rapidly being exhausted.

2.3 Second Generation (2G)

The 2G systems designed in the 1980s were based on digital technology rather than analog. They provided circuit- switched data communication services at a low speed. This allowed multiple conversations on the same channel, vastly increasing the capacity of cellular frequencies. While the primary use of this technology was still speech transmission, new features such as fax, data transmission and message services were becoming increasingly common. In addition, the industry was responding to the security concerns of cellular users by developing fraud prevention and encryption technologies.

A negative consequence of these technological advances was a competitive rush to design and implement digital systems leading to a variety of different and incompatible standards, mainly, Global System for Mobile Communication (GSM), Interim Standard-54 (IS-54) / Interim Standard -136 (IS-136), Time Division Multiple Access (IS-54 / IS-136 TDMA), Extended TDMA (E-TDMA), Personal Digital Cellular (PDC) and Interim Standard -95 CDMA (IS-95 CDMA).

2.3.1 GSM

GSM, initially created to provide a single standard pan-European cellular system uses TDMA technology. Its development began in 1982, and the first commercial GSM digital cellular system was activated in 1991. GSM has evolved to be used in a variety of systems and frequencies (900 MHz, 1800 MHz and 1900 MHz) including Personal Communications Services (PCS) in the U.S. and Personal Communications Network (PCN) systems throughout the world.

GSM uses time division multiplexed 200 kHz channels to enable up to 8 users to access each carrier by the assignment of a particular time slot. To allow duplex operation, GSM voice communication is conducted on two different radio frequencies. The duplex distance (distance between uplink and downlink frequencies) is 80MHz. During a voice conversation, one time slot period is dedicated for transmitting, one for receiving, and six remain idle. The mobile phone uses some of the idle time slots to measure the signal strength of surrounding cell carrier frequencies in preparation for handover [6].

A GSM carrier transmits at a rate of 270 Kbps, but a single GSM channel or time slot is capable of transferring only 1/8th of that (about less than 33 Kbps due to the transmission of non-information bits such as synchronization bits).

2.3.2 IS-136 TDMA

IS-136 TDMA is a digital system that uses TDMA technology. It evolved from the IS-54 specification that was developed in U.S. in the late 1980’s to allow the gradual evolution of AMPS to digital service. It is also referred to as Digital AMPS (DAMPS) or North American Digital Cellular (NADC).

A primary feature of the IS-136 systems is their ease of adaptation to the existing AMPS [6]. This is due to the fact that IS- 136 radio channels retain the same 30 kHz bandwidth as AMPS channels. Another factor was the development of dual mode mobile telephones operating on either IS-136 digital traffic (voice and data) channels or the existing AMPS radio channels.

All IS-136 TDMA digital radio channels are divided into frames with 6 time slots. The time slots used for the correspondingly numbered forward and reverse channels are time related so that the mobile telephone does not simultaneously transmit and receive. Also, a standard time slot is used as a Digital Control Channel (DCC) carrying system and paging information.

2.3.3 E-TDMA

Extended TDMA was developed by Hughes Network Systems in 1990 as an extension of IS-136 TDMA. ETDMA uses the existing TDMA radio channel bandwidth and channel structure and its receivers are tri-mode as they can operate in AMPS, TDMA, or ETDMA modes.

To overcome the wastage of bandwidth in TDMA due to the allocation of a time slot to a specific conversation whether or not anyone is speaking at that moment, ETDMA assigns subscribers dynamically on requirement basis. It transmits data through the pauses in normal speech. When subscribers have something to transmit, they put one bit in the buffer queue. The system scans the buffer, notices that the user has something to transmit, and allocates bandwidth accordingly. If a subscriber has nothing to transmit, the queue simply goes to the next subscriber. So, instead of being arbitrarily assigned, time is allocated according to need. If partners in a phone conversation do not speak over one another, this technique can almost double the spectral efficiency of TDMA, making it almost 10 times as efficient as analog transmission [6].

2.3.4 IS-95 CDMA

IS-95, based on CDMA technology, was initially developed by Qualcomm in the late 1980's. CDMA is a form of Spread-Spectrum communication that has been used in military applications for many years. Spreading of signals is achieved by Direct Sequence method in which digital data is directly coded at a much higher frequency. The code is generated pseudo-randomly, the receiver knows how to generate the same code, and correlates the received signal with that code to extract the data. Since Spread Spectrum signals are so wide, they transmit at a much lower spectral power density than narrowband transmitters.

IS-95 CDMA allows for voice or data communications on either a 30 kHz AMPS channel (when used on the 800 MHz cellular band) or a new 1.25 MHz CDMA channel. Some of its key attributes are capacity expansion by allowing multiple users to share a single radio channel, the optional use of same radio carrier frequencies in adjacent cell sites thus eliminating the need for frequency planning, the use of wide-band radio channel resulting in less severe fading and consistent quality voice transmission under varying radio signal conditions.

CDMA channels are unique in the sense that CDMA multiplies (and therefore spreads the bandwidth of) each signal with a unique Pseudo-random Noise (PN) code that identifies each user within a channel and is independent of the data of that user. Each CDMA channel contains the signals of many ongoing calls (voice channels) together with pilot, synchronization, paging, and control channels. Receivers select the signal they are receiving by correlating (matching) the received signal with the proper PN sequence. The correlation enhances the power level of the selected signal and leaves others unenhanced. The use of unique codes and synchronous reception allows multiple users to access the same frequency band simultaneously thus rendering CDMA as highly spectrally efficient.

Each IS-95 CDMA channel is divided into 64 separate (PN coded) channels [7]. A few of these channels are used for control, and the remaining carry voice information and data. A CDMA channel of 64 traffic channels can transmit at a maximum information throughput rate of approximately 192 Kbps, so the combined data throughput for all users cannot exceed 192 Kbps. To obtain a maximum of 64 communication channels in each CDMA channel, the average data rate for each user should approximate 3 Kbps. If the average data rate is higher, less than 64 traffic channels can be used. CDMA systems can vary the data rate for each user depending on voice activity (variable rate speech coding), thereby decreasing the average number of bits per user to about 3.8 Kbps. Varying the data rate according to user requirement allows more users to share the channel, but with slightly reduced voice quality. This is called soft capacity limit [8].

In 1997 the CDMA Development Group (CDG) registered the trademark cdmaOne ^{TM} as a label to identify 2G systems based on the IS-95 standard and related technologies.

2.4 2.5 G

During 1990’s, the telecommunications industry, recognizing the need for a single global standard of wireless communication, began making efforts to define a Third Generation (3G) system which would eliminate previous incompatibilities and become a truly global standard. However, the consumer market was pressing for improved data transmission and features in the present, not sometime in the future. This led to an intermediate step between 2G and 3G, called 2.5G.

Introduced in 2001, 2.5G systems use digital packet switching technology, providing increased capacity on the 2G radio channels and higher throughput (up to 384 kbps) for data service. A very important aspect of 2.5G is that the data channels are optimized for packet data, which introduces access to the internet from mobile devices, streaming video and enhanced multimedia applications. Primary 2.5G technologies are General Packet Radio Service (GPRS), (Enhanced Data GSM Environment (EDGE) and CDMA2000^{TM} Radio Transmission Technology (1xRTT).

2.4.1 GPRS

GPRS is a portion of the GSM specification that allows packet radio service on the GSM system. The GPRS system adds (defines) new packet channels and switching nodes within the GSM system. It provides for theoretical data transmission rates up to 172 Kbps [6].

2.4.2 EDGE

EDGE is an evolved version of GSM that uses 8 levels Phase Shift Keying (8PSK) and packet transmission for advanced high-speed data services. 8PSK allow one symbol change to represent 3 bits of information. This is 3 times the amount of information that is transferred by a 2 level Gaussian Minimum Shift Keying (GMSK) signal used by the first generation of GSM system. This results in a data transmission rate of 604.8 Kbps and a net maximum delivered theoretical data transmission rate of 384 Kbps.

2.4.3 CDMA2000^{TM}, (1xRTT)

CDMA2000^{TM} is a 3G standard allowing evolution of IS-95 networks to offer 3G services. The original CDMA2000^{TM} proposal contained two distinct evolutionary phases, the first known as 1xRTT used the same 1.25 MHz channels as IS-95 but delivered increased capacity and data rates as compared to IS-95. The second phase, called 3xRTT used 3 times the spectrum of IS-95 (3.75 MHz) and was capable of delivering data rates up to 2 Mbps. However, recent evolutions of 1xRTT are offering data rates in excess of this thus rendering 3xRTT redundant.

Evolution Data Only (1xEVDO) and Evolution Data and Voice (1xEVDV) are evolved versions of CDMA2000^{TM} 1xRTT using the same 1.25 MHz channel bandwidth as the IS-95 system [6]. The 1xEVDO version provides multiple voice channels and medium rate data services allowing data transmission rates up to 2.5 Mbps. It has an upgraded packet data transmission control system that allows for burst data transmission rather than for continuous voice data transmission. 1xEVDV provides for both data and voice service with a maximum data transmission rate of approximately 2.7 Mbps.

2.5 Third Generation (3G)

The International Telecommunications Union (ITU) made an effort to establish a single standard for wireless networks in 1999 to standardize wireless communications and make global roaming with a single handset possible. The concept of a single standard evolved into a family of 3G wireless standards of which the most widely accepted are CDMA2000, Wide-band CDMA (WCDMA) and Time Division Synchronous CDMA (TD-SCDMA). 3G wireless networks were required to provide high speed data transmission, greater network capacity, Internet Protocol (IP)based services, global roaming, and multimedia communications.The minimum bit-rate requirements were fixed as 2 Mbps in fixed or in-building environments, 384 Kbps in pedestrian or urban environments and 144 Kbps in wide area mobile environments.

2.5.1 WCDMA

WCDMA is a 3G digital cellular system that uses radio channels that have a wider bandwidth than 2G systems such as GSM or IS-95 CDMA. WCDMA is normally deployed in a 5 MHz channel plan.

The Third Generation Partnership Project (3GPP), featuring standards agencies from Japan, Europe, Korea, China and the U.S., oversees the creation of industry standards for 3G systems [6]. The 3GPP technology, also known as the Universal Mobile Telecommunications System (UMTS), is based on an evolved GSM core network that contains 2.5G elements, namely GPRS switching nodes. This concept allows a GSM network operator to migrate to WCDMA by adding the necessary 3G radio elements to their existing network, thus creating ‘islands’ of 3G coverage when the networks first launch.

2.5.2 CDMA2000

CDMA2000 is a family of standards representing the evolution of IS- 95 CDMA offering enhanced packet transmission protocols for advanced high-speed data services. It operates in the same 1.25 MHz radio channels as used by IS-95 and offer backward compatibility with IS-95 [6]. CDMA2000 is overseen by the Third Generation Partnership Project 2 (3GPP2), a standards setting project focused on developing global specifications for 3G systems.

2.5.3 TD-SCDMA

TD-SCDMA is a Chinese standard offering voice services and data services, both circuit-switched and packet-switched, at rates up to 2 Mbps. It uses a Time Division Duplex (TDD) technique in which transmit and receive signals are sent on the same frequency but at different times [6]. The timeslots on the radio carrier can either be allocated symmetrically for services such as speech or asymmetrically for data services where the bit rates in the two directions of transmission may differ significantly.

2.6 Fourth Generation (4G)

The official name for 4G is “3G and beyond”, an expression used to describe the next complete evolution in wireless communications. A formal definition of 4G has not been formulated yet; however, there are certain objectives defined. In order to fit the 4G category, a network must be a fully IP based integrated system, capable of providing speeds between100 Mbps-1 Gbps (both indoors and outdoors) with premium quality, high security and affordable cost. This can only be achieved by the convergence of wired and wireless technologies [9]. 4G systems are expected to solve the still remaining problems of 3G systems and to provide a wide variety of new services, from high quality voice to high definition video to high data rate wireless channels. The term 4G is used broadly to include not only cellular telephone systems but also several types of broadband wireless access communication systems. One of the terms used to describe 4G is MAGIC—Mobile multimedia, Anytime anywhere, Global mobility support, Integrated wireless solution, and Customized personal service.

4G systems are intended to complement and replace 3G systems, perhaps in 5 to 10 years. They will have broader bandwidth, higher data rate, smoother and quicker handoff and will focus on seamlessly integrating terminals, networks, and applications to satisfy increasing user demands. With 4G, a range of new services and models will be available. The Fourth Generation will encompass all systems from various networks (public and private), operator driven broadband networks and ad hoc networks.

The all-encompassing integrated perspective shows the broad range of systems that 4G intends to absorb, including satellite broadband, cellular 3G systems, Wireless Local Loop (WLL), Fixed Wireless Access (FWA), Wireless Local Area Network (WLAN) and Personal Area Network (PAN), all with IP as the integrating mechanism [9]. This seamless connectivity of networks is demonstrated in Figure 2.1. With 4G, a range of new services and models will be available.

Many companies have taken self-serving definitions of 4G to suggest they have 4G already in existence today, such as several early trials and launches of Worldwide Interoperability for Microwave Access Inc. (WiMAX) (group promoting IEEE 802.16 wireless broadband standard) which is part of the formal ITU standard for 3G. Other companies have made prototype systems calling those 4G. While it is possible that some currently demonstrated technologies may become part of 4G, until its standard or standards have been defined, it is impossible for any company currently to provide with any certainty wireless solutions that could be called 4G cellular networks conforming to the eventual international standards for 4G.

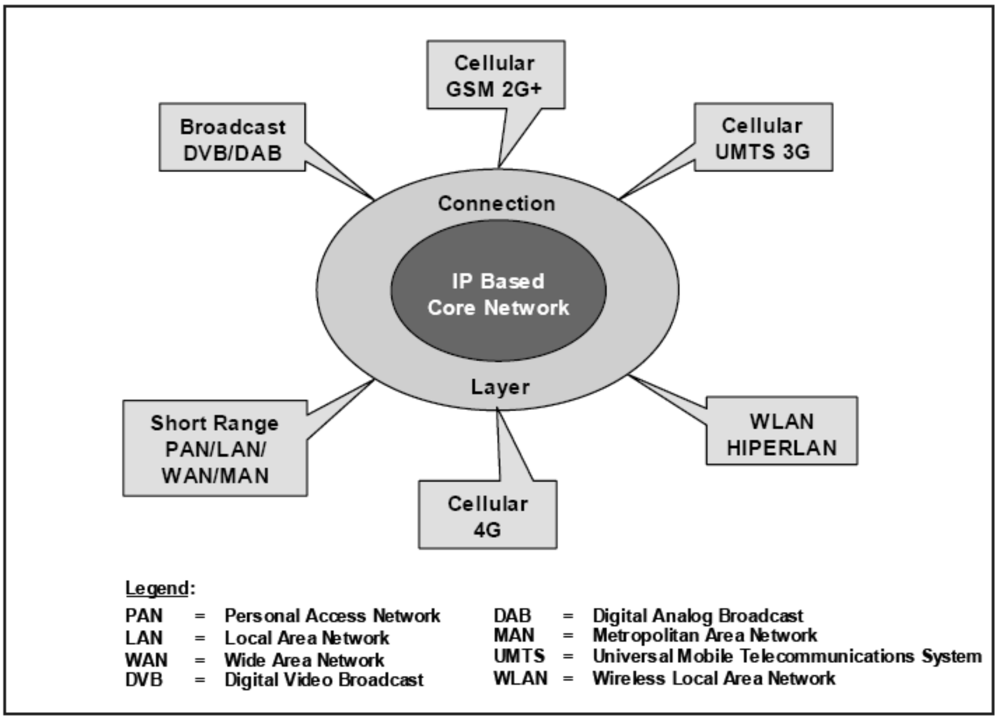

Figure 2.1: Seamless Connections of Networks [10]

2.7 Conclusion

This chapter provided a brief overview of the history of wireless communication. It outlines the major technologies of each generation and presents an overall vision of the 4G features, framework, and integration of mobile communication. As a promise for the future, 4G systems or cellular broadband wireless access systems have been attracting much interest in the mobile communication arena.

Chapter 3

INTERLEAVE DIVISION MULTIPLE ACCESS

3.1 Introduction

Direct-sequence Code Division Multiple Access (DS-CDMA or simply CDMA) has been adopted in second and third generation cellular mobile standards. While possessing many attractive features such as dynamic channel sharing, mitigation of cross-cell interference, asynchronous transmission, ease of cell planning, and robustness against fading, the performance of CDMA systems is mainly limited by multiple access interference (MAI) and Inter Symbol Interference (ISI). Encouraged by the success of turbo codes [11] in additive white Gaussian noise (AWGN) channels, turbo-type iterative multi-user detection (MUD) [12] has been extensively studied to overcome these problems and significant progress has been made. However, complexity is still a major concern since it increase with the increase in the number of users and much research has been carried out on this issue in pursuit of simple solutions without compromising performance. Moreover, a considerable gap continues to exist between the achieved performance and the theoretical limits of multiple access channels.

A conventional random waveform CDMA (RWCDMA) system (such as IS-95) involves separate coding and spreading operations. Theoretical analysis shows that the optimal multiple access channel (MAC) capacity is achievable only when the entire bandwidth expansion is devoted to coding [13]. This suggests combining the coding and spreading operations using low-rate codes to maximize coding gain and using interleavers to distinguish signals from different users. The principle of using chip level interleavers for user separation has been rigorously researched and its potential advantages have been demonstrated. M. Moher and P. Guinand [12] investigated the possibility of employing interleaving for user separation in coded systems. F. N. Brannstrom [14] proposed narrow-band coded-modulation schemes in which trellis code structures are used for user separation. The merits of assigning different interleavers to different users in conventional CDMA have been demonstrated in [15] and [16]. Ref. [17] suggested a chip interleaved CDMA scheme and a maximal-ratio-combining (MRC) technique for MACs with ISI. Finally, a multiple access scheme, [1] [2] relying on interleaving as the only means of user separation, was proposed and named interleave-division multiple-access (IDMA). It allows a very simple chip-by-chip iterative MUD strategy [1] [2] and displays the advantages of high spectral efficiency, improved performance and low receiver complexity. The normalized MUD cost (per user) is independent of the number of users.

3.2 IDMA Transceiver Structure

The key principle of IDMA is that the interleavers $\{\pi_k\}$ should be different for different users. These interleavers disperse the coded sequences so that the adjacent chips are approximately uncorrelated, which facilitates the simple chip-by-chip detection scheme of IDMA [18] [19].

The upper part of Figure 3.1 shows the transmitter structure of the multiple access scheme under consideration with K simultaneous users. The input data sequence $\boldsymbol{d}_k$ of user-k is encoded based on a low-rate code C, generating a coded sequence $\boldsymbol{c}_k = [c_k(1), \ldots, c_k(j), \ldots, c_k(J)]^T$, where J is the frame length. The elements in $\boldsymbol{c}_k$ are referred to as coded bits. Then, $\boldsymbol{c}_k$ is permutated by an interleaver π_k, producing $\boldsymbol{x}_k = [x_k(1), \ldots, x_k(j), \ldots, x_k(J)]^T$. Following the CDMA convention, the elements in

$\boldsymbol{x}_k$ are called “chips”. Users are solely distinguished by their interleavers, hence the name interleave-division multiple-access.

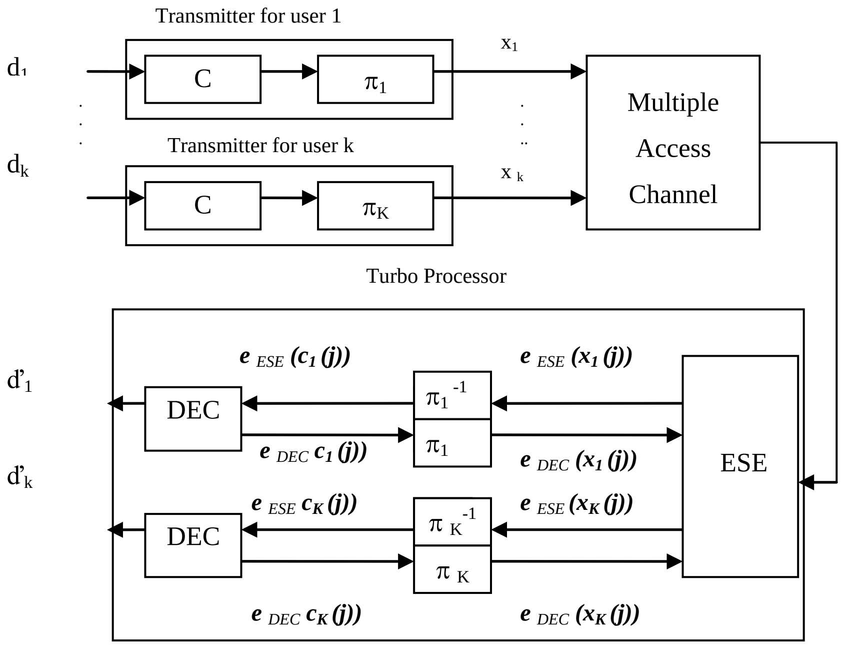

Figure 3.1: Transmitter and (iterative) receiver structures of an IDMA scheme with K simultaneous users [18] [19]

An iterative sub-optimal receiver structure, as illustrated in Fig. 1, consists of an elementary signal estimator (ESE) and K single-user *a posteriori* probability (APP) decoders (DECs). The multiple access and coding constraints are considered separately in ESE and DECs. The outputs of the ESE and DECs are extrinsic log-likelihood ratios (LLRs) about $\{x_k(j)\}$ defined below [2] [20] [21]:

$$e(x_K(j)) \equiv \log\left(\frac{\Pr(x_k(j)=+1)}{\Pr(x_k(j)=-1)}\right), \qquad \forall k, j. \tag{3.1}$$

These LLRs are further distinguished by subscripts, i.e. $e_{ESE}(x_k(j))$ *and* $e_{DEC}(x_k(j))$, depending on whether they are generated by the ESE or DECs. A global turbo type iterative process is then applied to process the LLRs generated by the ESE and DECs.

3.3 The Basic ESE Function

Considering that the channel has no memory. After chip-matched filtering, the received signal from *K* users can be written as

$$r(j) = \sum_{k=1}^{K} h_k x_k(j) + n(j), \qquad \text{j=1, 2, 3 …., J} \qquad (3.2)$$

Where h_k is the channel coefficient for user-*k* and $\{n\ (j)\}$ are samples of an AWGN process with variance $\sigma^2 = N_0/2$. The channel coefficients $\{h_k\}$ are known *a priori* at the receiver. Due to the use of random interleavers $\{\pi_k\}$, the ESE operation can be carried out in a chip-by-chip manner, with only one sample $r(j)$ used at a time. Rewrite (3.2) as

$$r(j) = h_k x_k(j) + \zeta_k(j) \qquad (3.3a)$$

Where

$$\zeta_k(j) \equiv r(j) - h_k x_k(j) = \sum_{k'=k} k_{k'} x_{k'}(j) + n(j) \qquad (3.3b)$$

is the distortion (including interference-plus-noise) in $r\ (j)$ with respect to user-*k*. From the central limit theorem, $\zeta_k(j)$ can be approximated as a Gaussian variable, and $r\ (j)$ can be characterized by a conditional Gaussian probability density function,

$$p(r(j) \mid x_k(j) = \pm 1 = \frac{1}{\sqrt{2\pi Var(\zeta_k(j)}} \exp\left(- \frac{(r(j) - (\pm h_k + E(\zeta_k(j))))^2}{2Var(\zeta_k(j))} \right) \qquad (3.4)$$

where E(·) and Var(·) are the mean and variance functions, respectively.

The following is a list of the ESE detection algorithm based on (3.2)-(3.4) [21], assuming that the *a priori* statistics $\{E(x_k(j))\}$ and $\{Var(x_k(j))\}$ are available [19].

Algorithm 1. Chip-by-Chip Detection in a Single-Path Channel

Step (i): Estimation of Interference Mean and Variance

$$E(r(j)) = h_k E(x_k(j)), \tag{3.5a}$$

$$Var(r(j)) = \sum_k |h_k|^2 Var(x_k(j)) + \sigma^2, \tag{3.5b}$$

$$E(\zeta_k(j)) = E(r(j)) - h_k E(x_k(j)), \tag{3.5c}$$

$$Var(\zeta_k(j)) = Var(r(j)) - |h_k|^2\, Var(x_k(j)), \tag{3.5d}$$

Step (ii): LLR Generation

$$e_{ESE}(x_k(j)) = 2h_k.\frac{r(j) - E(\zeta_k(j))}{Var(\zeta_k(j))}, \tag{3.6}$$

Comments

1. Assuming independent $\{x_k\ (j)\}$, (3.5) is a straightforward consequence of (3.2) and (3.3b).
2. Step (ii) is obtained by evaluating (3.1) based on (3.4).
3. Algorithm 1 is an extremely simplified form of that derived in [22] when the spreading sequences are all of length-1.
4. The cost in (3.5a) and (3.5b), i.e., generating $E(r(j))$ and $Var(r(j))$, are shared by all users, costing only three multiplications and two additions per coded bit per user. Overall, the ESE operations in (3.5) - (3.6) cost only seven multiplications and five additions per coded bit per user, which is very modest. Interestingly, the cost per information bit per user is independent of the number of users K. This is considerably lower than that of other alternatives.

For example, the well-known Minimum Mean Squared Error (MMSE) algorithm in [23] has complexity of $O\ (K^2)$.

3.4 The ESE Function for Multi-Path Channels

Now consider the ESE function in a quasi-static multi-path fading channel with memory length L-1. Let {h $_{k,0,\ldots\ldots,}h_{k,L-1}$ } be the fading coefficients related to user-k. After chip-matched filtering, the received signal can be represented by [19].

$$r(j) = \sum_{k=1}^{K}\sum_{l=0}^{L-1} h_{k,l}x_k(j-l) + n(j), \qquad \text{j=1 , 2…, J+L-1.} \tag{3.7}$$

$$r(j+l) = h_{k,l}x_k(j) + \zeta_{k,l}(j) \tag{3.8a}$$

Where

$$\zeta_{k,l}(j) = r(j+l) - h_{k,l}x_k(j) \tag{3.8b}$$

The similarity between (3.8a) and (3.3a) is clearly seen.

Algorithm 2: Chip-by-Chip Detection in a Multi-Path Channel

Assume again BPSK signaling and real channel coefficients. Algorithm 2 is an extension of Algorithm 1.

Step (i): Estimation of Interference Mean and Variance [19]

$$E(r(j)) = \sum_{k,l} h_{k,l}E(x_k(j-l)), \tag{3.9a}$$

$$Var(r(j)) = \sum_{k,l} |h_{k,l}|^2\ Var(x_k(j-l)) + \sigma^2, \tag{3.9b}$$

$$E(\zeta_{k,l}(j)) = E(r(j+l)) - h_{k,l}E(x_k(j)), \tag{3.9c}$$

$$Var(\zeta_{k,l}(j)) = Var(r(j+l) - |\,h_{k,l}\,|^2\ Var(x_k(j)), \tag{3.9d}$$

Step (ii): LLR Generation and Combining [19]

$$e_{ESE}(x_k(j))_l = 2h_{k,l}.\frac{r(j+l) - E\left(\zeta_{k,l}(j)\right)}{Var\left(\zeta_{k,l}(j)\right)}, \tag{3.10a}$$

$$e_{ESE}(x_k(j)) = \sum_{l=0}^{L-1} e_{ESE}(x_k(j))_l. \tag{3.10b}$$

Comments:

1. It is easy to see the connection between (3.9) and (3.5).
2. From (3.7), each $x_k(j)$ observed on L successive samples $\{r(j), r(j+1),$ (10a)$\ldots, r(j+L-1)\}$. Assume that the distortion terms with respect to $x_k(j)$ in these L samples, i.e. $\{\zeta_{k,0}(j), \zeta_{k,1}(j), \ldots, \zeta_{k,L-1}(j)\}$, are un-correlated. Then the overall *a posteriori* probabilities for $x_k(j) = \pm 1$ are the products of the individual *a posteriori* probabilities generated from $\{r(j), r(j+1), \ldots, r(j+L-1)\}$. Hence the LLRs for $x_k(j)$ can be directly summed as in (3.10b). This LLR combining (LLRC) technique is similar to the rake operation used in CDMA.
3. The overall complexity is approximately L times that of Algorithm 1.

The un-correlation assumption mentioned above is only an approximate, but it greatly simplifies the matter. The complexity (per coded bit per user) for Algorithm 2 is $O(L)$. There are other alternative treatments for channels with memory. One is the joint Gaussian (JG) technique [23] that takes into consideration the correlation among $\{\zeta_{k,0}(j), \zeta_{k,1}(j), \ldots, \zeta_{k,L-1}(j)\}$. This technique leads to improve performance but also increase cost ($O(L^2)$). Another alternative is the maximum ratio combining (MRC) technique [21], in which $\boldsymbol{r} = \{r_j\}$ is passed through K MRC filters, each matched to the L tap-coefficients for a particular user. MMSE detection is then applied to generate $\{e_{ESE}(x_k(j))\}$. The related complexity is $O(KL)$ [17].

Generally speaking, the JG technique demonstrates better performance but this becomes noticeable only when the number of users is very large or when the rate of C is high. Overall, the LLRC method is a good compromise between complexity and performance.

3.5 The ESE Function for More Complex Channels

Now, the case of more complex situations is considered. Superscripts $^{\text{“Re”}}$ and $^{\text{“Im”}}$ or function notations Re (.) and Im (.) are used to indicate real and imaginary parts, respectively. Consider quadrature-phase-shift-keying (QPSK) signaling [19],

$$x_k(j) = x_k^{\text{Re}}(j) + i x_k^{\text{Im}}(j), \tag{3.11}$$

where $i = (-1)^{½}$, $x_k^{Re}(j)$ and $x_k^{Im}(j)$ are two coded bits from $\boldsymbol{c}_k$.. For convenience, the elements in $\boldsymbol{x}_k$ are called “chips”. In this case, each chip contains two coded bits. Channel model (3.7) is adopted and expanded using complex channel coefficients $\{h_{k,l} = h_{k,l}^{Re} + h_{k,l}^{Im}\}$ as [19]:

$$r(j) = \sum_{k,l}\left(h_{k,l}^{\text{Re}} x_k^{\text{Re}}(j-l) - h_{k,l}^{\text{Im}} x_k^{\text{Im}}(j-l)\right) + i\sum_{k,l}\left(h_{k,l}^{\text{Re}} x_k^{\text{Im}}(j-l) + h_{k,l}^{\text{Im}} x_k^{\text{Re}}(j-l)\right) + n(j) \tag{3.12}$$

Where $\{n(j)\}$ are samples of a complex AWGN process with variance σ^2 per dimension. Denote by $h_{k,l}$, the conjugate of $h_{k,l}$. Recall (3.8): $r(j+l) = h_{k,l}\, x_k(j) + \zeta_{k,l}(j)$. The phase shift due to $h_{k,l}$ is cancelled out in $h_{k,l}\, r(j+l)$, which means that Im $(h_{k,l}\, r(j+l))$ is not a function of $x_k^{Re}(j)$. Therefore the detection of $x_k^{Re}(j)$ only requires [19]

$$\text{Re}\left(\overline{h_{k,l}}\, r(j+l)\right) = |\, h_{k,l}\,|^2\ x_k^{\text{Re}}(j) + \text{Re}\left(\overline{h_{k,l}}\,\zeta_{k,l}(j)\right), \tag{3.13}$$

Algorithm 3 below outlines the procedure to estimate $x_k^{Re}(j)$ based on (3.13) [19].

Algorithm 3. Chip-by-Chip Detection in a Complex Multi-Path Channel

Step (i): Estimation of Interference Mean and Variance

$$E(r^{\text{Re}}(j)) = \sum_{k,l}\left(h_{k,l}^{\text{Re}} E(x_k^{\text{Re}}(j-l)) - h_{k,l}^{\text{Im}} E(x_k^{\text{Im}}(j-l))\right), \tag{3.14a}$$

$$E(r^{\mathrm{Im}}(j)) = \sum_{k,l}\left(h_{k,l}^{\mathrm{Re}}E(x_k^{\mathrm{Im}}(j-l)) - h_{k,l}^{\mathrm{Im}}E(x_k^{\mathrm{Re}}(j-l))\right), \tag{3.14b}$$

$$Var(r^{\mathrm{Re}}(j)) = \sum_{k,,l}\left((h_{k,l}^{\mathrm{Re}})^2 Var(x_k^{\mathrm{Re}}(j-l)) + (h_{k,l}^{\mathrm{Im}})^2 Var(x_k^{\mathrm{Im}}(j-l))\right) + \sigma^2, \tag{3.14c}$$

$$Var(r^{\mathrm{Im}}(j)) = \sum_{k,,l}\left((h_{k,l}^{\mathrm{Im}})^2 Var(x_k^{\mathrm{Re}}(j-l)) + (h_{k,l}^{\mathrm{Re}})^2 Var(x_k^{\mathrm{Im}}(j-l))\right) + \sigma^2, \tag{3.14d}$$

$$\psi(j) = \sum_{k,l} h_{k,l}^{\mathrm{Re}} h_{k,l}^{\mathrm{Im}} (Var(x_k^{\mathrm{Re}}(j-l)) - Var(x_k^{\mathrm{Im}}(j-l))), \tag{3.15}$$

$$E\left(\mathrm{Re}\left(\overline{h_{k,l}}\zeta_{k,l}(j)\right)\right) = h_{k,l}^{\mathrm{Re}} E\left(r^{\mathrm{Re}}(j+l)\right) + h_{k,l}^{\mathrm{Im}} E\left(r^{\mathrm{Im}}(j+l)\right) - |\, h_{k,l}\,|^2\ E(x_k^{\mathrm{Re}}(j)), \tag{3.16a}$$

$$\begin{aligned} Var\left(\mathrm{Re}\left(\overline{h_{k,l}}\zeta_{k,l}(j)\right)\right) &= \left(h_{k,l}^{\mathrm{Re}}\right)^2 Var\left(r^{\mathrm{Re}}(j+l)\right) + \left(h_{k,l}^{\mathrm{Im}}\right)^2 Var\left(r^{\mathrm{Im}}(j+l)\right) \\ &+ 2h_{k,l}^{\mathrm{Re}} h_{k,l}^{\mathrm{Im}} \psi(j+l) - |\, h_{k,l}\,|^{4V}\ Var\left(x_k^{\mathrm{Re}}(j)\right) \end{aligned} \tag{3.16b}$$

Step (ii): LLR Generation and Combining

$$e_{ESE}(x_k^{\mathrm{Re}}(j))_l = 2\,|\, h_{k,l}\,|^2 \cdot \frac{\mathrm{Re}\left(h_{k,l} r(j+l)\right) - E\left(\mathrm{Re}\left(h_{k,l}\zeta_{k,l}(j)\right)\right)}{Var\left(\mathrm{Re}\left(\overline{h_{k,l}}\zeta_{k,l}(j)\right)\right)}, \tag{3.17a}$$

$$e_{ESE}(x_k^{\mathrm{Re}}(j)) = \sum_{l=0}^{L-1} e_{ESE}(x_k^{\mathrm{Re}}(j))_l. \tag{3.17b}$$

Comments:

1. Obtain (3.14a)–(3.14d) using (3.12) and obtain (3.16a) as follows (based on (3.8) and (3.13)),

   $$\mathrm{Re}\left(\overline{h_{k,l}}\zeta_{k,l}(j)\right) = h_{k,l}^{\mathrm{Re}} r^{\mathrm{Re}}(j+l) + h_{k,l}^{\mathrm{Im}} r^{\mathrm{Im}}(j+l) - |\, h_{k,l}\,|^2\ x_k^{\mathrm{Re}}(j). \tag{3.18}$$

2. It can be verified that ψ(*j*) in (3.15) is the covariance of $r^{\mathrm{Re}}(j)$ and $r^{\mathrm{Im}}(j)$. It is introduced for cost saving since it is shared by all users, costing *L* multiplications and *L*/2 additions per coded bit per user.
3. A similar procedure can be used to estimate $x_k^{\mathrm{Im}}(j)$ based on {Im ($h_{k,l}\, r(j+l)$), $l = 0,\ldots, L-1$}.
4. If the cost related to ψ(*j*) is ignored, the complexity of Algorithm 3 per coded bit per user is approximately two times of that of Algorithm 2. It slightly

increases by several additions and multiplications considering $\psi(j)$ but is still $O(L)$ [19].

3.6 The ESE Function for Channels with Multiple Receive Antennas

The above principles can be easily generalized to channels with multiple receive antennas. The signals from each receive antenna can be treated as those from a set of independent paths. The LLRC technique can be directly applied.

3.7 The DEC Function

The DECs in Figure 3.1 carry out APP decoding using the output of the ESE as the input. With BPSK signaling, their output is the extrinsic LLRs {e_{DEC} $(x_k$ $(j))$ of {x_k (j) defined in (3.1), which are used to generate the following statistics [19]

$$E(x_k(j)) = \tanh(e_{DEC}x_k(j))/2, \tag{3.19a}$$

$$Var(x_k(j)) = 1-(E(x_k(j)))^2. \tag{3.19b}$$

(With QPSK signaling, the DEC outputs are the extrinsic LLRs for $\{x_k^{\mathrm{Re}}(j)\}$ and $\{x_k^{\mathrm{Im(}}(j)\}$. As discussed above, {E $(x_k$ $(j))$} and {Var $(x_k$ $(j))$} will be used in the ESE to update the interference mean and variance in the next iteration [19].

APP decoding is a standard operation [11]. A special case of C that is formed by serially concatenating a Forward Error Correction (FEC) sub-codeC_{FEC} (same for every user) and a length-S repetition code C_{REP} is considered. This scheme is not optimized from performance point of view, as the repetition code is actually a poor spreading code. However, this structure does have the advantage of flexibility regarding the rate.

The input data sequence of each user is first encoded by C_{FEC}, generating $\{b_k(i), i = 1, 2 \ldots\}$. Then each $b_k(i)$ is repeated S times by C_{REP}, producing $\{c_k(j)\}$. For simplicity, the focus is on those replicas related to $b_k(1)$, i.e., $\{c_k(j), j = 1, 2, \ldots, S\}$. The treatment for replicas of $b_k(i)$ with $i > 1$ is similar.

The DEC for C carries out the following operations assuming BPSK modulation [19].

Obtain the estimate of each $b_k(i)$ based on $\{e_{ESE}(x_k(j))\}$ from the ESE. Assume that $\{e_{ESE}(x_k(j)), \forall . j\}$ are un-correlated (which is approximately true due to interleaving). Since, we have $c_k(j) = x_k(\pi_k(j))$, the *a posteriori* LLR for $b_k(1)$ can be computed from $\{e_{ESE}(x_k(j))\}$ as [17].

$$L(b_k(1) = \sum_{j=1}^{S} \log\left(\frac{\Pr\left(x_k(\pi_k(j)) = +1 \mid r(\pi_k(j))\right)}{\Pr\left(x_k(\pi_k(j)) = -1 \mid r(\pi_k(j))\right)}\right) = \sum_{j=1}^{S} e_{ESE}(x_k(\pi_k(j))). \tag{3.20}$$

Perform standard APP decoding for *CFEC* using $\{L(b_k(i))\}$ as the input, and generate the *posteriori* LLRs $\{L_{APP}(b_k(i))\}$ for $\{b_k(i)\}$.

$c_k(j) = b_k(1)$ for $j = 1, \ldots, S$.

Compute

$$e_{DEC}(x_k(\pi_k(j))) = e_{DEC}(c_k(j)) = L_{APP}(b_k(1)) - e_{ESE}(x_k(\pi_k(j))), \quad \text{j=1,…, S.} \qquad (3.21a)$$

The subtraction above ensures that $e_{DEC}(x_k(\pi_k(j)))$ is extrinsic.[11]

Alternatively, we can use an approximation of (21a),

$$e_{DEC}(x_k(\pi_k(j))) \approx L_{APP}(b_k(1)), \qquad \text{j=1, …, S.} \qquad (3.21b)$$

In this way, all the replicas of $b_k(i)$ have the same feedback from the DEC, so the memory usage can be greatly reduced (since we only need to store $\{L_{APP}(b_k(i))\}$ instead of $\{e_{DEC}(x_k(j))\}$). Eqn. (3.21b) may lead to certain performance loss compared with (3.21a) [19].

3.8 The Cost of the Overall Receiver

The DEC cost of a cascade *CFEC* /*CREP* structure studied in the previous Section is dominated by the APP decoding cost for *CFEC*, as the additional cost involved in (3.20) and (3.21) are usually marginal. In particular, suppose that a turbo type code is used as *CFEC*. Then even a single-user detector would involve iterative processing with APP decoding. In this case, the extra cost for the multi-user detector described above is mainly related to the ESE, which, as we have seen, is very modest. The overall complexity of the multiuser detector can be roughly comparable to that of a single-user one. (The exact ratio depends on the cost ratio between the ESE and APP decoding).

3.9 Conclusion

A new multi user scheme named IDMA has been introduced. It allows very low-cost multiuser detection. The basic principle is to use interleavers for user separation. A very large number of users can be processed with modest computing power. Multipath is no longer a serious issue as far as complexity is concerned. Near Shannon capacity performance is observed for multiple access channels.

Chapter 4

4G FEATURES OF IDMA

4.1 Introduction

In 2003, ITU formulated recommendations for 4G mobile communication systems. According to these recommendations, 4G systems are expected to be exceedingly efficient and adaptive exhibiting high bandwidth and power efficiency in addition to low transceiver complexity. They are also required to be flexible with respect to data rate (link adaptation), data reliability (QoS), and service provisioning as well as capable of operating on frequency-selective and fast-fading channels. In this chapter we address the goals mentioned above and demonstrate how they can be effectively realized by IDMA based 4G uplink proposal.

4.2 IDMA based 4G Uplink Proposal

The proposed transmitter and receiver structure [25] are shown in Fig. 4.1.

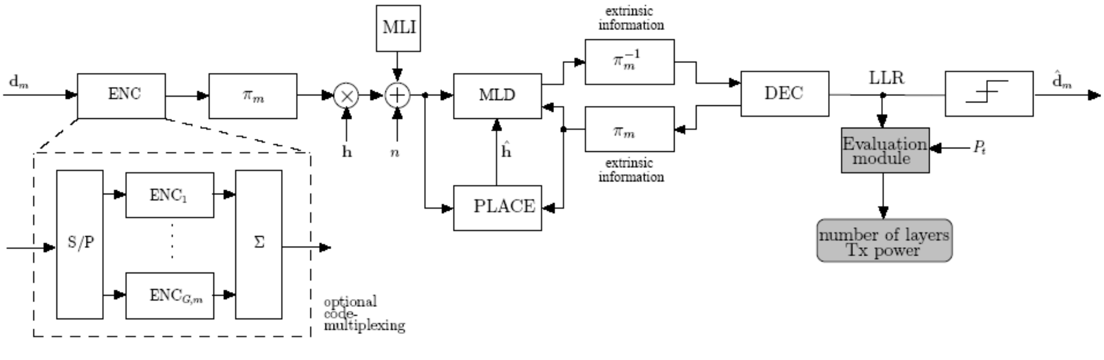

Figure 4.1: IDMA based system proposal (*m*-th layer) [28]

First of all, the data stream of user U_i is partitioned into layers of equal lengths. The data of the *m*-th layer is denoted as d_m, $1 \leq m \leq M$, where M is the number of active layers. All layers are separately encoded by the same FEC encoder and spreader. Then, layer-specific interleaving is done by a chip-by-chip interleaver π_m. Assuming a linear channel, the impact of the transmission channel can completely be represented by a vector $\boldsymbol{h} = [h_0,........,h_L]$, where h_ℓ denotes the ℓ-th (possibly time-varying) coefficient of the equivalent discrete-time ISI channel model, and L denotes the effective memory length.

At the receiver side the individual layers, which are experiencing Multilayer Interference (MLI), are detected by a low complexity Multilayer Detector (MLD). An iterative (turbo-like) receiver that exchanges extrinsic information between the MLD and the decoder (DEC) can be applied. This receiver structure is nearly optimal, of low complexity, and provides reliable soft outputs. The MLD uses channel estimates delivered by a Pilot-Layer Aided Channel Estimator (PLACE) [28]. When the log-likelihood values from the *m*-th layer are passed by the decoder after the last iteration, an evaluation module is used to calculate an estimate of the Bit Error Rate (BER) of the *m*-th layer. The BER estimate is used for soft link adaptation.

4.2.1 Soft Link Adaptation

An advantage of the low-cost IDMA-receiver considered in [26] is the inherent reliability of soft output information. In [11] an adaptation strategy based on the soft outputs is described. Besides delivering hard decisions after the final iteration, the receiver in Fig. 4.1 calculates estimates of the BER in an evaluation module. The evaluation module compares the estimated BER with the predefined target BER *Pt*. Since the BER degrades with increasing number of layers because of increased MLI, the number of layers transmitted in the next block is decreased at the transmitter side if the estimated BER is higher than the target BER. If the estimated BER is below the target BER, the transmission power can be reduced. It was shown in [27] that the proposed iterative receiver is appropriate for the suggested adaption strategy.

4.2.2 Quality of Service (QoS)

QoS is mainly defined by a maximum bit error rate, a minimum data rate, and a maximum delay (especially for packet based services). These parameters are highly dependent on the application, e.g. text message, voice transmission or video transmission. IDMA-based systems can be made highly adaptive in order to guarantee a certain QoS level. Hence, we do not seek quasi error-free transmission, but apply the soft link adaption strategy to guarantee a certain bit error rate for a layer or group of layers allocated to a user or application.

The bit error rate that can be tolerated is application-dependent, e.g. voice transmission allows higher bit error rates than data transmission. Instead of using adaptive modulation and/or channel coding, in IDMA the number of layers and the transmission power are modified to meet this requirement. The number of layers used for transmission can be reduced if the data rate is higher than needed or, if the data rate cannot be reduced for QoS reasons, the transmit power can be increased until the target BER is achieved.

The data rate is an essential QoS parameter, for example text messaging services need much lower data rates than video transmission. The data rate is adapted in a similar way as the target BER is. With a higher number of layers assigned to a user, its data rate is higher. To ensure a certain BER the power can be adapted as well.

In some applications, e.g. real-time speech transmission, a large delay is very inconvenient, in other applications even critical, e.g. packet loss in TCP based networks. To achieve small delays, the block length for IDMA transmission can be chosen to be quite small. This is possible because the chip-by-chip interleaving is done.

4.2.3 Extension of Pure IDMA

In [27] it is shown how to improve the error performance of IDMA by means of a hybrid scheme with orthogonal code multiplexing and IDMA (OCDM/IDMA). An optional extension of IDMA based on this approach is depicted in Fig. 4.1. The data stream of one user is parallelized in multiple layers. Different encoders are used for the single layers. All layers of one user share one interleaver.

It is also possible to perform the spreading over multiple sub-carriers to obtain a Multi-carrier IDMA (MC-IDMA) system. This is an interesting alternative to IDMA for systems with a huge number of sub-carriers, or an extension of existing or planned MC-CDMA systems.

4.2.4 Multiple Antenna Systems

Multiple antenna systems are a key technology for 4G. In [22] IDMA has been extended to multiple antennas with good results. The extension of IDMA to Multiple Input Multiple Output (MIMO) systems is easy because the superposition of the different layers at the transmitter side and their separation at the receiver side is done anyway. Therefore, neither special design is needed nor further increase in complexity is caused.

4.2.5 Pilot-Layer Aided channel Estimation

Channel estimation is an important task for at least two reasons: Maximizing the data rate implies that we want to operate as close as possible to the channel capacity in all fading conditions. Secondly, reliable channel estimates are required in order to obtain meaningful reliability values at the output of the Chip Reliability Estimator (CRE) even after many iterations. Channel estimation is particularly difficult for time varying channel conditions.

In order to solve all these requirements, a novel channel estimation scheme called PLACE is proposed [28]. For each user the first layer carries training symbols, which are known at the receiver. Therefore, this layer is referred to as the *training layer*. (Some symbols of the training layer may carry info bits or signaling bits (such as the number of active layers). For reasons of simplicity, however, we assume a pure training layer in the following.) This training layer is proposed to be transmitted continuously. This is particularly helpful in the acquisition phase and for resynchronization after a deep fade. The data layers are linearly superimposed, depending on the pre-defined QoS and the current channel condition. PLACE is similar to the burst structure of the uplink dedicated physical channel in UMTS. In the latter case, however, training data (and control information) are carried in the quadrature component, whereas the information bits are carried in the in phase component. PLACE is also similar to superimposed pilot-aided channel estimation. It is anticipated that due to the chip-by-chip processing fast fading channels can be tracked.

4.3 Conclusion

In this chapter, an IDMA-based system proposal for the 4G uplink is presented. Some requirements and possible characteristics of the 4G uplink are discussed along with the ability of IDMA to meet them. The main advantages of IDMA are its low complexity, high bandwidth and power efficiency, and excellent adaptivity. Besides soft link adaptation, the reliable soft outputs generated by the receiver enables a wide range of possible applications like soft channel decoding, iterative schemes and other information combining technologies. Further improvements are expected from the straight forward extension to key technologies like MIMO and MC technologies, which are currently considered for 4G systems.

Chapter 5

SIMULATION TESTBED FOR IDMA IMPLEMENTED IN SIMULINK

5.1 Introduction

This chapter provides the implementation algorithm and details of entire IDMA system built using SIMULINK. System is modeled to curtail processing delays and develop a software test bed. This test bed can be used to study the performance of IDMA system with variation in system parameters and channel conditions.

A block diagram type simulator is more convenient than the M-files of MATLAB to build and simulate communication systems. Such tools have an environment where blocks corresponding to different algorithms are available in a library and can be connected to form a system. SIMULINK uses the MATLAB engine for simulations and has a substantial library of functions for communication systems.

5.2 Flexibility of SIMULINK

Computers have provided engineers with immense mathematical powers, which can be used to simulate (or mimic) dynamic systems without the actual physical system. Simulation of dynamic systems has been proven to be immensely useful when it comes to system modeling and control design. This is because it saves the time and money that would otherwise be spent in prototyping a physical system. SIMULINK is a software add-on to MATLAB which is a mathematical tool developed by Mathworks. MATLAB is powered by extensive numerical analysis capability. SIMULINK is a tool used to visually program a dynamic system (those governed by Ordinary Differential equations) and look at results. Any logic circuit or a control system for a dynamic system can be built by using standard building blocks available in SIMULINK Libraries. Various toolboxes for different techniques, such as Fuzzy Logic, Neural Networks, Digital Signal Processing, Statistics etc. are available in SIMULINK, which enhance the processing power of the tool. The main advantage is the availability of templates / building blocks, which avoid the necessity of typing code for various mathematical processes.

In SIMULINK, data/information from various blocks is sent to another block by lines connecting the relevant blocks. Signals can be generated and fed into blocks (dynamic / static). Data can be fed into functions. Data can then be dumped into sinks which could be virtual oscilloscopes, displays or could be saved to a file. Data can be connected from one block to another, can be branched, multiplexed etc. In simulation, data is processed and transferred only at discrete times, since all computers are discrete systems. Thus, a simulation time step (otherwise called an integration time step) is essential, and the selection of that step is determined by the fastest dynamics in the simulated system.

5.3 IDMA Transmitter Structure

The IDMA transmitter structure is shown in Fig. 5.1. For clarity, SIMULINK transmitter model for only three users is depicted (K=3). At this end , the *n*th bit $d_n^{(k)} \in \{+1,-1\}$, $n = 1, 2, \ldots, 64$, in the input data stream $d^{(k)}$, from user-k is spread using a length-16 spreading sequence $s^{(k)}$ in the form $d_n^{(k)} \rightarrow d_n^{(k)} s^{(k)}$. We write the chip sequence obtained after spreading as $\{c_j^{(k)}, j = 1, 2, \ldots, 1024\}$ where $J = (N \text{ x } S)$ = (64 x 16) =1024 is the frame length. A chip-level interleaver $\pi^{(k)}$ is then applied to produce the transmitted signals $\{x_j^{(k)}, j = 1, 2, \ldots, 1024\}$. Removing the interleaver $\pi^{(k)}$ in Fig. 1 leads to a conventional CDMA scheme, in which different signature sequences $\{s^{(k)}, k = 1, 2, \ldots, K\}$ are employed for user separation. Conversely, in

IDMA scheme, a common spreading sequence is used for all users $\{s^{(1)} = s^{(2)} = \ldots\ldots\ldots\ldots = s^{(k)} = \ldots\ldots = s^{(K)} = s\}$ and user-specific interleavers $\{\pi^{(k)}, k = 1, 2, \ldots\ldots\ldots, K\}$ are employed for user separation.

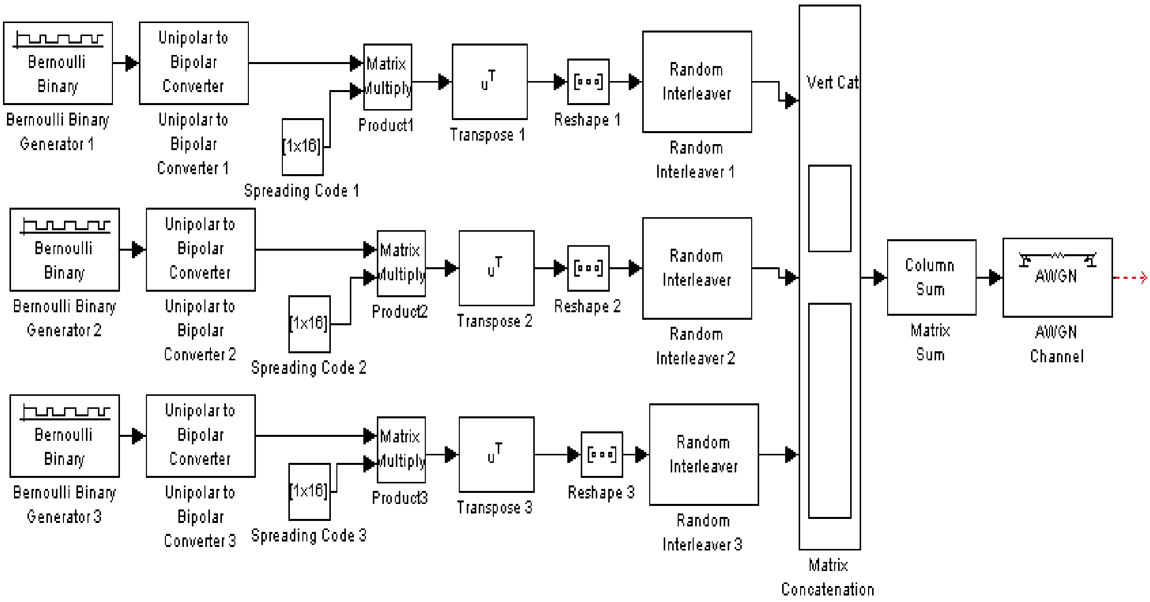

Figure 5.1: SIMULINK model of IDMA transmitter

For simplicity, we only consider synchronous BPSK systems over a time-invariant single-path channel. The received signal at time instant *j* can be written as:

$$r(j) = \sum_{k=1}^{K} h_k x_k(j) + n(j) \qquad j=1, 2, 3 \ldots, 1024 \qquad (5.1)$$

Here, $x_j^{(k)} \in \{+1,-1\}$ denotes the transmitted chip from user-*k* at time instant *j*, $h^{(k)}$ the channel coefficient for user-*k* and n_j zero-mean additive white Gaussian noise (AWGN) with variance $\sigma^2 = N_0/2$. $h^{(k)}$ represents the combined effect of power control and channel loss. In light of Shannon's Theorem of channel capacity [11], IDMA allocates unequal power to each user to minimize BER and maximize channel capacity. Perfect knowledge of channel coefficients at the receiver is assumed. To simplify implementation only real channel coefficients $\{h^{(k)}\}$ are considered but the principle can be extended to situations with complex channel coefficients. Table 5.1 shows the energy level assignments for uncoded IDMA system with BPSK modulation and AWGN channel (system parameters are: No. of users=64, Spreading Length=16) [29]. The SIMULINK block of power allocation is shown in Figure 5.2

Table 5.1: Relative Power Levels for IDMA system

User Number	Power Level (dB)
24	0
12	7.976
2	9.116
8	13.6738
4	14.813
6	19.37
8	20.51

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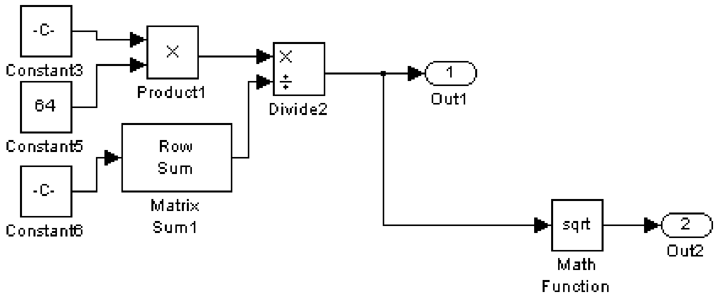

Figure 5.2: Unequal Power Allocation Block

5.4 IDMA Receiver Structure

The iterative chip-by-chip receiver consists of an elementary signal estimator (ESE) and a bank of K single-user *a posteriori* probability decoders (DECs) for the dispreading operation working in a turbo-type manner. The ESE performs a coarse chip-by –chip estimation. The outputs of the ESE are initially noisy but an iterative technique is applied to improve the estimation. The global process starts from the ESE. At the beginning, if no *a priori* information is available, the means and variances of all of the transmitted chips are initialized to zero and one, respectively.

This simply means that each chip takes +1 and -1 with equal probability (assuming binary signaling over {+1, –1}). The ESE then produces coarse estimates as follows. Rewriting Eq.5.1:

$$r_j = h^{(k)} x_j^{(k)} + \zeta_j^{(k)} \quad (5.2)$$

where $\zeta_j^{(k)}$ is the distortion (including both interference and additive noise) contained in r_j with respect to $x_j^{(k)}$. The distortion component $\zeta_j^{(k)}$ is the summation of the received signals from other $K - 1$ users (except user k) plus noise. Based on the assumption that these signals are random and independent of each other, $\zeta_j^{(k)}$ can be approximated by a Gaussian random variable for a large K, using the central limit theorem. The ESE operations to estimate $x_j^{(k)}$ are listed in Table 5.2.

Table 5.2: Operations of Elementary Signal Estimator (ESE)

STEP 1	Estimate mean of r_j	$\mathrm{E}(r_j) = \sum_{k=1}^{K} h^{(k)} \mathrm{E}(x_j^{(k)})$
STEP 2	Estimate variance of r_j	$\mathrm{Var}(r_j) = \sum_{k=1}^{K} \lvert h^{(k)}\rvert^2 \mathrm{Var}(x_j^{(k)}) + \sigma^2$
STEP 3	Estimate mean of $\zeta_j^{(k)}$	$\mathrm{E}(\zeta_j^{(k)}) = \mathrm{E}(r_j) - h^{(k)} \mathrm{E}(x_j^{(k)})$
STEP 4	Estimate variance of $\zeta_j^{(k)}$	$\mathrm{Var}(\zeta_j^{(k)}) = \mathrm{Var}(r_j) - \lvert h^{(k)}\rvert^2 \mathrm{Var}(x_j^{(k)})$

STEP 5	Estimate $x_j^{(k)}$	L($x_j^{(k)}$)= 2$h^{(k)}$ ((r_j) - E($\zeta_j^{(k)}$)) / Var($\zeta_j^{(k)}$)

SIMULINK blocks of mean / variance estimation of r_j and calculation of L($x_j^{(k)}$) are shown in Fig. 5.3 and 5.4 respectively.

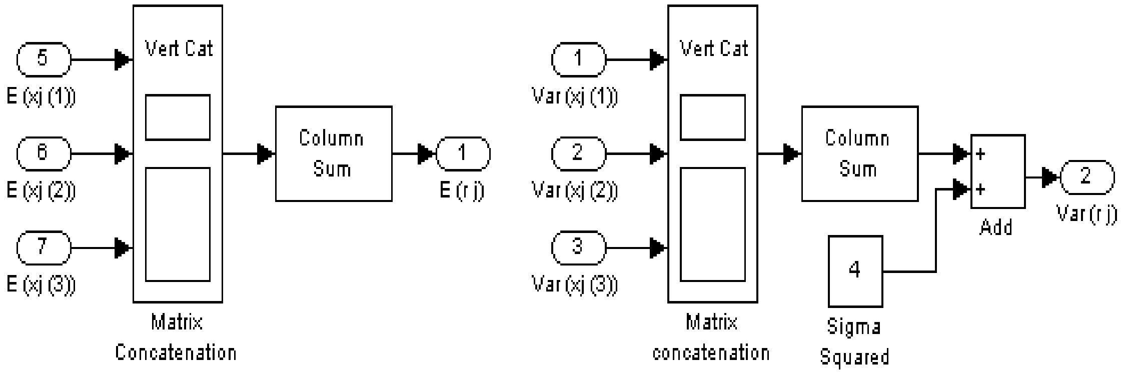

Figure 5.3: Estimating Mean and Variance of r_j

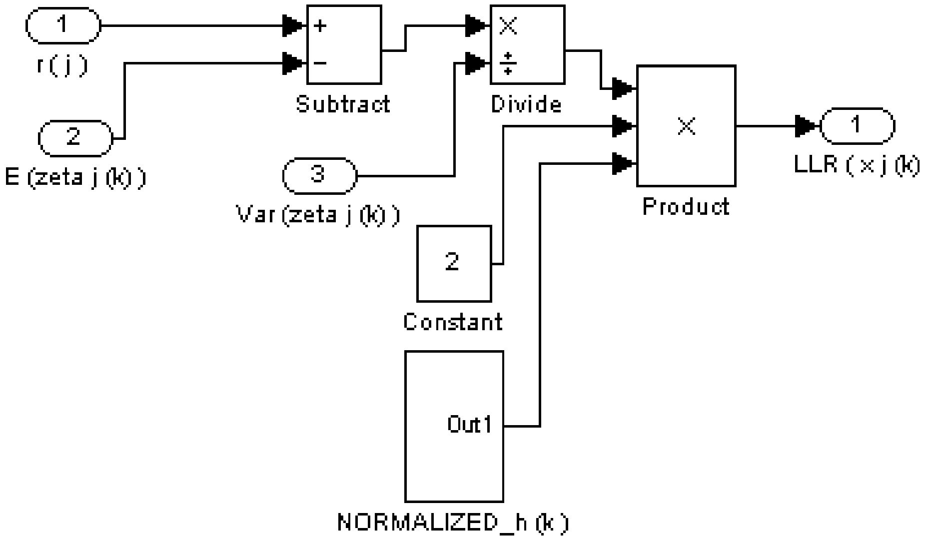

Figure 5.4: Calculation of L($x_j^{(k)}$)

For user-*k*, the corresponding ESE outputs {L ($x_j^{(k)}$), j =1, 2,........., 1024} are de-interleaved to form {L ($c_j^{(k)}$), j =1, 2,........., 1024}and delivered to the DEC for user-*k*. The DEC performs a soft-in/soft-out chip-by-chip de-spreading operation as detailed below.

For simplicity, consider the chips related to $d_1^{(k)}$, the first bit of user-*k*. The rest of the chips are treated similarly. Initially, $d_1^{(k)}$ was spread into the chip sequence $d_1^{(k)} s^{(k)} = \{c_j^{(k)}, j = 1, 2, \ldots, 16\}$ where $s^{(k)} = \{s_j^{(k)}\}$ is the binary signature sequence (over {+1, −1}) for user-*k*. We assume that L ($c_j^{(k)}$) are uncorrelated (which is approximately true due to interleaving). Let the interleaving for user-*k* be expressed as $\pi_{(k)}^{(j)} = j'$, i.e., $c_j^{(k)} = x_{j'}^{(k)}$, Then the *a posteriori* LLR for $d_1^{(k)}$ can be computed using L ($c_j^{(k)}$) as:

$$L(d_1^{(k)}) = \log \left(\frac{\Pr(d_1^{(k)} = +1 | r}{\Pr(d_1^{(k)} = -1 | r} \right) \tag{5.3}$$

$$L(d_1^{(k)}) = \left(\frac{\prod_{j=1}^{S} \Pr(c_j^k = s_j^k | r_j)}{\prod_{j=1}^{S} \Pr(c_j^k = -s_j^k | r_j)} \right) \tag{5.4}$$

$$= \sum_{j=1}^{S} \log \frac{\Pr(c_j^k = s_j^k | r_j)}{\Pr(c_j^k = -s_j^k | r_j)} \tag{5.5}$$

$$L(d_1^{(k)}) = \sum_{j=1}^{S} s_j^{(k)} \, L \, (c_j^{(k)})$$

(5.6)

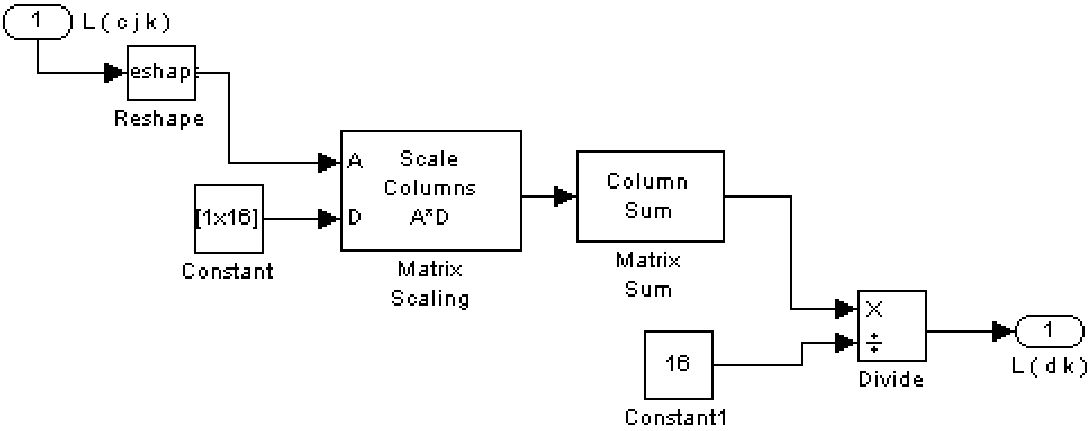

Figure 5.5: Despreading Operation at DECs

The extrinsic LLR for a chip $c_j^{(k)}$ within $d_1^{(k)}\, s^{(k)}$ is defined by:

$$Ext\ (c_j^{(k)}) = \log \left(\frac{\Pr(c_j^k = s_j^k \mid r_j)}{\Pr(c_j^k = -s_j^k \mid r_j)} \right) - \mathrm{L}\ (c_j^{(k)})$$

(5.7)

$c_j^{(k)} = +1$ if $s_j^{(k)} = d_1^{(k)}$ and $c_j^{(k)} = -1$ otherwise. Therefore,

$$Ext\ (c_j^{(k)}) = s_j^{(k)}\ \mathrm{L}(d_1^{(k)}) - \mathrm{L}\ (c_j^{(k)}) \qquad (5.8)$$

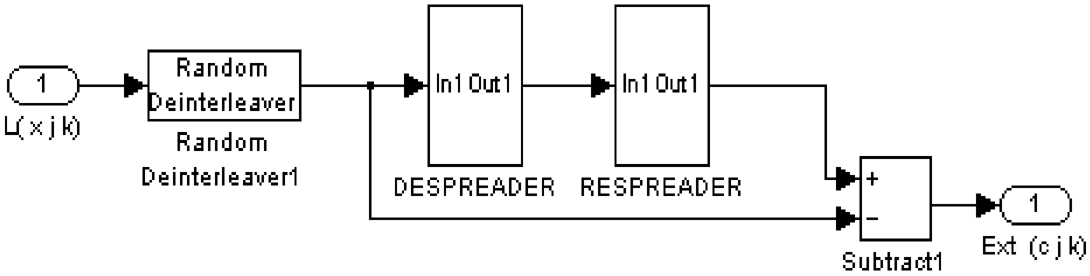

Figure 5.6: Calculation of Extrinsic LLRs

The extrinsic LLRs $\{Ext\,(x_j^{(k)})\}$ form the outputs of the DECs and are fed back to ESE after interleaving. In the next iteration, $\{Ext\,(x_j^{(k)})\}$ are used to update $\{E\,(x_j^{(k)})\}$ and $\{Var\,(x_j^{(k)})\}$ using:

$$E\,(x_j^{(k)}) = \frac{\exp\{Ext\,(x_j^{(k)})\} - 1}{\exp\{Ext\,(x_j^{(k)})\} + 1} = \tanh\left(\frac{Ext\,(x_j^{(k)})}{2}\right) \tag{5.9}$$

$$Var\,(x_j^{(k)}) = 1 - E\,(x_j^{(k)})^2 \tag{5.10}$$

This iterative process is repeated a preset number of times. In the final iteration the DES produces hard decisions on information bits $d^{(k)}$ based on (5.6).

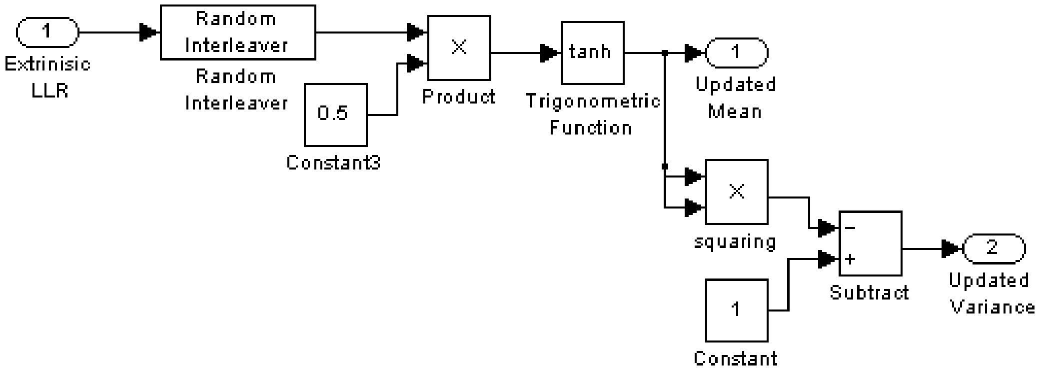

Figure 5.7: Updating the mean and variance

5.5 Conclusion

This Chapter discusses the implementation of entire IDMA system in SIMULINK. Each step of system procedures along with its implementation method in SIMULINK is systematically presented providing an in depth knowledge of the system functions. The developed model can serve as a software test bed for analyzing different properties and testing out the system under various conditions.

Chapter 6

SIMULATION RESULTS

6.1 Introduction

SIMULINK’s Real Time Workshop (RTW) provides the capability to link SIMULINK to any hardware available, thus providing control capability directly from a high-level programming language. This concept, known as Hardware in-the-Loop (HIL) is used extensively in control development. This chapter discusses simulation results of SIMULINK implementation of IDMA and the transferring of the model to any hardware compatible with SIMULINK environment.

6.2 SIMULINK Real Time Workshop

Real Time Workshop automatically generates C code directly from SIMULINK block diagrams. This allows the execution of continuous, discrete-time, and hybrid system models on a wide range of computer platforms, including real time hardware. Real Time Workshop provides a comprehensive set of features and capabilities that provide the flexibility to address the following broad range of applications:

1. As a rapid prototyping tool, Real Time Workshop enables the quick implementation of designs without lengthy hand coding and debugging. Control, Signal Processing, and Dynamic System algorithms can be implemented by developing graphical SIMULINK block diagrams and automatically generating C code.
2. Once a system has been designed in SIMULINK, code for real time controllers or digital signal processors can be generated, cross-compiled,

linked, and downloaded onto selected target processor. The Real Time Workshop supports DSP boards, embedded controllers, and a wide variety of custom and commercially available hardware.

3. Code for an entire system or specified subsystems for hardware in the loop simulations can be created and executed. Typical applications include training simulators (pilot in the loop), real time model validation and testing.
4. Stand-alone simulations can be run directly on the host machine or transferred to other systems for remote execution. Because time histories are saved in MATLAB as binary or ASCII files they can be easily loaded into MATLAB for additional analysis or graphic display.
5. Automatic code generation handles continuous time, discrete time, and hybrid systems.
6. Optimized code guarantees fast execution.
7. Control framework Application Program Interface (API) uses customizable “makefiles” to build and download object files to target hardware automatically.
8. Portable code facilitates usage in a wide variety of environments.
9. Concise, readable, and well-commented code provides ease of maintenance.
10. Interactive parameter downloading from SIMULINK to external hardware allows system tuning on the fly.
11. A menu-driven, graphical user interface makes the software easy to use.

The Real Time Workshop supports the following target environments:

1. dSPACE DS1102, DS1002, DS1003 using Texas Instruments (TI) C30/C31/C40 Digital Signal Procesors (DSPs)
2. VxWorks, VME/68040 Processor Board
3. 486 PC-based systems with Xycom, Matrix, Data Translation, or Computer Boards I/O devices and Quanser MultiQ board

6.3 Simulation Results

The IDMA model has been successfully compiled in SIMULINK’s Real Time Workshop (RTW) and is ready to be transferred to a compatible hardware device. In addition the simulation processing time has been successfully reduced to 8.6 minutes on a stand alone personal computer (PC).

Figure 6.1 illustrates the results of the first ten iterations of IDMA’s iterative detection process for 64 bits of one user of a 64-user uncoded IDMA system designed in SIMULINK (with randomly generated interleavers, information block length of N=64 bits per user and a common length-16 spreading sequence for all users) for AWGN channels.

Figure 6.2 demonstrates the successive decrease in BER within the first ten iterations of IDMA detection process. The results achieved by this design achieve convergence in fewer iterations as compared to the previous simulations. Tables 6.1 to 6.6 demonstrate the iteratively calculated values for eight bits of user data of six users. They exhibit the initial change of values and their subsequent approach towards convergence before the calculation of hard decision at the end of tenth iteration.

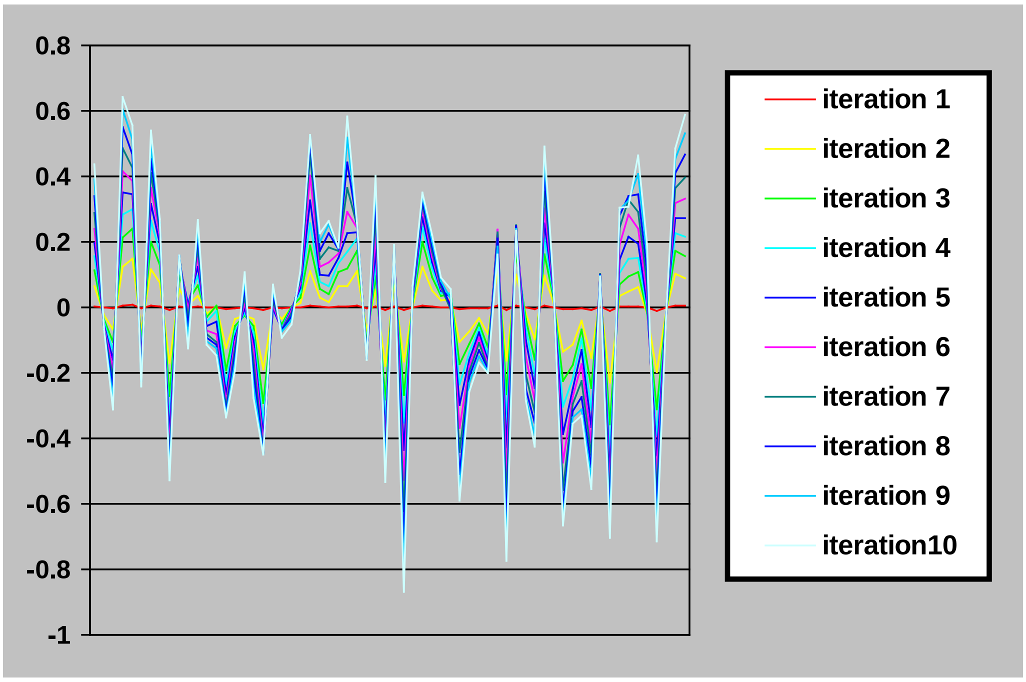

Figure 6.1: Detection performance of uncoded IDMA system of 64 users

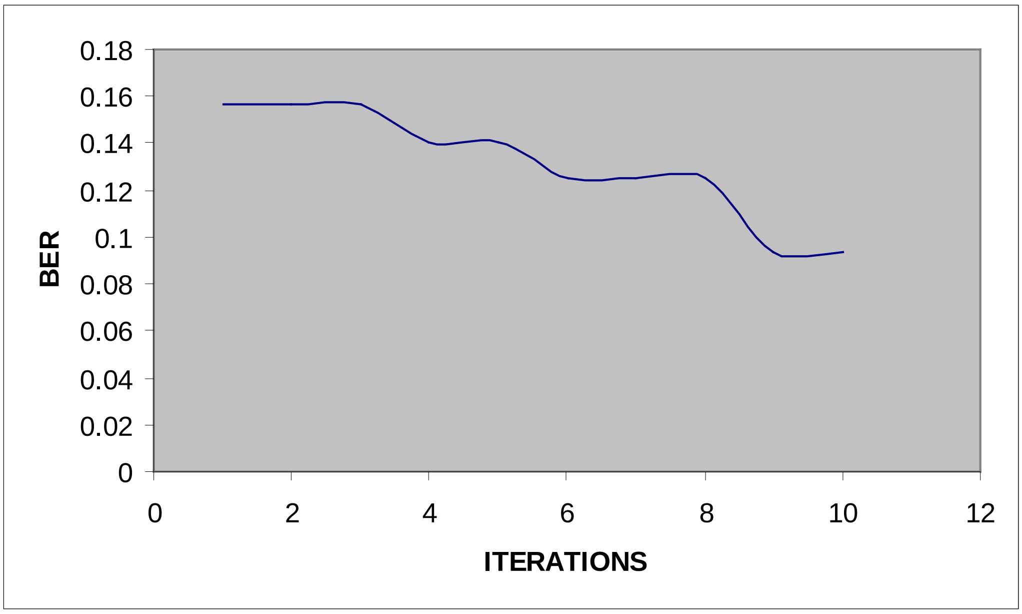

Figure 6.2: BER performance of uncoded IDMA system of 64 users

Table 6.1: Iterative detection of 8-bits of user 1 (10 Iterations)

Iteration 1	0.014224	-0.00368	0.008733	0.003096	-0.00135	0.010159	0.00742	0.005129
Iteration 2	0.29604	-0.07812	0.18123	0.063618	-0.02976	0.2112	0.15391	0.10623
Iteration 3	0.44969	-0.147	0.26392	0.078721	-0.07908	0.31599	0.22458	0.15003
Iteration 4	0.55698	-0.18553	0.32064	0.08953	-0.1164	0.39111	0.27883	0.1828
Iteration 5	0.64022	-0.20545	0.364	0.096797	-0.14703	0.45106	0.32733	0.20727
Iteration 6	0.71056	-0.21283	0.40052	0.10139	-0.17358	0.50356	0.37633	0.22455
Iteration 7	0.7743	-0.21093	0.43399	0.10402	-0.19769	0.55317	0.42882	0.23593
Iteration 8	0.83501	-0.20175	0.46664	0.1054	-0.22051	0.60204	0.48263	0.24513
Iteration 9	0.89383	-0.1873	0.49937	0.10607	-0.24287	0.64931	0.5298	0.25918
Iteration 10	0.94936	-0.17052	0.5317	0.10634	-0.2653	0.69113	0.56331	0.28399
DEC o/p	1	-1	1	1	-1	1	1	1
original data	1	-1	1	1	-1	1	1	1

Table 6.2: Iterative detection of 8-bits of user 2 (10 Iterations)

Iteration 1	-0.00102	-0.00164	-0.00069	0.00808	0.008859	-0.00545	0.007528	0.001445
Iteration 2	-0.02273	-0.03565	-0.01587	0.16759	0.18373	-0.11534	0.15654	0.029287
Iteration 3	-0.06654	-0.08691	-0.05499	0.24351	0.26518	-0.21174	0.23482	0.028959
Iteration 4	-0.1023	-0.1244	-0.08184	0.29698	0.32	-0.2756	0.29563	0.034549
Iteration 5	-0.13661	-0.15438	-0.10114	0.3379	0.36228	-0.32161	0.34663	0.041908
Iteration 6	-0.17295	-0.17973	-0.11554	0.37093	0.39923	-0.35734	0.39203	0.04923
Iteration 7	-0.21254	-0.20194	-0.12669	0.39845	0.43512	-0.38687	0.43444	0.055828
Iteration 8	-0.253	-0.22154	-0.13562	0.42187	0.47292	-0.41218	0.47541	0.06168
Iteration 9	-0.28817	-0.23851	-0.14322	0.44223	0.5145	-0.43416	0.51561	0.066965
Iteration 10	-0.312	-0.25285	-0.15025	0.46068	0.55998	-0.45356	0.55511	0.071776
DEC o/p	-1	-1	-1	1	1	-1	1	1
original data	-1	-1	-1	1	-1	-1	1	1

Table 6.3: Iterative detection of 8-bits of user 3 (10 Iterations)

Iteration 1	0.001319	0.007487	0.005981	0.013269	-0.00273	-0.00113	-0.01088	-0.00584
Iteration 2	0.026058	0.15479	0.12409	0.27619	-0.05857	-0.02484	-0.22848	-0.12359
Iteration 3	0.0103	0.21055	0.17892	0.42474	-0.12995	-0.06324	-0.39037	-0.22637
Iteration 4	-0.00454	0.23885	0.21894	0.54136	-0.19069	-0.08581	-0.50193	-0.29621
Iteration 5	-0.01898	0.25224	0.25007	0.65005	-0.25057	-0.09954	-0.58981	-0.34838
Iteration 6	-0.03329	0.25683	0.27632	0.75716	-0.31398	-0.10786	-0.66759	-0.39121
Iteration 7	-0.04767	0.25584	0.30044	0.8477	-0.37713	-0.11259	-0.74292	-0.42981
Iteration 8	-0.06213	0.25128	0.32412	0.90581	-0.4279	-0.11461	-0.81939	-0.46707
Iteration 9	-0.07666	0.24472	0.3477	0.93717	-0.45838	-0.11437	-0.89649	-0.50346
Iteration 10	-0.09133	0.23746	0.37013	0.95491	-0.47239	-0.11219	-0.96966	-0.53643
DEC o/p	-1	1	1	1	-1	-1	-1	-1
original data	-1	-1	1	1	-1	-1	-1	-1

Table 6.4: Iterative detection of 8-bits of user 4 (10 Iterations)

Iteration 1	-0.00601	0.001408	-0.00234	-0.00273	0.006632	0.011311	0.003812	0.006693
Iteration 2	-0.12676	0.028402	-0.05032	-0.05841	0.13715	0.23495	0.078257	0.1382
Iteration 3	-0.22643	0.023652	-0.10959	-0.12591	0.19905	0.34437	0.096018	0.18757
Iteration 4	-0.29199	0.02207	-0.15534	-0.17978	0.2581	0.41299	0.10497	0.21785
Iteration 5	-0.34081	0.020966	-0.19843	-0.22816	0.32583	0.45901	0.10797	0.23934
Iteration 6	-0.38197	0.019638	-0.24325	-0.27455	0.40673	0.49147	0.10629	0.25643
Iteration 7	-0.42043	0.01806	-0.28458	-0.32084	0.49366	0.51526	0.10064	0.27115
Iteration 8	-0.45813	0.016484	-0.30846	-0.36817	0.56865	0.53335	0.091818	0.28459
Iteration 9	-0.49401	0.015114	-0.3073	-0.41733	0.62237	0.54789	0.080901	0.29732
Iteration 10	-0.52458	0.014034	-0.28785	-0.46828	0.65928	0.56061	0.06881	0.30967
DEC o/p	-1	1	-1	-1	1	1	1	1
original data	-1	1	-1	-1	1	1	1	-1

Table 6.5: Iterative detection of 8-bits of user 5 (10 Iterations)

Iteration 1	0.005014	0.004243	0.006626	0.008994	0.000413	-0.00634	0.000437	-0.00252
Iteration 2	0.10356	0.087185	0.13718	0.18654	0.006969	-0.13368	0.007993	-0.05384
Iteration 3	0.14285	0.10952	0.19499	0.26597	-0.02085	-0.24816	-0.01086	-0.10716
Iteration 4	0.17435	0.12267	0.23837	0.31234	-0.04126	-0.34293	-0.0236	-0.13722
Iteration 5	0.20243	0.13116	0.27634	0.34012	-0.05667	-0.43692	-0.03579	-0.15366
Iteration 6	0.22909	0.13689	0.31391	0.3568	-0.06902	-0.53915	-0.05052	-0.16088
Iteration 7	0.25558	0.14068	0.35441	0.36652	-0.07968	-0.64806	-0.06952	-0.16087
Iteration 8	0.28296	0.14287	0.39987	0.37195	-0.08939	-0.75081	-0.09272	-0.15444
Iteration 9	0.31191	0.14365	0.45039	0.37486	-0.09833	-0.83407	-0.1175	-0.14232
Iteration 10	0.34252	0.14345	0.5029	0.37628	-0.1064	-0.89222	-0.13887	-0.12598
DEC o/p	1	1	1	1	-1	-1	-1	-1
original data	1	-1	1	1	-1	-1	1	1

Table 6.6: Iterative detection of 8-bits of user 6 (10 Iterations)

Iteration 1	0.006618	0.006865	0.003472	0.000914	-0.00519	0.012006	0.008399	-0.00244
Iteration 2	0.13741	0.14235	0.071012	0.017891	-0.1101	0.24967	0.17425	-0.05212
Iteration 3	0.20003	0.20635	0.082851	0.006064	-0.20559	0.37193	0.26075	-0.10316
Iteration 4	0.24423	0.25589	0.088763	0.002571	-0.26989	0.45184	0.33547	-0.13107
Iteration 5	0.2764	0.30092	0.091882	0.003479	-0.31637	0.508	0.41061	-0.14651
Iteration 6	0.30037	0.34769	0.093291	0.006589	-0.35223	0.54991	0.49207	-0.15485
Iteration 7	0.31851	0.39936	0.093313	0.010674	-0.38155	0.58289	0.57978	-0.15901
Iteration 8	0.3324	0.45399	0.092147	0.014954	-0.40664	0.61033	0.66512	-0.16053
Iteration 9	0.343	0.5038	0.090076	0.018679	-0.42893	0.63446	0.73672	-0.16035
Iteration 10	0.35096	0.54184	0.087487	0.021252	-0.44923	0.65681	0.7922	-0.15903
DEC o/p	1	1	1	1	-1	1	1	-1
Original data	1	1	-1	1	-1	1	1	-1

6.4 Conclusion

The implementation method has successfully reduced the processing delays to 8.6 minutes on a stand alone PC. Moreover, the model has been successfully compiled in SIMULINK’s Real Time Workshop (RTW) thus facilitating the transfer of the system code to a compatible hardware device.

Chapter 7

CONCLUSION

7.1 Overview

The aim of this research work is to optimize IDMA system for successful implementation in real time environment by the significant reduction of system processing delays. Successful simulations of the IDMA system have already been conducted but the process is time consuming.

7.2 Objectives Achieved

The complete multiple access system has been successfully implemented and tested in SIMULINK for 3, 4, 16, 32, 64 users. The SIMULINK model has also been compiled in SIMULINK's Real Time Workshop (RTW) which means that the system is configured to be transferred to a variety of hardware compatible with RTW. Processing delays on a plain PC have been reduced to approximately 8.6 minutes. The SIMULINK model can also act as a simulation test bed to test IDMA's behavior under a variety of different conditions and channels.

7.3 Future Work

Suggestions for extension of this work might include:

1. The IDMA system implemented in SIMULINK does not have any error correction block included in it. An optimal error correction coding technique can be incorporated in this model.
2. The model can be implemented using low rate as well as high rate turbo codes.

3. The model although ready for hardware deployment has not been entirely tested on a RTW compatible hardware yet. Implementation on FPGAs could pose interesting issues.

7.4 Conclusion

The entire IDMA system has been implemented in SIMULINK. The design has been successful in reducing processing delays considerably. The developed model can also serve as a software test bed for analyzing different properties and testing out the system under various conditions. Moreover, the model has been successfully tested in SIMULINK's Real Time Workshop (RTW). The compatibility of RTW with a variety of hardware renders the IDMA system model ready to be deployed in real time environment.

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ACHIEVEMENTS

International Publications:

Sana Javed, Imtiaz Ahmad Khokhar, Atiya Obaid, **“ A Novel Proposal for chip by chip iterative detection in Interleave Division Multiple Access (IDMA)”**, 4th International Symposium on High Capacity Optical Networks and Enabling Technologies (HONET 2007) at Dubai, UAE, 18-20 November 2007.

Sana Javed, Imtiaz Ahmad Khokhar **“Implementation of Interleave Division Multiple Access (IDMA)”**, IEEE Sarnoff Symposium 2008 at Princeton, New Jersey, US, 28-30 April 2008.