Integrated Control of Parallel Connected Multiple SEPIC Converters For DC Microgrid Operation

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DEDICATION

To my parents, whose unwavering love and support have been my constant source of strength. To my mother, for her endless sacrifices, encouragement, and belief in me when I needed it most—this work is a reflection of your boundless love.

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ABSTRACT

DC microgrids are gaining popularity now a days due to their advantages such as improved efficiency, reliability, and renewable energy integration and also due the environmental challenges like carbon and other greenhouse gases emission from fossil fuel consumption for energy purposes. One of the core challenges in DC microgrids is stabilization and regulation of DC bus voltage, which is crucial for the proper operation of the loads connected to DC bus. Parallel connection of DC DC converters is a commonly used approach for combining and distributing multiple sources of DC power in a microgrid. In this thesis, a fourth order DC DC Single Ended Primary Inductor Converter (SEPIC) converter is selected and it's mathematical model is built including it's peracetic resistances/ESRs in order to realize the real case scenarios, based on this mathematical model a Linear Quadratic Controller (LQR) is designed for an optimal control strategy of the parallel connected SEPIC converters in a DC microgrid. The proposed optimal control strategy uses a decentralized distributed control approach, where each converter self regulates its voltage output based on estimated values of all states through a state observer. In this work a decentralized and distributed an optimal control scheme is selected, analyzed and modelled for power balance operations in an islanded 80-100V-LVDC microgrid, consisting of a renewable energy source, an electronic load and storage capability. Control is realized through DC bus voltage monitoring and control operations on the interfacing converters, based on predefined voltage set points. To cope with the converter uncertainties, external disturbance, to annihilate the need for sensors and most importantly to annihilate the bandwidth communication lines a robust optimal controller based on extended state observer (ESO) is proposed and applied to SEPIC converters in parallel mode of operation. The comparison with PI control shows that the proposed method can achieve better disturbance rejection ability without overshoot in step response.

The control strategy is designed to provide rapid response to different loading conditions, improve regulation of voltage, and reduce voltage ripples. Through MATLAB/Simulink simulations and hardware module results shows that the proposed control strategy effectively regulates and tracks the DC bus voltage reference and hence ensures the stability of overall DC microgrid under different loading conditions and as well as different reference voltage levels. The proposed control strategy can be a useful approach for DC microgrid designers and operators to ensure the proper functioning of the microgrid and improve its overall performance.

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LIST OF ABBREVIATIONS

DCMG: Direct Current Micro Grid.

DRE: Distributed Renewable Energy.

RES: Renewable Energy.

ACS: Active Current Sharing.

OL: Outer Loop.

EL: External Loop.

DL: Dual Loop.

LQR: Linear Quadratic Regulator.

LQI: Linear Quadratic Integrator.

LQE: Linear Quadratic Estimator.

ESO: Extended State Observer.

CS_bus: Current Sharing Bus.

CCM: Continuous Conduction Mode.

DCM: Discontinuous Conduction Mode.

ARE: Algebraic Reccartii Equation.

Ess: Steady State Error.

PID: Proportional Integrator Derivative.

Chapter 1

Introduction

1.1 Background

The energy hungry cities, modern residential, offices and Industries rely on and prefer Direct Current DC over AC loads due the advantages of DC over AC equipment/load. For an example, steel industries in earlier times uses AC arc furnaces but now this sector's trend has shifted and almost all steel industries have deployed DC arc furnaces due to their less consumption of electric energy than AC arc furnaces. This phenomenon has prevailed through all over socioeconomic arena hence the concept of DC microgrids DCMGs are increasingly gaining attention among both scientific and industrial community due to the increasing ratio of DC energy end user demands than AC microgrids [1,2]. The growth of the share of distributed renewable energy (DRE) in total electricity production in addition to the tremendous advancement of technology in power electronics and the increase in DC loads, lead to the DC microgrid (DCMG) concept as a valid model for future energy, specifically for the areas where the current network of electrical energy generation, transmission and distribution is not satisfied and sufficient.

Moreover, one of the main sources of DC energy and only one being in the abundance is renewable energy sources (RES). The RES are now a trend worldwide because of the fact that RES are environmental friendly energy sources like photovoltaic PV which converters solar energy into electrical energy/DC energy. Offshore wind turbines, which produces DC energy from wind/air flow. One of the the utility of this energy generated from RES it that, this DC energy is fed to an AC grid through a DC bus to be converted again into AC energy to provide it to the end users having AC loads [3,4]. The conversion stage can be annihilated which also improves the overall efficiency of the system, by designing and shifting the distribution system on a DC network [5-7]. A DC microgrid consists of distributed sources, load and storage connected to the DC bus via converters. There are mainly two problems in DCMG operation which is the power balance between the supply and demand and its implementation through interface converters, which in turn must be able to facilitate these operations. Many grid control strategies can be used but whatever a strategy, control is realized through regulation of the DC bus voltage.

Additionally, the advantages which comes along with a DC microgrids is their capabilities of employing the static storage. Most of this static storage also known as storage systems, which includes ultra-capacitors and batteries are purely DC. Apart from static storage utilizing capabilities of a DCMG, the concatenation of mechanical storage systems such as flywheels which uses a permeant magnetic synchronous machine, can be done, generally through a DC bus [8,9].

In the past few years, the idea and a will for more efficient nexus of distributed renewable energy and storage systems in energy infrastructure, the idea of DCMGs has gained more attention due to its being economical and efficient, for an instance in DCMG process of the rectification and conversion stages are not required hence annihilated [10]. For interlinking the distributed energy resources (DER) with a DCMG, DC DC converter are required, which can be connected in serval fashion among which is parallel connection of DC DC converters can be employed, parallel connected converters offers serval advantages compared to a single unit structure. as shown in Fig. 1.

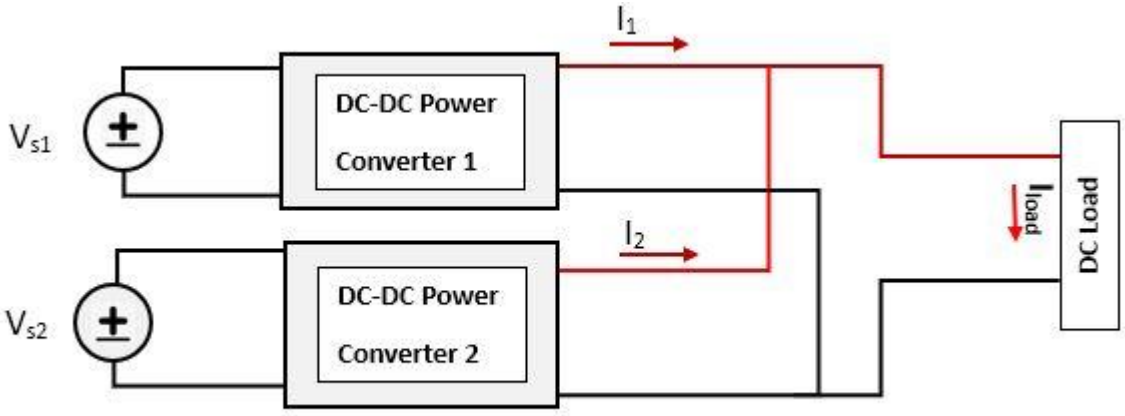


Figure 1: Parallel-connected converters.

Generally, the main goal of utilizing this scheme of parallelly connected converters in a DC microgrid is to ensure and achieve the following:

- Less Thermic Stress: The parallel connected converters are able to share the burden of the total load power demand to every module, resulting in small power dissipation in each

converters/module. Thus, the protection and design of components is simplified for parallel configuration.

- Reliability: Since there is less thermal stress on each module in parallel configuration, which ensures better power management and no overloading of converters, results in enhanced system reliability.
- Scalability: Parallel scheme provides the pliancy to add or remove converters as per the system requirements. This makes the system feasible to boost up or down the power capacity of the overall system without redesigning the system.
- Redundancy: Since multiple converters operate in parallel mode, there is incorporated redundancy. In case of failure or shutting down one of the modules for maintenance, the other modules are able to operate and provide uninterrupted power supply, minimizing downtime and improving system availability.

Although DC DC converters in parallel operation is faces major challenges such as circulating currents among converters, unbalanced sharing of load current and degradation of DC bus regulation of voltage [11]. In parallel scheme of connection of the converters, any unbalanced and unequal voltage outputs, causes to start the circulating currents, which steer the higher current flow through the switch of power electronics converters and it results in mismatched sharing of load current among DC converters.

The current disproportion yields in increased switch stress/thermal stress on particular units and lower the reliability of the overall system. Consequently, expanding the size for increased power rating of the switches and other power electronic components is required at the expense of higher cost.

Substantial efforts/attempts have been made to alleviate and subdue the challenges encountered in an operation of DC parallelly connected converters forming a DCMGs. Thus, many schemes of control action for the DC converters in parallel connection are presented and analyzed in past [12-16]. For DC DC converters connected parallelly the control action is categorized in two main schemes that is, ACS and Droop methods. The Figure 1.2 represents the general classes of control action for parallelly connected DC DC converters.

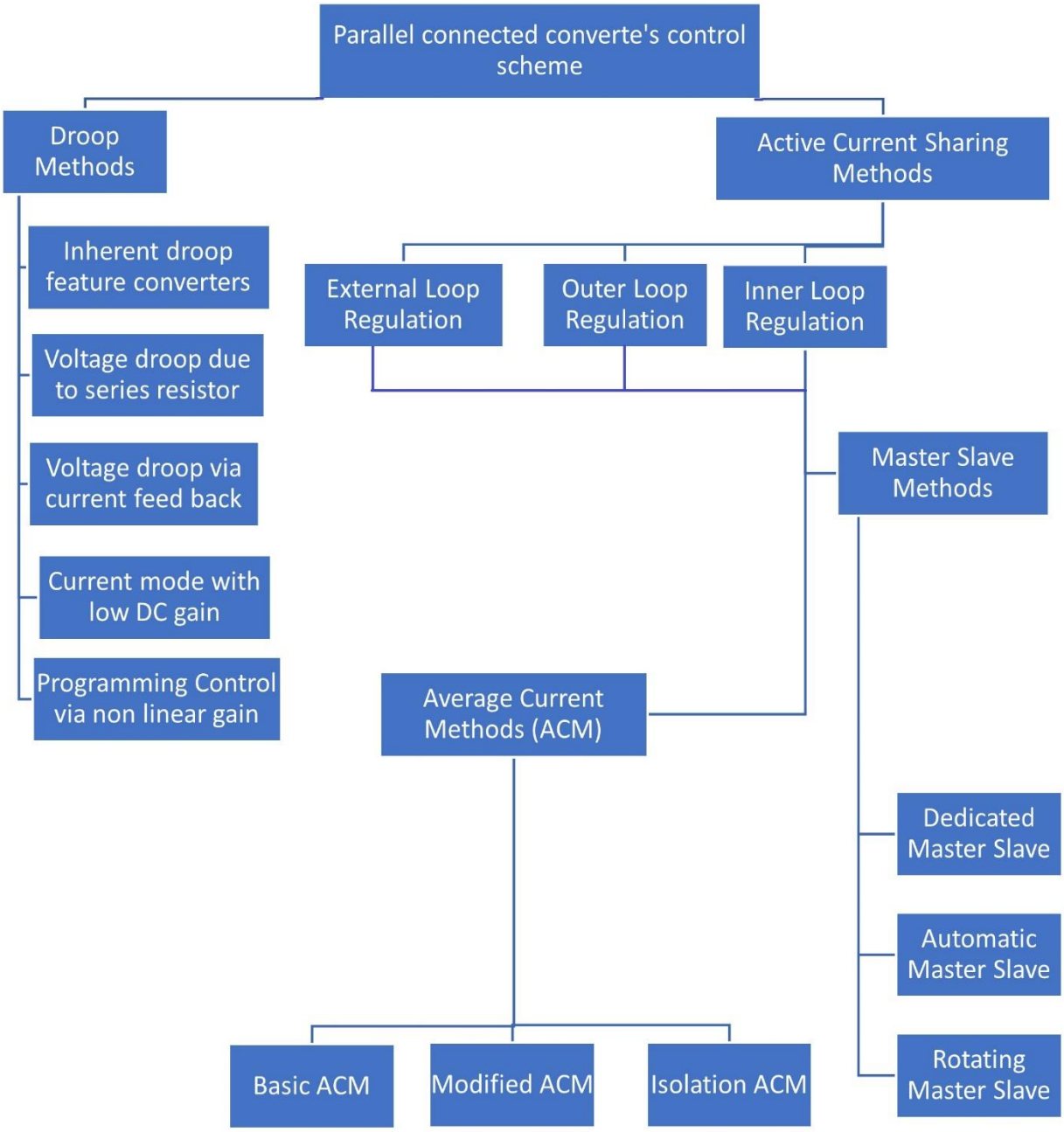


Figure 2: Control Schemes for DC DC converters connected Parallelly.

From Figure 1.2 the Active Sharing of current (ACS) control scheme are further categorized into two classes of control schemes, namely Average Current Methods (ACM) and master-slave methods. The ACS methods bring forth good precision in regards to sharing of current and regulation of voltage, but it needs processing error signal of the sharing of current between the modules. The ACS methods predominantly based on particular control scheme of operation, which are inner loop (IL), outer loop (OL), or external loop(EL) scheme of control action. The three said control schemes differ from each other on the basis of sharing of current error signal. Iner Loop (IL) regulation is correlated with the use of a single error signal as a feedback from point of common coupling/DC bus. Outer loop (OL) regulation in ACS involves adjusting the control variables or parameters of the individual devices to ensure equal sharing of current. This is typically done by measuring the current flowing through each device and using a control algorithm to adjust their respective duty cycles or operating points. The External loop (EL) regulation mode collates all signals of sharing of load current from each DC DC parallelly connected converters and calibrates the respective control input to adjust the sharing of current equally. In the main, signal of error/difference in sharing of current are crucial to get better and accurate current as well as load sharing between parallel connected DC DC converters. Hence, many of the ACS mode of control schemes require a communication network with high-bandwidth, which is uneconomical and undesirable choice for a DC microgrids [13]. While other methods like offer more reliability as they do not incorporates the communication schemes but they suffer from less sharing of current precision and regulation of voltage. As depicted in Fig. 1.2, the droop scheme can be divided in five control schemes, which are based on different methods to get the benefits offered by droop method/scheme for DC DC parallelly connected converters. Despite the fact that the communication signal between parallel connected converters is not needed, the regulation of voltage and sharing of current precision is the core drawback of the mentioned droop methods. Therefore, to mitigate these issues low bandwidth communication is deployed to improve the balanced load sharing and regulation of voltage [14]. Balanced sharing of load current and proper regulation of voltage are constrained by the deployment of communication network among DC DC parallelly connected converters, which leads to the higher cost and less reliability of DCMG. Each of these strategies of the proposed methods for controlling converters parallelly connected has their tradeoffs in terms of their implementation, operation

and application. However, the considerate utility of these methods is to obtain an accurate and balanced sharing of load current and proper regulation of voltage. A suitable selection of the control scheme for converters connected parallelly depends on the pros and cons of different schemes. Although the advantage of parallelly connected converters are well established and acknowledged, selecting one of these control schemes for parallel connected converters must consider factors including, reliability, modularity, cost and complexity for a definite application. The research/thesis focuses on the ACS methods.

1.2 Motivation

Numerous methods on control architecture for DC DC converters in parallel connection mode of operation in a DC microgrid is presented in literature [17-37]. The performance evaluation on the bases of reliability, cost, complexity and precision are the crucial factors of these techniques of control action. Substantial research has been done in order to ameliorate one or multiple factors to improve the functionality of ACS methods. In spite of the fact that the precision of ACS methods is ensured, the precision enhancement of ACS method highly depends on the communication network to route the voltage and current signal among the parallelly connected converters.

The aim of this work is to establish an alternate and improved ACS method that fulfills the criteria of DC DC converters in parallel connection mode of operation, which is to annihilate the circulation current, equal sharing of load current, accurate and proper regulation of voltage of DC bus under various loading conditions and wide range of input voltages. The desired operational performance of the converters in parallel mode of is realized by eliminating the high bandwidth communication network between modules connected in parallel, which in return leads to a lesser complexity and reduction in the total cost and increases the system reliability, fault tolerance and scalability along with enabling Plug and Play (PnP) feature without jeopardizing the whole microgrid's stability meanwhile making the control architecture more intelligible. The aims will be ensured and realized through the following objectives mentioned on next page.

1.3 Objectives

1. Mathematical Model of a SEPIC converter including the ESRs of the components without order reduction.

2. State Space analysis to design a Linear Quadratic Controller LQR for SEPIC converter.

3. State feedback to annihilate steady error, track and regulate the voltage reference at DC bus by deploying integral action.

4. Designing an Extended State Observer (ESO) to estimate/observe the states and reject any system or external disturbances, which annihilates the need for sensors and hence the need for communication network.

5. Ensure synchronous switching and finding of an optimal operating point (duty cycle) for different sizes of parallelly linked SEPIC converters under different loading and input voltage conditions, to annihilate the actuation of circulating current.

1.4 Outline of the Thesis

The theme of this work is discussed in this section respective of each six chapters and organized in a way to make sense of the steps involved in executing/developing the proposed method.

Chapter 1

In this chapter a brief introduction and background of this study/thesis is presented. It discusses several classifications of control schemes for DC DC parallelly connected converters forming a DC microgrid. It describes the advantages of using DC DC converters in parallel connection over a single mode of operation of a converter. The motivation behind the proposed method in this thesis is presented to emphasize the value of this research and at the end of this chapter, the research goals, outline and flow of this dissertation is described.

Chapter 2

A review of the existing literature on different control schemes designed for operation of DC DC converters operation in parallel link is done in this chapter. Control schemes are categorized in two classes, droop scheme and ACS methods. In this section the argument of using modified ACS method is justified and the tradeoffs and limitation of the droop scheme and conventional ACS methods is described on the basis of already existing literature on it.

Chapter 3

The development of mathematical model of DC DC converters, which is SEPIC converter in this work, is presented in detail in this chapter. The working of the DC DC converter in different modes of operation is discussed along with converter's components selection and designing process is also discussed in detail in this chapter.

Chapter 4

In Chapter 4, a brief introduction of Linear Quadratic Controller (LQR) is presented and the designing of this optimal controller according to the proposed methodology is described in detail. Also, an Extended State Observer (ESO) is designed to estimate and observe all the states and to mitigate the effects of system disturbances as well as external disturbances on DC DC converter in a DC microgrid operation is given. The proposed optimal controller developed is then deployed to a single stage converter to perform a stability analysis through state space analysis.

Chapter 5

The extension of the developed controller to the operation of SEPIC converter in parallel connection in a DC microgrid is investigated. Also, four cases: two for different loading and two for different voltage input conditions are implemented and verified through MATLAB/Simulink simulation in this chapter. In this chapter the proposed method of modified ACS scheme of control for parallel connected DC DC converters is defended and justified, by eliminating the need for high bandwidth communication and measurements of currents and voltages among the parallelly connected converters to regulate the DC bus voltage as well as proper sharing of load current, through the MATLAB/Simulink simulation results. In the proposed method, the locally estimated current and voltage values through a state observer/estimator are utilized to predict and estimate the set point voltage for each parallelly linked converter. To satisfy that the load current is shared based on the load regulation characteristics for each converter the voltage reference is fed locally to the outer voltage loop of each output parallelly linked converter. Also, comparison of the proposed scheme with conventional control scheme is also presented at the end of this chapter.

Chapter 6

In Chapter 6, the major outcomes and primary contributions and application of this thesis are summarized. Conclusion and suggestions for further extension of this work in future is presented in the end of this last chapter.

Chapter 2

Literature Review

2.1 General Overview.

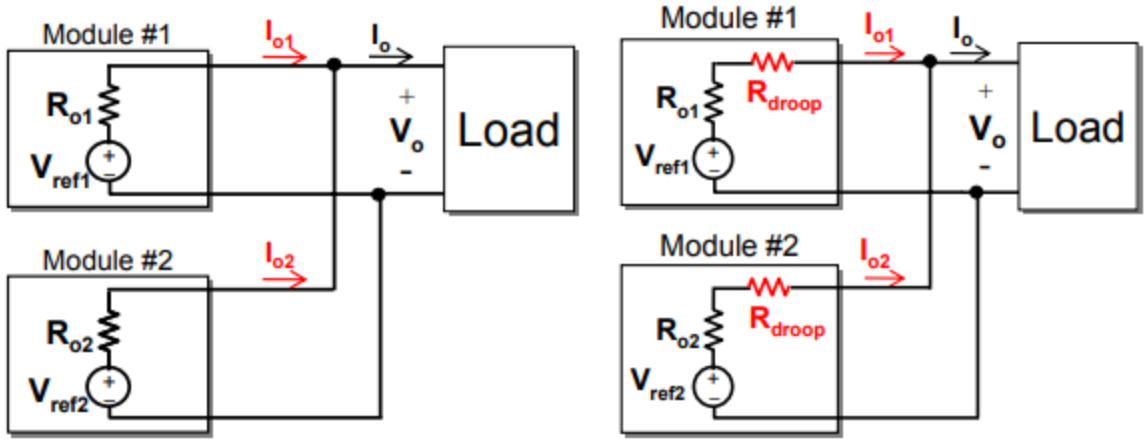
As mentioned before several advantages can be obtained by deploying DC DC converters in parallel connection mode of operation in a DC microgrid. Nonetheless, the main issues and challenges in parallel mode of operation of converters are proper sharing of load current, circulating currents and proper regulation of voltage of a DC bus. To cope with these challenges, a number of methods and techniques have been reported and presented in literature. These methods attenuate and curb the problems that arise in the operation of parallel connected DC DC converters. Such methods have been presented and deployed for better sharing of load current and regulation of voltage at DC bus while eliminating the current circulation among the converters operating in parallel connection mode. The factors like reliability, applicability, cost and complexity are deciding factors pf these methods to deploy them in DC microgrid operation.

The core goal of this section is to explore these methods in detail and discuss the corresponding research contributions done in the area of control methods for parallelly connected DC DC converters forming a DC microgrid. This chapter spotlights on the pros and cons of each method in order to signify and establish the core context of the suggested research work.

2.2 Method of Passive Droop Sharing of current:

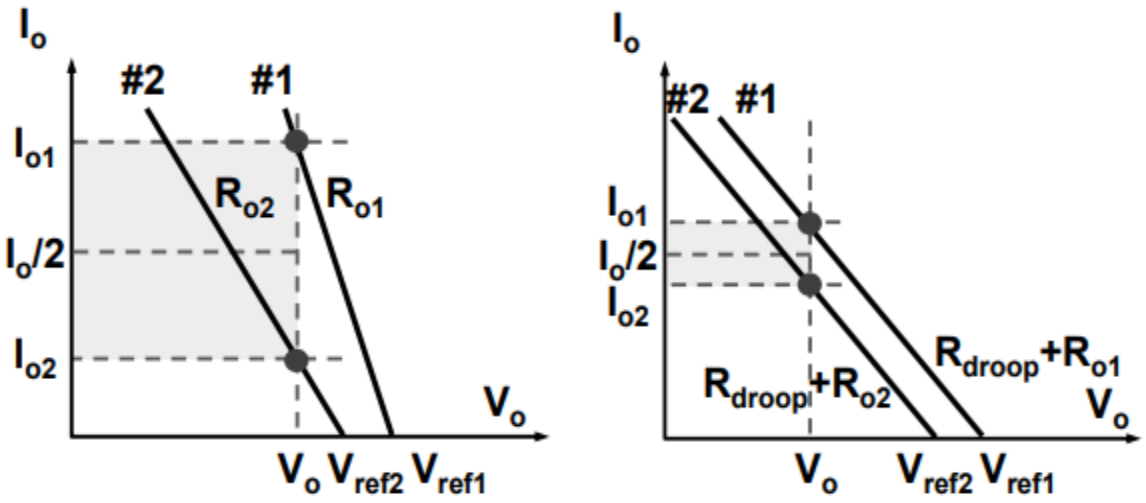
Several sharing of current methods have been investigated, suggested and implemented by researchers in related area/industry, and a corelative classification of the methods for sharing of current among DC DC converters reported [38]. Just as the word "droop" infer, this scheme of parallel linkage is realized by designing/altering each power modules with a specific and definite resistance, R_{droop}, in order to allow voltage output fall a bit as the load current is increases.

$$I_{o1} - I_{o2} = \frac{2.(V_{ref1} - V_{ref2})}{R_{o1} + R_{o2}} + \frac{I_o.(R_{01} - R_{o2})}{R_{o1} + R_{o2}} \qquad \textbf{2.1}$$



(a) without droop **(b) with droop**

Figure 2.1 A Parallel connected DC converters: **(a)** without droop sharing of current. **(b)** with droop sharing of current.



(a) without R_{droop} **(b) with R_{droop}**

Figure 2.2 V-I Output characteristics: **(a)** without $R_{droop.}$ **(b)** with $R_{droop.}$

Regulation of voltage is determined by:

$$V_o = \frac{(V_{ref1}R_{O2}+V_{ref2}R_{o1})}{R_{o1}+R_{o2}} + \frac{I_o.R_{01}R_{o2}}{R_{o1}+R_{o2}} \qquad \textbf{2.2}$$

Addition of the droop resistance, R_{droop}, the output impedances becomes $R_{o1}+R_{droop}$ similarly $R_{o2}+R_{droop}$. Equation (2.1) clearly indicates that with the increased resistance output values, the error in sharing of current is reduced. Obtaining this advantage without using of either high bandwidth or low bandwidth communication network between the DC DC parallelly connected converters is the main perk of droop sharing of current control methods.

But from equation (2.2) the drawback of droop sharing of current control methods are also obvious, there is a clear tradeoff indicated between reduced sharing of current error and degraded regulation of voltage with the addition of R_{droops} The disadvantages are evident: based on (2.2), the degraded regulation of voltage is inevitable to ensure an accurate sharing of current, and it's hard and tedious to attain balance sharing of current between modules with different power ratings of components of each DC DC converter connected in parallel [39]. The details about implementation and constraint of droop sharing of current schemes are discussed in detail in remaining of this section.

2.2.1 Droop Sharing of current Method Configuration.

The implementation of droop resistance R_{droop}, can be done in several ways according to works reported in literature [40][41][42][43]. In the following section, different implementation schemes of droop method of sharing of current illustrated in Fig 1.2, and their characteristics is briefly introduced.

(a) Inherent droop feature converters:

One of the simpler and straightforward schemes to enable proper operation of DC DC converters in parallel connection forming a DCMG is to choose DC DC converters with built in droop properties. Some DC DC converters operate in the discontinuous current mode (DCM), such as boost and buck converters, have built in capability of proper load sharing and ability to be deployed in parallel connection with the requirements and necessities of proper regulation [40].

Figure 2.3 illustrates the V-I characteristics of parallelly connected two buck converters. Converters mode of operation working in DCM. Since in DCM it has an inherent droop property, load current balance to some extent is realized without an extra efforts and arrangements.

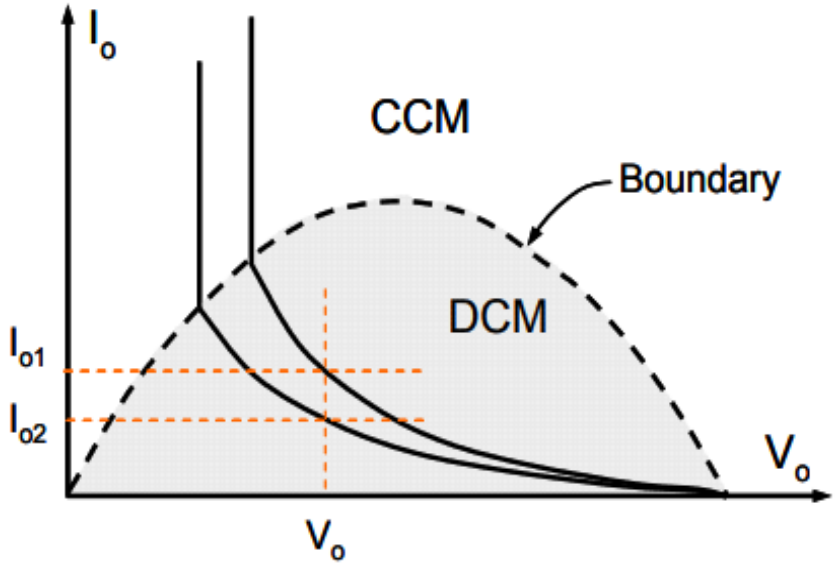


Figure 2.3: V-I output characteristics of buck converters in parallel under DCM operation.

Some other variants of DC DC converters have inherent droop features such as the resonant converters. In such converters the relationship between load resistance and voltage output is nonlinear for specific range of control switching frequencies, the output I-V characteristics as illustrated in below Figure 2.4 exhibits inherent droop feature properties. Hence, there is possibility for such converters to use this property to perform droop action to perform proper sharing of load current between the resonant converters connected parallelly forming a DC microgrid.

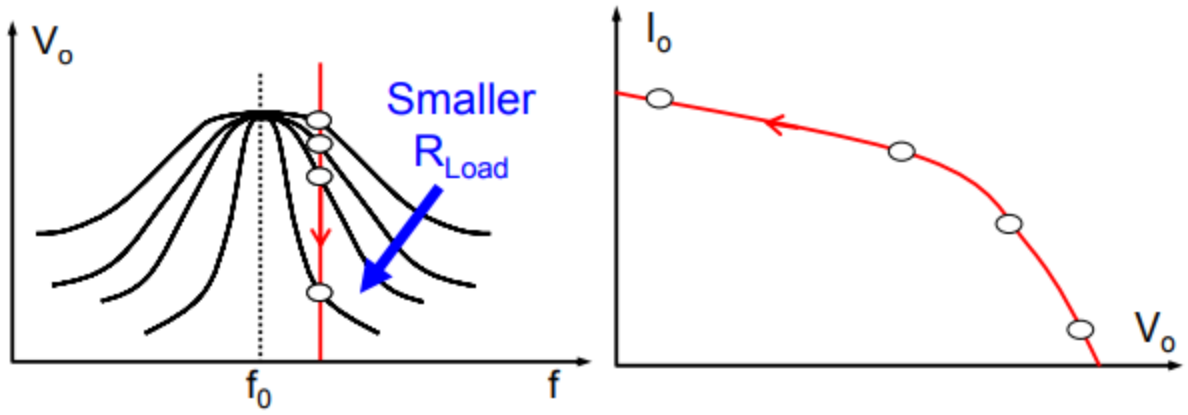


Figure 2.4 I-V output characteristics of series resonant converters.

(b) Voltage Droop via External Resistances:

The droop sharing of current is realized with the addition of external resistor to each module connected in parallel mode of operation. The DC DC converter modules connected in parallel have an initial setup, which is arranged through a potentiometer, are made near identical to each other. A resistor in series is added to each converter's output terminal such that, a voltage drop I*R is ensured at the output terminals of each module [41]. Clearly the core disadvantage of this method is the power dissipation due to added resistor in series, this power dissipation is directly proportional to the droop action that is the higher value of resistance added.

Suppose a system where two modules are connected in a parallel mode and due to the fault in one module, another module is responsible to supply the load.

For a 20V, 15A rated system, with a 0.07-Ω series resistor, a 1.05 voltage droop appears

Hence, this method is feasible only for system which are needed for low power supplies.

(c) Voltage droop through current feedback:

In this scheme to achieve the droop action, current of each module is sensed at out terminals. As illustrated in Fig 2.5 along with feedback voltage information, a current feedback information is also added, droop action realized is proportional to the current output of the module [41]. In a voltage feedback loop compensator, with having an infinite DC gain K_v, the output droop characteristic equation is given as follow:

$$V_O = \frac{V_{ref} - K_i I_{o1}}{K_v} \qquad \textbf{2.3}$$

Hence, the resultant droop resistance can be expressed as follow:

$$R_{droop} = \frac{K_i}{K_v} \qquad \textbf{2.4}$$

Obviously, this scheme depicts the almost identical performance to the method of droop action ensured through an addition of resistor in series with each module's output as described in above section **(b)**. Nevertheless, the sensing of current output feedback signal is done through a small resistance instead of using a large resistance for better droop action. Hence the power losses due to addition of resistor is mitigated to greater extend in this method, another benefit of this method is the conveniently programing of droop value in the feedback loop.

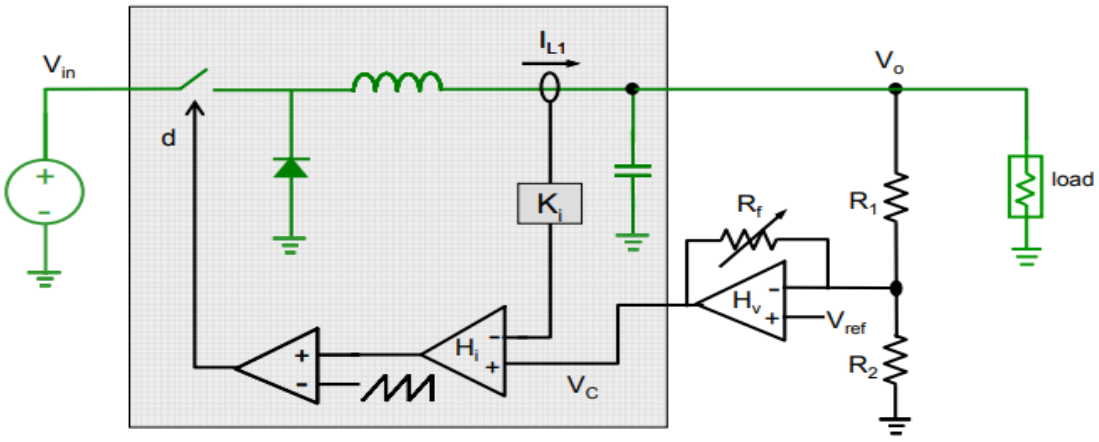


Figure 2.5 Droop action through current output feedback.

This scheme of droop action is also deployed to achieve the function of Active Voltage Position (AVP) in voltage regulators, used to power the microprocessors [45].

(d) Current Mode Control with low DC Gain:

This scheme of droop sharing of current is common among industrial manufacturers and vendors for parallel connection of DC DC converters. This method of droop action is common because of it's comparatively good sharing of load current and good response in transients. The key feature of this method is that the any change in voltage error (difference between set point and actual voltages) causes the control signal that is duty cycle, of the converter to change accordingly to compensate the error. This method is realized by excluding the series capacitor, used for DC isolation in feedback loop of the error amplifier [39] [41] [44]. Thus reducing the DC gain of the error amplifier which leads to induced droop action in voltage output. A schematic of this current mode-controlled module with a finite DC gain is illustrated in below Figure 2.6.

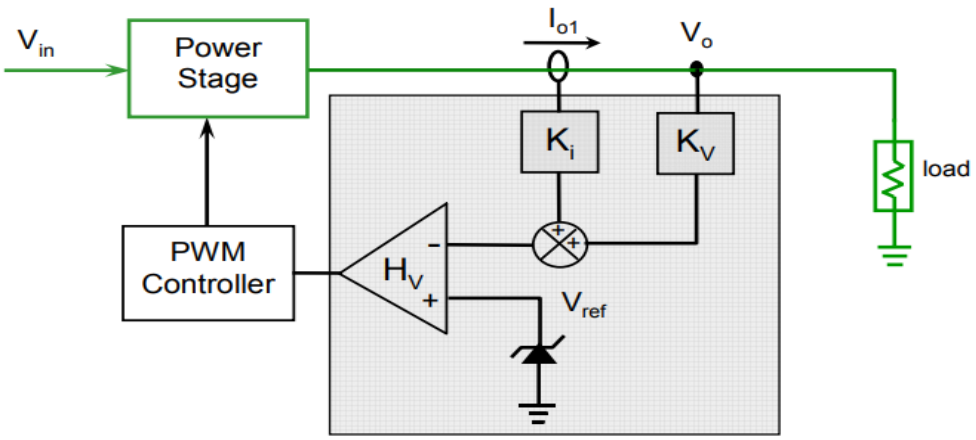


Figure 2.6: Current mode control with low voltage compensator gain of a converter.

The droop induced in this mode is derived as follow:

$$V_0 = V_{o'} - I_{l_1}\frac{R_1}{R_f}K_i \qquad \textbf{2.5}$$

$$V_{o'} = V_{ref}(1 + \frac{R_1}{R_2} - \frac{R_1}{R_f}) \qquad \textbf{2.6}$$

K_i = Compensator gain of current.

$V_{o'}$= Initial resultant voltage output.

Hence, resultant droop resistance is then given by:

$$R_{droop} = K_i \frac{R_1}{R_f} \qquad \textbf{2.7}$$

(e) Summery:

Even though there are several approaches for implementing droop sharing of current methods on parallelly connected converters in a DC micro-grid, the modules connected in parallel have same output characteristics. As a result, steady state and transient behaviors of each module also similar. So, it is straightforward to investigate the limitations of droop sharing of current methods through examples involving current feedback signal.

2.2.2 Investigation on The Regulation of voltage Issues in Droop Methods

In literature [12] the study of precision of sharing of current realized through droop method is conducted, the deviation between current output of each converter is calculated via the mismatch between the voltage output of each and every converter/module and the reference voltage and droop resistance R_{droop}. Supposing the same output resistance values, Figure 2.7(a)(b) shows the dependency of precision of the sharing of current denoted by δI_{o_max} and the mismatch of the reference voltages by δV_{o_SPA}. Then the steady-state sharing of current error is determined by following formula:

$$\delta I_{ss} = \frac{\delta I_{o\_max}}{I_{o\_avg}} \qquad \textbf{2.8}$$

I_{o_avg} : Average current output of all modules connected in parallel.

While there is specific requirement of precision for voltage output to meet, regardless of the loading conditions. This implies that the sizing of R_{droop} is constrained to limited value, else $2*\delta V_{o\_SPA}$ in Fig 2.7(b) would increase which will result in the poor regulation of voltage and hence no desired voltage output level on DC bus.

That being the case, a large R_{droop} is required for a enhanced precision of sharing of current. While at the same time, R_{droop} should be kept small in order to ensure a proper regulation of voltage and to achieve a desired reference of voltage on DC bus. Thus this the main tradeoff between sharing of current precision and proper regulation of voltage in droop methods.

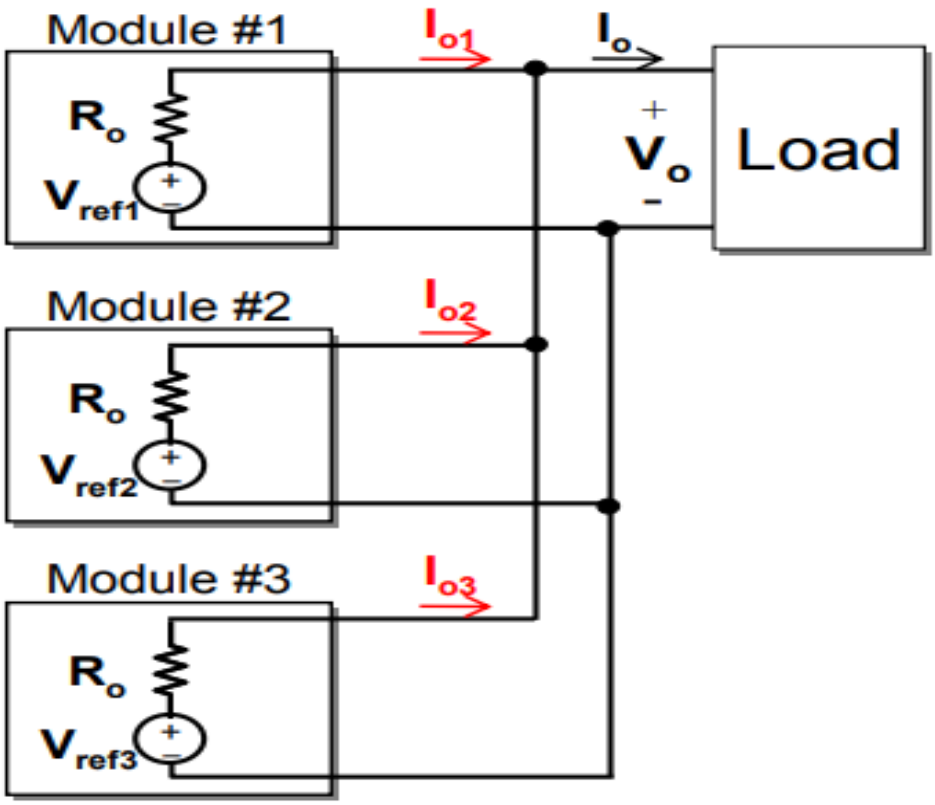


Figure 2.7(a): Parallel connected converters through Droop sharing of current.

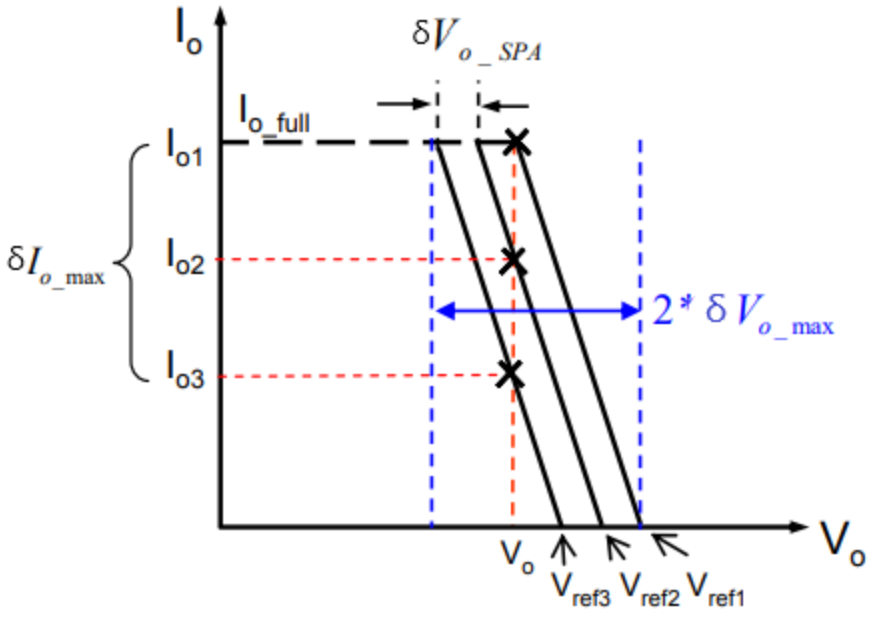


Figure2.7(b): Tradeoff between sharing of current precision and regulation of voltage.

An example is illustrated in Figure 2.9, reported in literature [46] of a parallel connected converters in Regulation of voltage Mode VRM based on intel's specifications [47], the voltage output precision is set to be ±5%. While set point precision through out the life span and temperature of the modules is ±0.8%. Based on these conditions, it is determined that the relative sharing of current error on full loading condition is 25%, which is far higher than the requirement of 10%.

Meanwhile, to keep the full sharing of load current precision below 10%, it is crucial to to have the voltage output setpoint precision better than ±0.35%. However, the set-point-precision of ±0.35% over the life span and temperature of the module is not doable and maintainable provided the cost constraints.

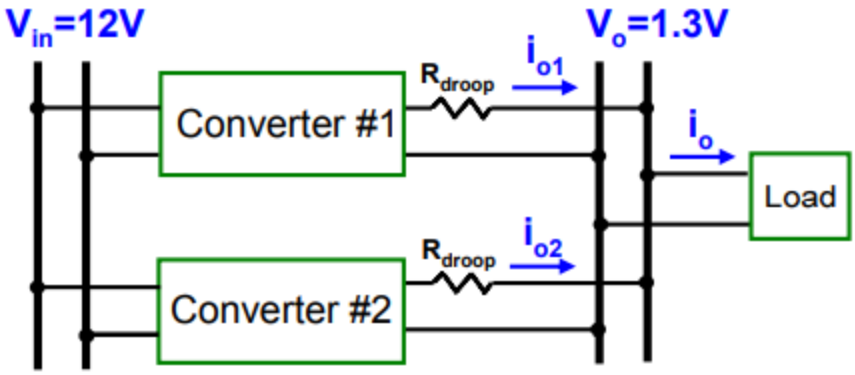


Figure 2.8: Parallel connected power system based on Intel's specifications for a fair cost-efficient system.

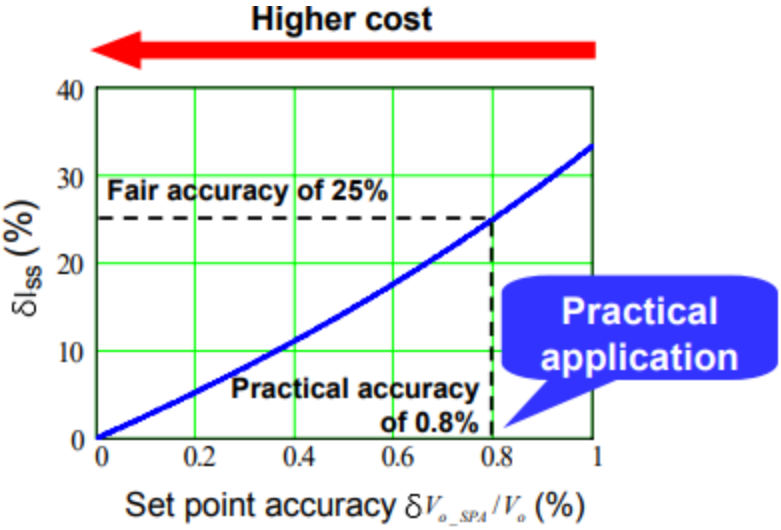


Figure 2.9: Tradeoff between practical precision and steady state error of sharing of current.

In summary, there exists a tradeoff between sharing of current precision and regulation of voltage in methods of passive droop sharing of current. Therefore, this method is applicable where precision requirement of sharing of current is low.

2.3 ACS Methods:

Given the fact that, the droop method of sharing of current suffers from aforementioned regulation of voltage problems, the ACS scheme was developed to mitigate these issues in parallel connected DC DC converters for proper sharing of load current. Most of these ACS techniques have basic functionality of signal processing/sensing of current error between modules connected in parallel. The processed error signal then generally provides a common current reference signal. Every module then adjusts their respective control input to follow the reference, thus evenly distributing and proper sharing of load current among these modules.

2.3.1 ACS Method Configurations:

To resolve the issues encountered while applying droop sharing of current methods, ACS approach has been adopted. The ACS is realized through the proper combination of two arrangements, these two arrangements are:

(a) Control Structure: The arrangement of sharing of current loop in relation to regulation of voltage loop. The arrangement is classified into three classes namely Inner Loop, Outer Loop and External/Dual Loop Regulation.

(b) Bus Program Method: The organization and flow of common current reference through sharing of current bus among converters. There are two main methods namely Average Sharing of current Scheme and Master-Slave Control Scheme.

2.3.1.1 Control Structures

(i) Inner Loop Regulation Mode:

This mode of control operation is realized with the deployment of a processing unit used to process the sharing of current signal inside the regulation of voltage loop as illustrated in Figure 2.10. The V_{err} in Figure 2.10 is the mismatch between reference voltage and actual voltage on the terminal of each converter. This V_{err} creates a sharing of current bus CS_Bus which is basically the communication line carrying the information of current from other modules, feeding this signal to the current regulation loop of each converter to generate the reference current signal, and inductor current of each converter follows this reference current signal. The scheme is depicted in Figure 2.10.

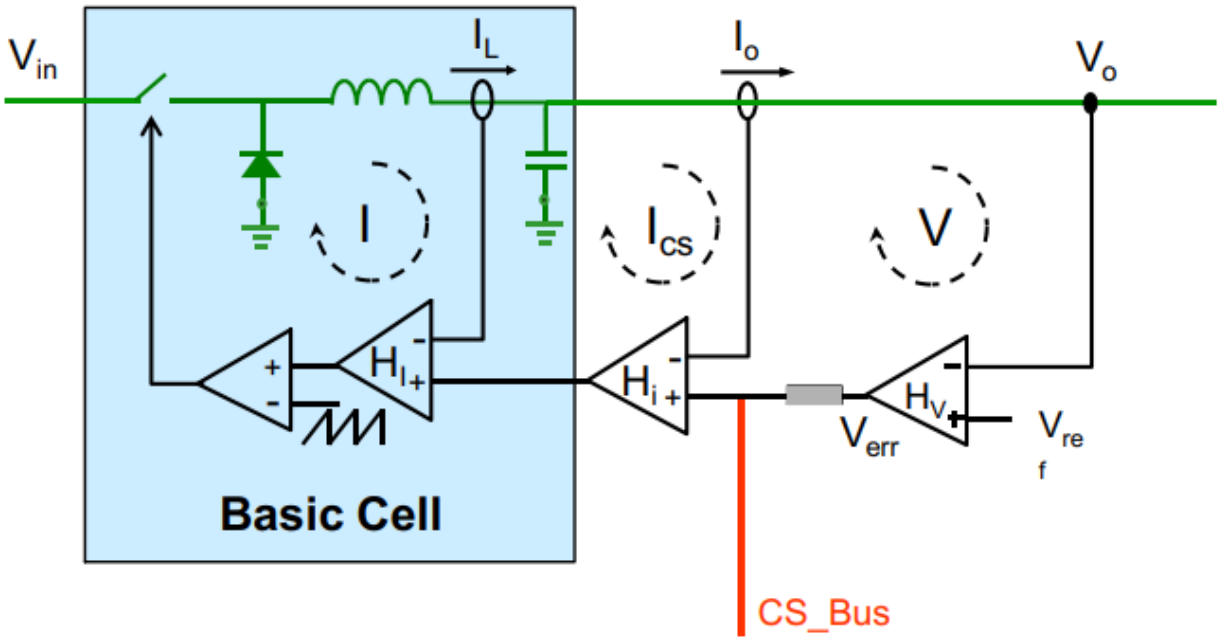


Figure 2.10: Inner Loop Regulation.

(ii) Outer Loop Regulation Mode

In this mode of regulation, by using the signal of sharing of current error, the voltage output of every module is adjusted until the proper and equal sharing of load current is realized. This mode of control operation is realized with the deployment of a processing unit used to process the sharing of current signal outside the regulation of voltage loop as illustrated in Figure 2.11.

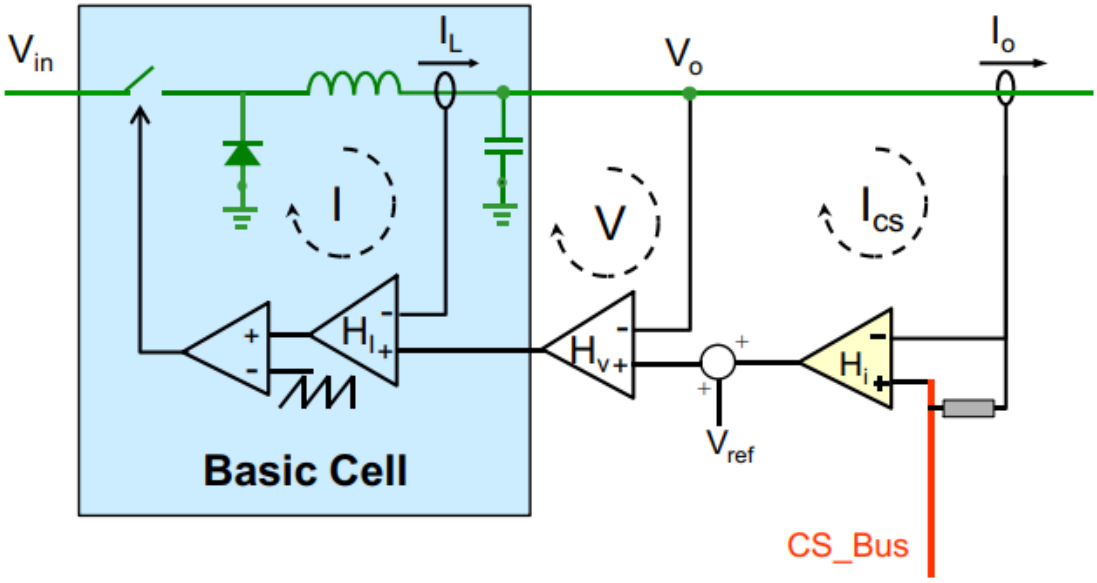


Figure 2.11 Outer Loop Regulation

(iii) External/Dual Loop Regulation:

All the current output provided by each module connected in parallel is compared with sharing of load current signal through a sharing of current bus Ics at each module. This sharing of current loop is placed in parallel with regulation of voltage loop and fed to the basic cell as depicted in Figure 2.12. The proper balanced sharing of load current among the module is realized by adjusting the current feedback controller for each converter.

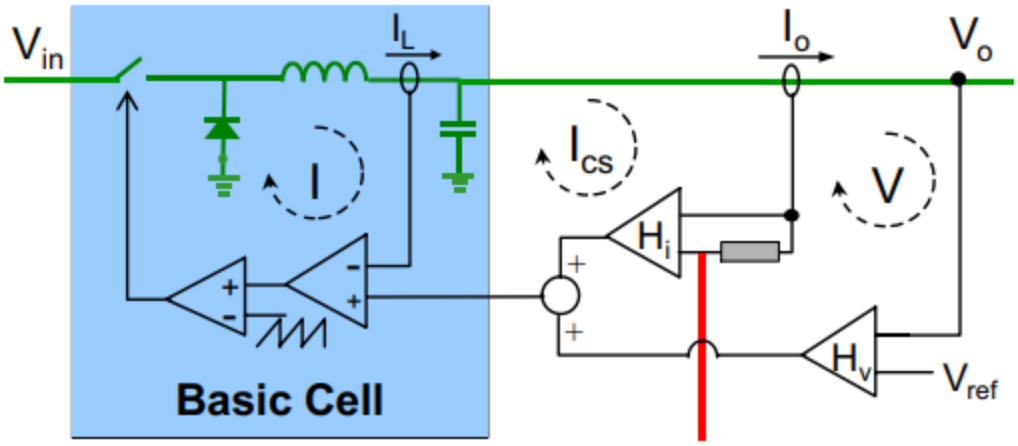


Figure 2.12 External/Dual Loop Regulation.

2.3.1.2 Bus Programing Method:

(i) Master-Slave Method

This scheme of bus programing to achieve the control objectives which is proper regulation of voltage and equal sharing of load current among parallel connected modules, is reported in literature proposed [48][49][50][51][52]. One of the key benefits of this scheme is that this scheme can be applied to non-identical DC DC converters and can be also applied on different types of converters in parallel mode of operation. The theory behind this scheme, as its name suggests, has one single module working as master deciding the current reference signal and set for slave converters, following this current reference signal generated by the master converter. The Master-Slave method is depicted in below figure 2.13.

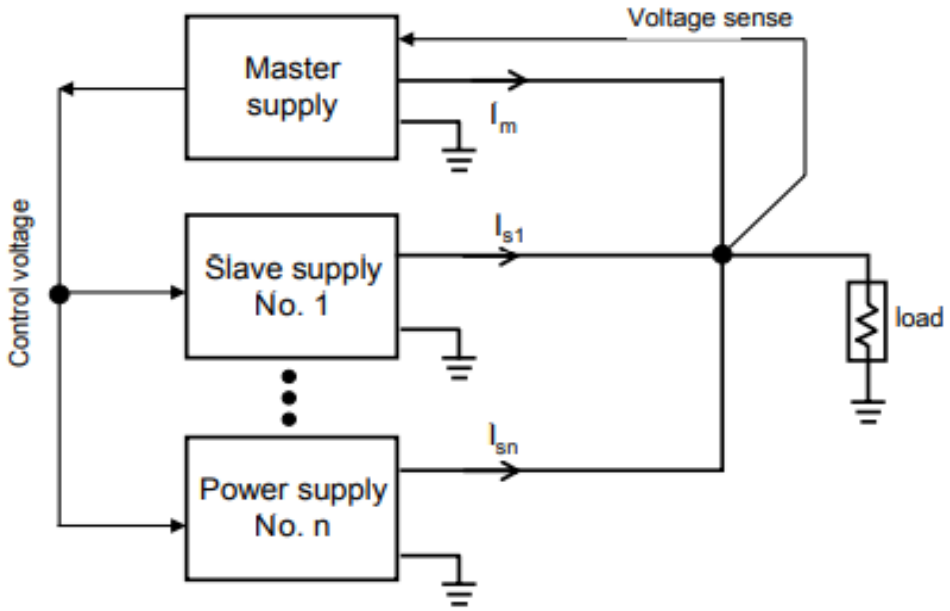


Figure 2.13: General Block Diagram of Master-Slave configuration.

The configuration of the master-slave scheme is doable in several ways. The current mode control converters is the earliest configuration presented in literature [53][54], the Figure 2.14 shows this implementation, where the modules connected in parallel are controlled with the help of feedback signals of voltage output and inductor currents of the converters. As it can be seen from Figure 2.14, the compensation of voltage is being done through a single voltage compensator in master converter only, so there exists no point at issue due to different voltage set points as reference. The single voltage compensation loop in master converter programs the current levels for all the converters and hence an accurate sharing of current is ensured. Meanwhile the voltage output that is the DC bus voltage is regulated by master converter, the proper regulation of voltage is also obtained. So the sharing of current precision is improved to greater extent while ensuring proper regulation of voltages, than in droop methods.

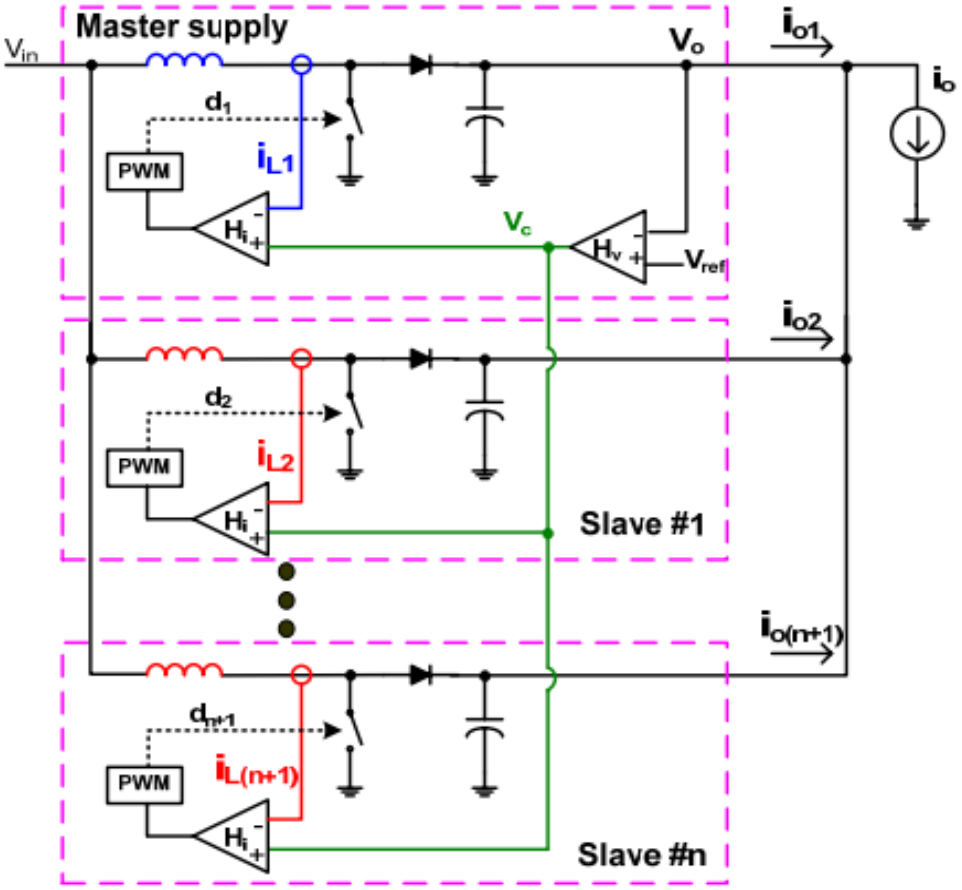


Figure 2.14: Sharing of current through Master-Slave Bus Program with Current Control Mode.

That being the case, the key benefit of the master-slave sharing of current technique is the proper sharing of current during transient as well as at steady state. However, the drawback of this techniques is also apparent as a failure of one converter (master) will cause a failure of the whole power system or DC microgrid in our case. For an example, as illustrated in Figure 2.5, if a fault occurs at voltage compensation loop in master unit or any other type of fault which disables the functionality of the master converter, both the sharing of current and regulation of voltage would be failed. As the master converter's structure is different from slave converters, they are not interchangeable hence making the whole system complicated and less recoverable. To overcome this disadvantage other approaches are proposed.

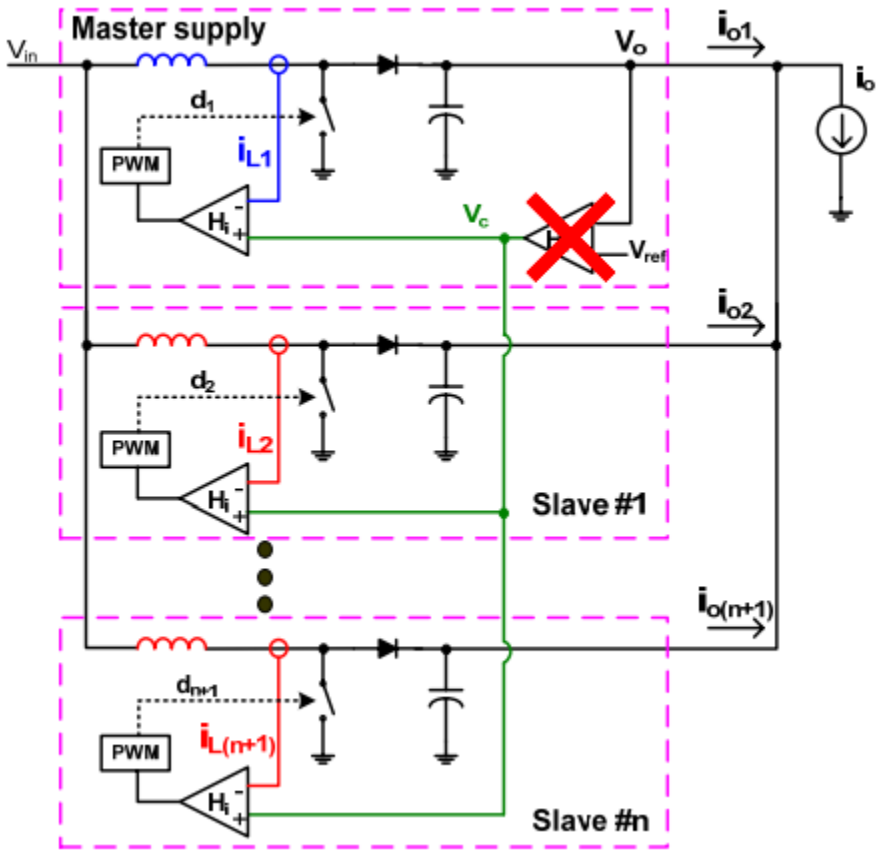


Figure 2.15: A faulty master module in parallel connected converters through master-slave configuration.

(ii) Democratic Configuration:

From the point of view of reliability, ACS approaches which ensures the proper sharing of current without making the system more complex by the implementation of an extra controller for sharing of current or master-slave configurations. In the democratic configuration, as it's obvious from the name, each and every converter is responsible for the sharing of load current and regulation of voltage either in stand alone or in parallel combination, allowing the feature of redundancy and scaling of the power system. Normally this type of configuration can be administered via two methods. The first method is passive droop sharing of current as discussed in detail in previous section 2.2 of this chapter. Passive droop sharing of current techniques are straightforward to implement and understand and does not depend on communication between the parallelly connected converters. Nonetheless, the main drawback of droop method is the existence of a tradeoff between proper sharing of load current and bus regulation of voltage, hence these methods are not applicable to the systems where there is requirement of proper and good regulation of voltage. Second method to implement the democratic configuration is through active feedback control. A single communication wire, sharing of current bus (CS_bus) is required to share the current reference to each converter connected in parallel. At the same time, though every individual module have their own voltage compensation loop, consisting of voltage sensors and reference circuitry, all the parallelly connected converters required to be regulated and should track the voltage reference signal at DC bus. This technique thus resolves the tradeoff between regulation of voltage and sharing of current. In literature [55]-[61] different methods were reported and proposed. In [55] an automatic average output sharing of current is propose. In the proposed scheme the reference voltage in voltage compensation loop ($\mathbf{V_{\_comp}}$), is adjusted by the sharing of current error signal from sharing of current compensation loop ($\mathbf{I_{\_comp}}$), so as to generate the required duty cycle to annihilate the deviation of current output of each module from the average current on CS_bus as illustrated in Figure 2.16. Since all the voltage and current error compensations are being done locally in every converter, there is no role of master-slave converters left in this proposed method. The average current is routed to all modules through a CS_bus by providing a connection to all current output through

identical resistors. Hence with a high gain of **I_comp**, current output of each converter is bounded to follow the CS_bus signal.

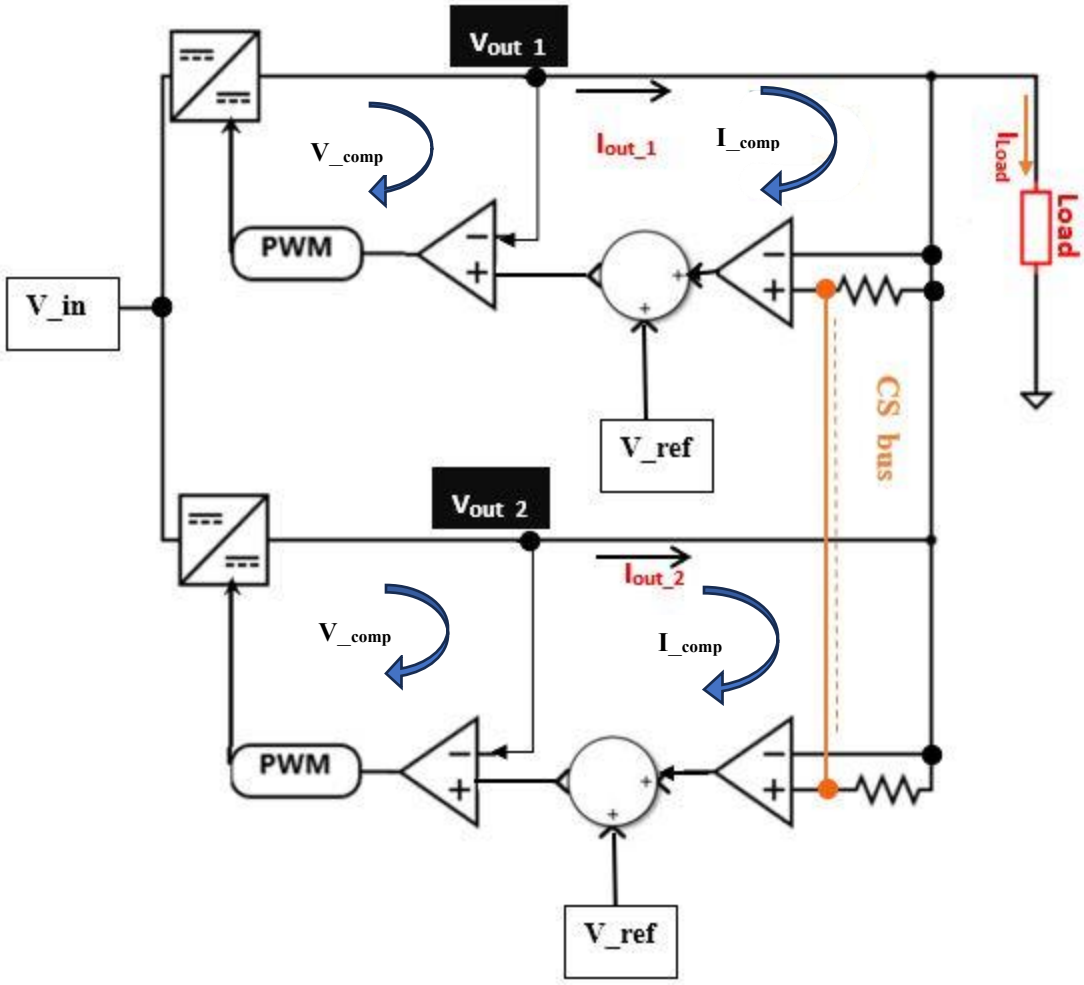


Figure 2.16: Autonomous sharing of current.

The above scheme in Figure 2.16, it obvious that the fault tolerance of the system is poor. On account of the failure of one module will result in the failure of the whole system. Hence for this reason extra circuitry for protection is necessary to cut out the injection of sharing of current signal into CS_bus from faulty module. One of the simplest solutions to this problem is proposed in different literature for improved democratic configuration, is to replace the resistors, through which modules are connected to CS_bus, with diodes. Therefore, the CS_bus will have the highest current among the converters in parallel connection because of the fact that forward biasing of the

diodes will be done only by the converters having highest current output. The voltage on CS_bus, will be an input command for the converters with initially lower current output, this will lead to the adjustment of the reference voltages to higher levels of modules with lower current output to increase their current output, until the voltage on output of the compensator of current loop equals to the voltage on CS_bus. Hence the role of master-slave will be determined automatically.

2.4 Limitations Of The Existing Methods:

The general purpose of the ACS techniques is to ensure the proper regulation of voltage and balanced sharing of load current among parallelly connected converters. Although these methods provide better performance than droop sharing of current methods but they also have several limitations which should be considered. The key limitations which restrict the deployment of this methods are mentioned below and goal of this work is to curb these limitations by designing an optimal control scheme for the parallelly connected converters, forming an islanded DC micro grid.

Precision and Precision: ACS methods rely on feedback control loops to regulate the sharing of current among modules. However, achieving precise and accurate sharing of current can be challenging due to variations in component tolerances, parameter drift, and differences in dynamic response. This can lead to imbalances in sharing of current, especially under light load or transient conditions.

Complexity and Cost: Implementing ACS methods requires additional circuitry, such as current sensing elements, amplifiers, and control loops. This complexity increases the cost and board space requirements of the overall power supply system. Moreover, the design and calibration of these circuits can be time-consuming and may require specialized expertise.

Dependency on Matching: ACS methods typically require a good match between the modules in terms of their electrical characteristics, such as output impedance and regulation of voltage. Small differences in these parameters can affect the precision of sharing of current. Achieving close matching between modules can be challenging and may limit the flexibility in module selection or replacement.

Dynamic Response and Transients: ACS methods may exhibit limitations in dynamic response during load transients or sudden changes in load conditions. The control loops may have a finite response time, which can result in temporary imbalances in sharing of current until the control system adjusts. This can impact the system's stability and transient performance.

Sensitivity to External Factors: ACS methods can be sensitive to external factors such as changes in ambient temperature, input voltage variations, and component aging. These factors can affect the precision of current sensing, introduce additional errors, and impact the overall sharing of current performance.

Scalability: Scaling up the number of converters/modules in a parallel configuration can introduce additional challenges in achieving reliable and accurate sharing of current. As the number of modules increases, the complexity of the control system and the inter-module communication may become more demanding. Ensuring consistent performance and stability across a large number of modules can be difficult.

Failure Modes: In some cases, the failure of a single module can disrupt the sharing of current balance and cause excessive loading on the remaining modules. ACSmethods should include provisions to handle module failures and prevent cascading failures that could lead to system shutdown or damage.

It's important to carefully evaluate these limitations and consider the specific requirements and constraints of the power supply system before implementing ACS methods.

Chapter 3

DC Micro-Grid System:

The theory and design of the DC DC converters, forming a major part of the DC microgrid power system is discussed in this chapter. The designing and selection of the DC DC converters are done on basis of commercially available low to medium power rating typically used for renewable energy resources (RES). The laboratory based 98 watts power DC microgrid consisting of two Single Ended Primary Inductor Converter (SEPIC) as energy source converter, connected in parallel feeding power to the load connected in DC bus is designed. The parallelly connected converters are designed to maintain any voltage set point on DC bus between 70V-95V, depending on the reference input. The two SEPIC converters operate from an input voltage within the range of 80V – 100V and provide any desired/reference voltage output between 70V and 95V. Figure 2.17 shows the DC microgrid setup developed for this work.

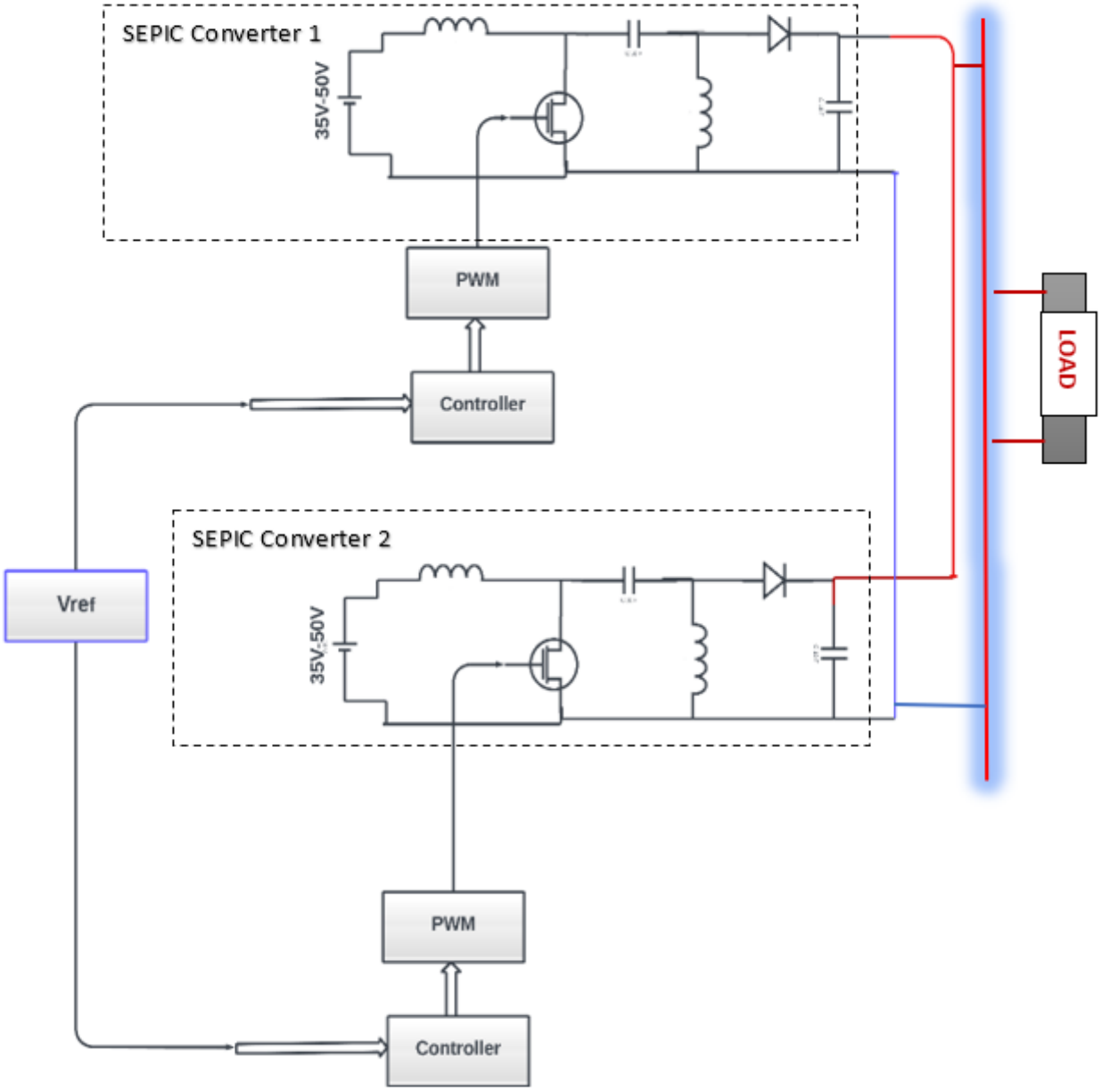


Figure 3.1: Two SEPIC Parallelly connected converters Forming a DC Micro-Grid.

3.1 DC DC Converters:

Devices which have capability of converting one DC voltage level to another DC voltage level are known as DC DC converters. These devices are composed of power electrics and both controlled and uncontrolled switching power electronic components. DC DC converters have two main topologies, Boost and Buck converter. DC DC converters are preferred choice when integrating RES (generally photovoltaics PV) with DC microgrids. Microgrid designers and researchers generally consider custom topology converters like boot, buck, buck-boost, SEPIC, flyback, cuck, dual active bridge and push-pull converters, as well as several other converters which enables the designers and researchers, to achieve less voltage stress on convert's switch, high gain and less duty cycles. [20][26].

In DC voltage level conversitions, diodes and voltage bridges are useful for reducing the voltage level for a desired level, but can not be sufficent. For a refrence voltage generation voltage regulators are used. Energy Storage Systems (ESS) like batteries, are used to support the microgrids as backups or as power factor corrections, the voltage level of batteries decreases as batteries discharge and their health also gets degraded over their life span this can cause several problems if there is no proper voltage control actions. One of the most effiecent and straightforward methods to regulate the voltage through circuits is by the deployment of DC DC converters and their proper control design. Generally there are five main types of DC DC converters. **Buck Converters:** These converters can only reduce the voltage levels. **Boost Converters:** Boost converters can only increase the voltage levels. **Buck-Boost, Cuk** and **SEPIC Converters:** The converters have capability of both increasing and decreasing the voltage levels, each of one having their limitations and tradeoffs.

Depending on the application and desired specifications of converters they only need to increase or decrease the voltage levels by using the corresponding converters. However, if the desired voltage output level is in the range of input voltage levels, it is general trend to use converters which can perform both increasing and decreasing the voltage level. Buck-Boost converters can be a suitable option for this application interms of cost and simipilicity because of the fact that this

converter has only one inductor and one capacitor. However, high levels of input current ripples is the main drawback of these converters which limits it's application.

This high ripple induces harmonics in circuit, curbing these induced harmonics is sometime necesserary in many applications, which requires a bulky and large capacitors or an Inductor Captacitor filters (LC filter). This makes the deplyoment of Buck-Boost converters ineffiecent and sometimes costly. Another major issue of this Buck-Boost converter topology is they invert the voltage output. To mitigate this voltage inversion and high input current ripple, Cuk converters, by using extra inductor and capcitor in it's circuit, can be a good replacement of Buck-Boost converter topology. But both Buck-Boost and Cuk converters induces electrical and thermal stress on the power electronic cmponents which leads to the rapid degradition of performance of these components and sometimes total failure. To over come these disadvantages SEPIC converters are proposed with proper control design.

3.1.1 Single Ended Primary Inductor Converter - SEPIC:

(a) Topology:

Figure 3.2 illustrates a circuit diagram of SEPIC. SEPIC converter is the modified form Boost converter topology. A capacitor $\mathbf{C_1}$ is inserted between the diode $\mathbf{D_1}$ and inductor $\mathbf{L_1}$. Clearly this added capacitor $\mathbf{C_1}$ cutoffs the path for DC current flow between the input and output. Meanwhile, the diode $\mathbf{D_1}$ anode needs to be connected to suitable potential in order to achieve the proper forward and reverse biasing of this diode $\mathbf{D_1}$. This can be realized by grounding diode $\mathbf{D_1}$ through another inductor $\mathbf{L_2}$. This inductor $\mathbf{L_2}$ can operate separately or coupled to inductor $\mathbf{L_1}$ by wounding both inductors to same core. For a realistic and practical implementation, the SEPIC converter is modeled considering the parasitic resistances $\mathbf{rl_1}$ and $\mathbf{rl_2}$ of both inductors $\mathbf{L_1}$ and $\mathbf{L_2}$ respectively. The control switch **S**, typically a transistor such as IGBT or a MOSFET, is responsible for the proper amount of energy transfer. A proper control design to control this controlled switch **S** through a suitable duty cycle generation is crucial for the proper operation of any converter topology. Based on the high and low pulse of duty cycle (on/off state of the switch **S**) the mode of operation of SEPIC converter is divided into two modes of operation **S1** and **S2**. and the consequent circuits are illustrated in Figure 3.1(a) and Figure 3.1(b) respectively.

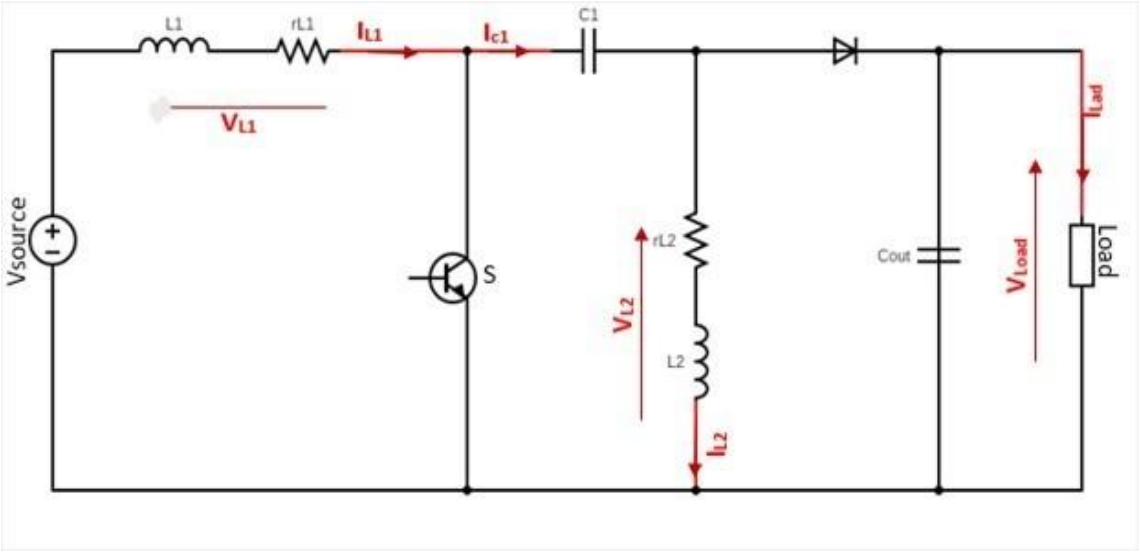


Figure 3.2: Single Ended Primary Inductor Converter-SEPIC

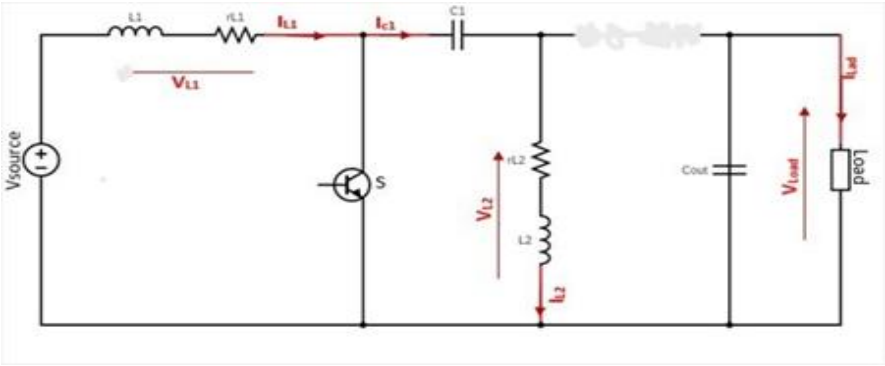


Figure 3.2(a): S1 operation mode of SEPIC.

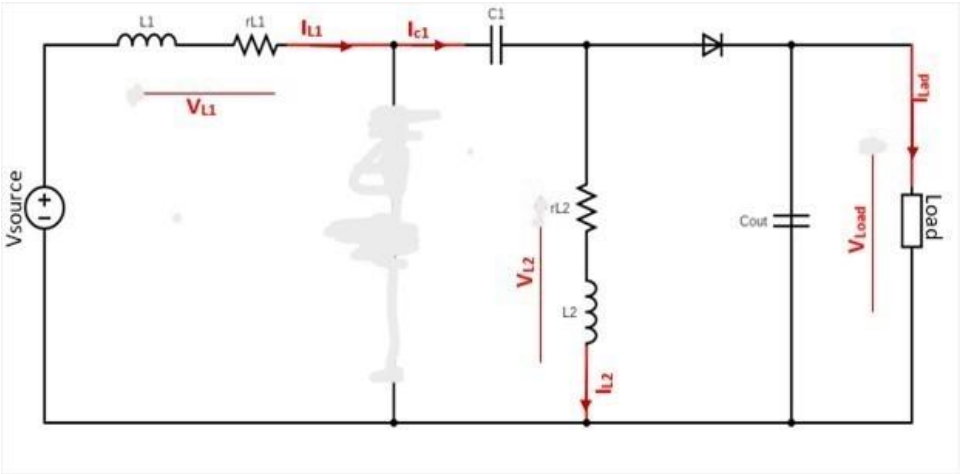


Figure 3.2(b): S2 operation mode of SEPIC.

(b) Operation:

As stated above, the operation mode of SEPIC converters is divided in two modes of operation **S_1** and **S_2**. These modes are divided based on the state of the control switch **S** typically a MOSFET, the control signal being generated from the designed controller is fed to PWM generator, to generate a suitable pulse (high and low) to operate the switch properly.

1) Mode S_1:

During the high level of pulse (on state of MOSFET/closed switch), the voltage on inductor **L_1** is equal to input voltage Vsource that is inductor **L_1** gets charged by the DC source voltage **V_{source}** and the voltage **V_{L2}** across Inductor **L_2** is equal to **$-V_{c1}$** that is inductor **L_2** is charged by the voltage **V_{c1}** of capacitor **C_1**. The diode **D** is reverse biased hence the voltage output to the load Vload is totally maintained by voltage **V_{c_out}** across capacitor **C_{out}.**

2) Mode S_2:

During the low level of pulse (off state of MOSFET/Open switch), the voltage on inductor **L_2** is equal to the voltage output **V_{c_out}**. Meanwhile the voltage across switch **S** is equal to **V_{source} (V_{c1}) + V_{load} (V_{l1})**, so the voltage on **L_1** is equal to that of voltage on load that is **$V_{L1} = V_{Load}$**. In this mode the diode **D** gets forward biased and allows paths for both inductors to discharge through it and supply voltage to the load and charge the capacitors at same time. For the large time period of low level of pulse, the voltage output will be greater because of the fact that the longer the inductors discharge and charge the capacitors the greater their voltage will be, but it should be noted that if the low level period of the pulse remains for a long time the converter will be failed because of insufficient charge on inductor hence a low voltage on capacitor.

This effect is categorized as Continuous Conduction Mode CCM and Discontinuous Conduction Mode DCM, as far as this work is concerned the CCM is considered.

(c) Specifications:

The SEPIC converter should meet the following design requirements shown in table 1.

Table 1: Specifications

$\mathbf{V_{in}}$	100V
$\mathbf{V_{out}}$	70v-230v
$\mathbf{I_{out}}$	2.4A-3A
$\mathbf{F_s}$	50kHz
$\mathbf{\Delta I_{out}}$	0.05
$\mathbf{\Delta V_{out}}$	0.5

(d) Duty Cycle Calculation:

The *buck* and boost capability of SEPIC basically depends on the duty cycle and components parasitic in the circuit.

Output of an ideal SEPIC convert is given by:

$$\boldsymbol{V_{out} = \frac{D * V_{in}}{1 - D}} \qquad 3.1$$

The above equation does not consider the parasitic such as the voltage $\mathbf{V_D}$ =0.5V drop across diode **D.** On including the voltage drop $\mathbf{V_D}$ in equation 3.1, it becomes:

$$\boldsymbol{V_D + V_{out} = \frac{D * V_{in}}{1 - D}} \qquad 3.2$$

To calculate desired duty cycle **D**, the equation 3.2 is manipulated as follow:

$$\boldsymbol{D = \frac{V_D + V_{out}}{V_{in} + V_{out} + V_D}} \qquad 3.3$$

When V_{in} is at minimum which is 60V, the duty cycle D will be maximum denoted as D_{max} and calculated as follow:

$$\boldsymbol{D_{max} = \frac{0.5v + 95v}{60v + 95v + 0.5v} \approx 0.61} \qquad 3.4$$

When V_{in} is at maximum which is 100V, the duty cycle D will be minimum denoted as D_{min} and calculated as follow:

$$\boldsymbol{D_{min} = \frac{0.5v+95v}{100v+95v+0.5v} \approx 0.48} \qquad 3.5$$

(e) Inductor (L_1, L_2) Calculations:

To achieve less voltage and current ripples, the inductance should be greater, greater inductance means bulky inductor device along with the higher costs with higher parasitic resistance. The greater the parasitic resistance, the lesser the efficiency of the converter. Designing the best converter requires inductors which are just large enough to operate under the acceptable range of current and voltage ripples.

The calculation of value for inductance is done as follow:

$$L = \frac{V_{inMin} * D_{max}}{F_s \Delta I_{out}} \qquad 3.6$$

Putting the values in equation 3.6 gives

$$L = \frac{60*0.61}{50*10^3*0.05} \approx \boldsymbol{0.0146 \approx 14.6mH} \qquad 3.7$$

(f) Capacitors (C_1 and C_{out}) Calculations:

Based on the literature [18][19], the voltage ripple of coupling capacitor C_1 and output capacitor C_{out} should be considered different from each other. The ripple voltage on output capacitor C_{out} results in 6 percent voltage draw against the maximum input voltage $V_{in.}$ While coupling capacitor C_1 can cause a reduction of 1 percent of voltage output V_{out}. Based on this, the capacitances of both capacitors can be calculated as follow:

$$C_{1,out} = \frac{I_{out} * D}{\Delta V_{out} * F_s} \qquad 3.8$$

$$C_{1,out} = \frac{2.4*0.61}{0.5*100*50*10^3} \approx 59\text{nf} \qquad 3.9$$

3.1.2 MATHEMATICAL MODEL OF THE SEPIC CONVERTER.

DC DC converters, which have power electronic components as main building blocks, are types of circuits which are considered to be difficult while modeling them. This is due to the fact that the differential equations which govern them have discontinuities [ZRG03], this makes them the hybrid systems. Passive elements in DC DC converter modules are responsible for the generation of continuous behavior of the converter module, such as voltage and current waveforms. Controlled switching actions are offered by switching devices such as Metal Oxide Field Effect Transistors (MOSFETs) or Insulated Gate Bipolar Transistors (IGBTs). Uncontrolled switching phenomenon is generated by diodes.

The hybrid modeling of SEPIC is straightforward. Hybrid models includes the behavior of the circuit unlike other modeling techniques [VRGL10]. Hence a hybrid model is an accurate representation of the DC DC converters in governing equations form describing the dynamic characteristics of an actual system, however the hybrid model does not cater for the transient behavior at the very initial period of switching.

As illustrated in figure 3.1, the SEPIC is being controlled with a switching device that is MOSFET, both the switching devices MOSFET and diodes are assumed to be ideal and have no voltage drop across them. Also the important assumption throughout this work is that the SEPIC is in CCM, in other words the current on diode D never falls to zero during the S_2 mode of operation the converter. These assumptions prompt to two different states of the circuit that is S_1 and S_2 or ON and OFF state of the switch, then on applying the KVL and KCL on the relative circuits, the consequent governing differential equations for relative states, which also represents a combined model of continues and discrete phenomena of circuit, is modeled in next page.

3.1.2.1 Hybrid State Space Model of SEPIC:

The state space hybrid model is constructed while considering the parasitic components of inductors, represented by ESRs, rL_1 and rL_2.

The two state space models (when the control input is 0 or 1), in form of matrices can be represented in form of generic state-space equations as:

$$\begin{cases} \dot{X} = A_1\dot{x} + B_1 u \\ y = C_1^T x \end{cases} \quad 3.11$$

$$\begin{cases} \dot{X} = A_2\dot{x} + B_2 u \\ y = C_2^T x \end{cases} \quad 3.12$$

where,

A_1, B_1, C_1: represents the circuit component states when control input D=1.

A_2, B_2, C_2: represents the circuit component states when control input D=0.

x: represents the state vectors that is $[i_{L1}\ i_{L2}\ V_{c1}\ V_{c\_out}\ ]^T = [\ x_1\ x_2\ x_3\ x_4\ ]^T$

u: represents the input vector

C_1 and C_2: represents the circuit component's state responsible for the output i.e [0 0 0 1].

On applying KVL and KCL on the circuit, we get the governing equations/mathematical model of the converter for the two mode as follow:

ON State/ S_1 Mode:

$$\frac{di_{L1}}{dt} * \boldsymbol{L_1} = \boldsymbol{V_{in}} - \boldsymbol{i_{L1}} * \boldsymbol{rL_1} \quad 3.13$$

$$\frac{di_{L2}}{dt} * \boldsymbol{L_2} = -\boldsymbol{i_{L2}} * \boldsymbol{rL_2} - \boldsymbol{V_{C1}} \quad 3.14$$

$$\frac{dv_{c1}}{dt} * \boldsymbol{C_1} = \boldsymbol{i_{L2}} \quad 3.15$$

$$\frac{dv_{C\_out}}{dt} * \boldsymbol{C_{out}} = \frac{V_{C\_out}}{R_{Load}} \qquad 3.16$$

OFF State/S_2 Mode:

$$\frac{di_{L1}}{dt} * \boldsymbol{L_1} = -\boldsymbol{i_{L1}} * \boldsymbol{rL_1} - \boldsymbol{V_{C\_out}} - \boldsymbol{V_{C1}} + \boldsymbol{V_{in}} \qquad 3.17$$

$$\frac{di_{L2}}{dt} * \boldsymbol{L_2} = -\boldsymbol{i_{L2}} * \boldsymbol{rL_2} + \boldsymbol{V_{C\_out}} \qquad 3.18$$

$$\frac{dv_{c1}}{dt} * \boldsymbol{C_1} = \boldsymbol{i_{L1}} \qquad 3.19$$

$$\frac{dv_{C\_out}}{dt} * \boldsymbol{C_{out}} = \boldsymbol{i_{L1}} - \boldsymbol{i_{L2}} - \frac{\boldsymbol{V_{C\_out}}}{\boldsymbol{R_{Load}}} \qquad 3.20$$

The state space representation of the two operation mode of the converter, based on equations 3.11-3.18 is done as follow:

ON State/ S_1 Mode:

$$\begin{bmatrix} \dot{\boldsymbol{i_{L1}}} \\ \dot{\boldsymbol{i_{L2}}} \\ \dot{\boldsymbol{V_{C1}}} \\ \dot{\boldsymbol{V_{Cout}}} \end{bmatrix} = \begin{bmatrix} -\frac{rL_1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{rL_2}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & \frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_{Load}C_{out}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{c1} \\ V_{Cout} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}] \qquad 3.21$$

Or

$$\dot{X} = A_1 x + B_1 u$$

OFF State/S_2 Mode:

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{V}_{C1} \\ \dot{V}_{Cout} \end{bmatrix} = \begin{bmatrix} -\frac{rL_1}{L_1} & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ -\frac{rL_2}{L_2} & 0 & 0 & \frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_{out}} & -\frac{1}{C_1} & 0 & -\frac{1}{R_{Load}C_{out}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{c1} \\ V_{Cout} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}] \qquad 3.22$$

Or

$$\dot{X} = A_2 x + B_2 u$$

The above representations 3.21 and 3.22 can be combined into single model by the introduction of control input u {1,0}or{u, 1-u}, then the unified model can be represented as follow:

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{V}_{C1} \\ \dot{V}_{Cout} \end{bmatrix} = \begin{bmatrix} -\frac{rL_1}{L_1} & 0 & \frac{u-1}{L_1} & \frac{u-1}{L_1} \\ -\frac{rL_2}{L_2} & 0 & -\frac{u}{L_1} & \frac{1-u}{L_2} \\ \frac{1-u}{C_1} & \frac{u}{C_1} & 0 & 0 \\ \frac{1-u}{C_{out}} & \frac{1-u}{C_1} & 0 & -\frac{1}{R_{Load}C_{out}} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{c1} \\ V_{Cout} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}] \qquad 3.23$$

$$\dot{X} = Ax + BV_{in}$$
$$y = C^T x \qquad 3.24$$

Where,

$A = A_1*u + A_2*(1-u)$

$B = B_1*u + B_2*(1-u)$

$C = C_1*u + C_2*(1-u)$

As the combined representation in 3.23 is clearly a hybrid model, as the system's dynamics is represented in both discrete and continuous variables. The key issue in this model representation is the hybrid dynamics itself, as with the change of mode of operation to ON or OFF, circuit topology changes as well, so does their associated linear continuous time properties. To over come this issue Average State Space models are adopted in control theory.

3.1.2.2 Average Model of SEPIC:

A well-known mathematical model for control design of systems with hybrid natures is modeling through average state space techniques. In this method, by assuming that the natural frequency of the DC DC converter is much smaller than the switching frequency F_s of converter, then the state space model is constructed by using the average values of the state vectors of the hybrid state space model. By defining a duty cycle "d", averaging of the state space equations 3.11 and 3.12 for ON (d) and OFF(1-d) modes of switch is done over a time period of $T_{switch} = 1/F_s$, the average model thus obtained as follow:

$$\begin{cases} \dot{\boldsymbol{x}} = (\boldsymbol{dA_1} + (\boldsymbol{1-d})\boldsymbol{A_2})\boldsymbol{x} + (\boldsymbol{dB_1} + (\boldsymbol{1-d})\boldsymbol{B_2})\boldsymbol{V_{in}} \\ \boldsymbol{y} = \left(\boldsymbol{dC_1^T} + (\boldsymbol{1-d})\boldsymbol{C_2^T}\right)\boldsymbol{x} \end{cases} \qquad 3.25$$

As control input signal is d, the average state space model is obviously a bilinear system model. This bilinear model of the system has feature of representing the system dynamics not only around an equilibrium (steady state point) but also over a wide range of operation (transients). The nonlinear control theory deals and designs controllers based on these types of bilinear models, Although the development of nonlinear controller is not the scope of this work however the linear controller developed in this study for single stage SEPIC and study the results of this controller in parallel operation of average model of SEPIC is the scope this study. So, for single stage SEPIC this average model needs to be linearized around an operating point in order to apply linear control theory and develop a linear controller for SEPIC converter and study the step response.

3.1.2.3 Linearization of the Average Model of SEPIC:

To approximate the behavior and properties of non linear systems, small signal modeling and analysis methods are common among engineers and scientists. From nonlinear model equation 3.25, by linearizing this equation around an operating point, a small signal, linear model of the SEPIC converter can be realized to design an optimized linear control law for the SEPIC converters to be connected in parallel to form a DC microgrid.

The variables in no linear average state space equation 3.5 are each perturb with their small signals around an equilibrium/steady state operating point as follow:

$$\begin{cases} x = X + \hat{x} \\ d = D + \hat{d} \\ V_{in} = Vin + \widehat{V_{in}} \\ y = Y + \hat{Y} \end{cases} \qquad 3.26$$

Where,

$\begin{cases} X \\ D \\ Vin \\ Y \end{cases}$ Steady state values

$\begin{cases} \hat{x} \\ \hat{d} \\ \widehat{V_{in}} \\ \hat{Y} \end{cases}$ Small signal values

The steady state values can be obtained from equation 3.24 by assuming $\dot{x} \rightarrow 0$ as follow:

$$\begin{cases} 0 = AX + BV_{in} \\ Y = C^T X \end{cases}$$

$$\begin{cases} X = -A^{-1}BV_{in} \\ Y = -C^T A^{-1}BV_{in} \end{cases} \qquad 3.27$$

Using equation 3.27 in 3.25 gives:

$$\begin{cases} \dot{\hat{x}} = [A_1(D + \hat{d}) + A_2(1 - D - \hat{d})](X + \hat{x}) + [B_1(D + \hat{d}) + B_2(1 - D - \hat{d})](Vin + \widehat{V_{in}}) \\ \hat{y} = C_1^T(X + \hat{x})(D + \hat{d}) + C_2^T(X + \hat{x})(1 - D - \hat{d}) \end{cases} \qquad 3.28$$

Since the product of small terms results is even smaller numbers so they can be neglected, hence products of small terms like $\hat{x}\,\hat{d}$ and $\widehat{V_{in}}\hat{d}$ can be neglected, this leads to the overall simplified small signal dynamic model as follow:

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + B\widehat{V_{in}} + [(A_1 - A_2)X + (B_1 - B_2)Vin]\hat{d} \\ \hat{y} = C^T\hat{x} + (C_1^T - C_2^T)X\hat{d} \end{cases} \qquad 3.29$$

Equation 3.29 is a small signal linear model, the significance of this equation is the application of this equation in linear control tools to design the control law for the dynamic system.

3.2 Finalized State-Space Model in MATLAB:

Figure 3.3 shows the finalized version of the implementation of above discussed steps involved in developing the state space model for SEPIC. Also the transfer function of SEPIC model is depicted in figure 3.4, this transfer function is used in chapter 4 for the discussion of step response analysis of open and close loop system of SEPIC.

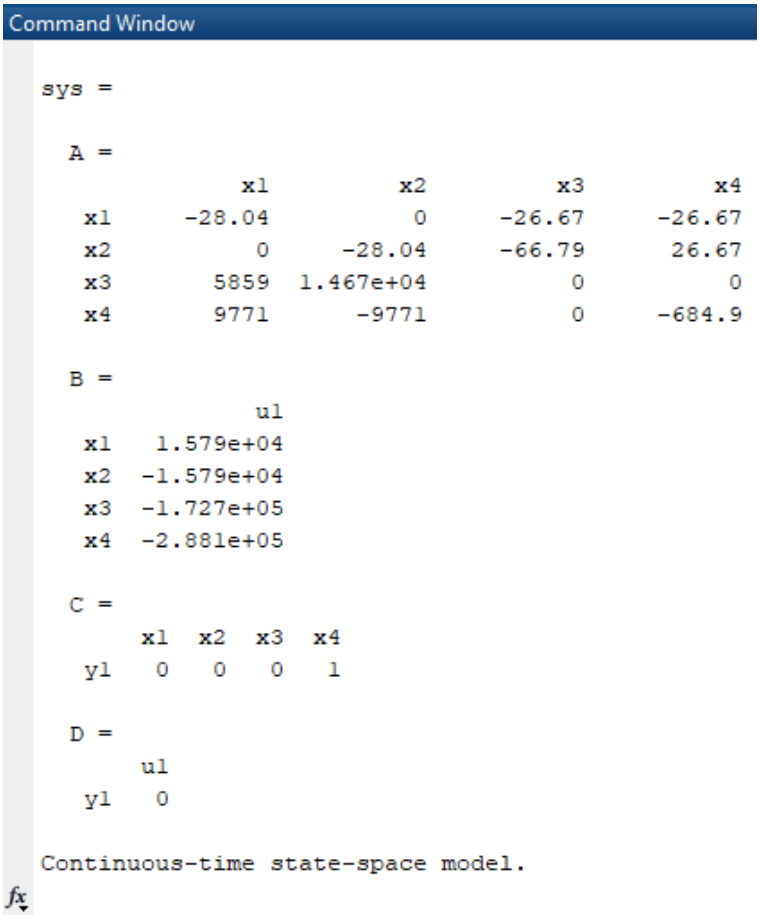


Figure 3.3: State-Space Model of SEPIC

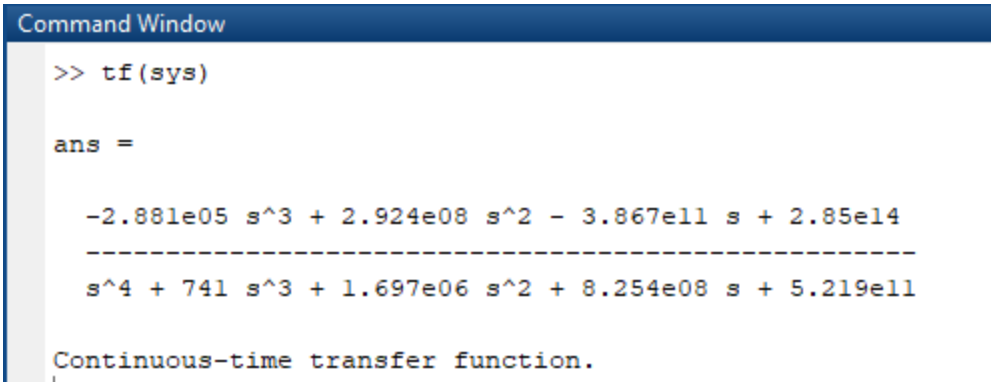


Figure 3.4: Transfer Function of SEPIC

Chapter 4

Controller Design

The key goal of any control design for a system is to place the system poles in system equations to achieve stability and robustness. Since there are more than one solution to this control design and pole placements, there should and must be a relatively better solution than others. This leads to the concept and idea of Optimal Control Theory. There has been many methods and tools to solution of this optimal control theory such as Dynamic Programing, Linear Quadratic Gaussian control LQG and Linear Quadratic Regulation Control LQR. The proposed controller for this work is Linear Quadratic Regulation Controller LQR and Linear Quadratic Gaussian Control schemes, the brief overview and design process in discussed in upcoming sections of this chapter.

4.1 Linear Quadratic Controller (LQR):

Linear Quadratic Controllers falls under the category of modern control techniques that deals and governs multiple input multiple output (MIMO) systems, which is responsible for deciding an optimal control response by determining the state feedback gains for the close-loop systems. LQR uses state space techniques to develop an optimal controller for the system. In this work the LQR will be designed based on the state space linearized model developed for SEPIC converter in

chapter 3.

The optimal control techniques such as LQR's functionality is based on the minimization of coast function. The cost function as shown in 3.30 is constituted of state variables related to the system (inputs and outputs) which are subjected to the constraints and specifications defined by the designers, through a weighted matrices in cost function. Based on the state space equation 3.24 for the SEPIC converter system a cost function can be defined as follow:

$$J_{min} = \int_0^{\infty} (x^T Q x + u^T R u) * dt \qquad 4.1$$

Where

U: Denotes the control input.

Q: Represents the weighted positive definite matrix related to system states.

R: Represents the weighted positive semi definite matrix related to input.

The structure of both matrices Q and R is diagonal. The theory and logic is simple for assigning values to both these matrices. Assigning higher values to the entries in Q matrix means giving importance to the relative states which leads to the generation of more aggressive control plan for reducing the deviations of respective states. Contrary larger values of entries in R matrix emphasizes on the minimization of the control input, so that lesser control effort is needed to minimize the cost function. The selection of Q and R matrix is briefly described in next sections of this chapter according to the proposed control scheme for the SEPIC converters in parallel connection.

4.1.1 Working of LQR.

The cost function of LQR in 4.1 is time integral of addition of energies of both control and transients of the system. The aim is to minimize the cost function subjected careful and suitable selection of the Q and R matrices along with solving the Algebraic Recarti Equation (ARE) to determine an optimal gain $K_{LQR,}$ which ensures the stability of the system. State feedback for a LTI system can be obtained as follow:

$$\dot{X} = Ax + Bu \qquad 4.2$$

For LQR problem all states should be controllable, so we assume that all states are available, then there exists a gain K_{LQR}, then the optimal control input u is defined as:

$$u = -K_{LQR}(x - \tilde{x}) \qquad 4.3$$

Where

$\tilde{x}$: denotes the desired value of state vector, then on using 4.3 in 4.2 the closed loop system is determined as follow:

$$\dot{X} = (A - BK_{LQR})x + BK_{LQR}\tilde{x} \qquad 4.4$$

From 4.4 it can be seen that the gain K_{LQR} depends on the system's pole locations according the attain desired control performance.

For a linear system the gain K_{LQR} vector matrix is determined as follow:

$$K_{LQR} = R^{-1}B^{T}P$$

Where P matrix is the solution to the ARE as follow:

$$A^{T}P + PA - PBR^{-1}B^{T} + Q = 0$$

This a straightforward method to generate the K_{LQR} based on Q and R matrix. Moreover MATLAB offers a very simpler and quicker function lqr(A,B,C,Q,R) to calculate the gain matrix.

4.1.1.1 Selection of Q and R Matrices:

As discussed above the Q and R matrices are related to the weight assigned to system states and inputs. In this work since SEPIC is of 4th order DC DC converter system with one control input, hence the dimension of Q matrix is 4x4 and R matrix's dimension is 1x1. Since the system requirement is to give more concentration towards current ripples than voltage ripples, so the wights of first two diagonal entries is kept higher than the rest of diagonal entries as in the state space model built for SEPIC in chapter 3, in the state vector $\mathbf{x_1}$ and $\mathbf{x_2}$ represents the inductor current $\mathbf{i_{L1}}$ and $\mathbf{i_{L2}}$ respectively. As for the weight associated with R matrix, since the controller only regulates the duty cycle the weight is kept 1 as follow:

$$Q = \begin{bmatrix} 10 & 0 & 0 & 0 \\ 0 & 10 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$R = [1]$$

4.1.1.2 Controllability Check:

To design a control scheme for any system, it is crucial to have all the states controllable. Any system is considered controllable if the control input (u) can interrelate the states with each other in a specific time frame. To check if the system is controllable, there exists a method in which using the state space model matrices A and B a controllability matrix is constructed as shown in () and then if the rank of this controllability matrix is full then the system is controllable. The figure 4.1 shows the controllability check done for the state space model determined in chapter 3 for the system considered in this work.

$$C_{controlabilityMatrix} = [A\ AB\ A^2B\ \dots A^{n1}B]$$

```
Command Window
A=A1
B=B1
C=[0 0 0 1];
D=0;
ControllabilityMatrix = ctrb(A,B);
ControlabilityCheck = rank(ControllabilityMatrix)

A =

       -927.83              0       -116.33       -116.33
             0       -354.55      -1109.77        405.38
       1408.17        3854.99             0             0
       1408.17      -1408.17             0       -119.62

B =

      47740.69
    -166369.06
     -35766.47
     -35766.47

ControlabilityCheck =

          4.00
```

Figure 4.1: Controllability check.

In above figure 4.1 it can be seen that the system is controllable since the controllability matrix is of full rank.

4.2 Implementation of LQR to the Single Stage SEPIC:

Using the linearized state space model developed for SEPIC converter in chapter 3, the LQR gain matrix K_{Lqr} is calculated within the MATLAB environment using function "lqr". Figure 4.2 shows the steps involved in calculation of LQR gain matrix. The open loop and close loop step response analysis of SEPIC is performed in this section.

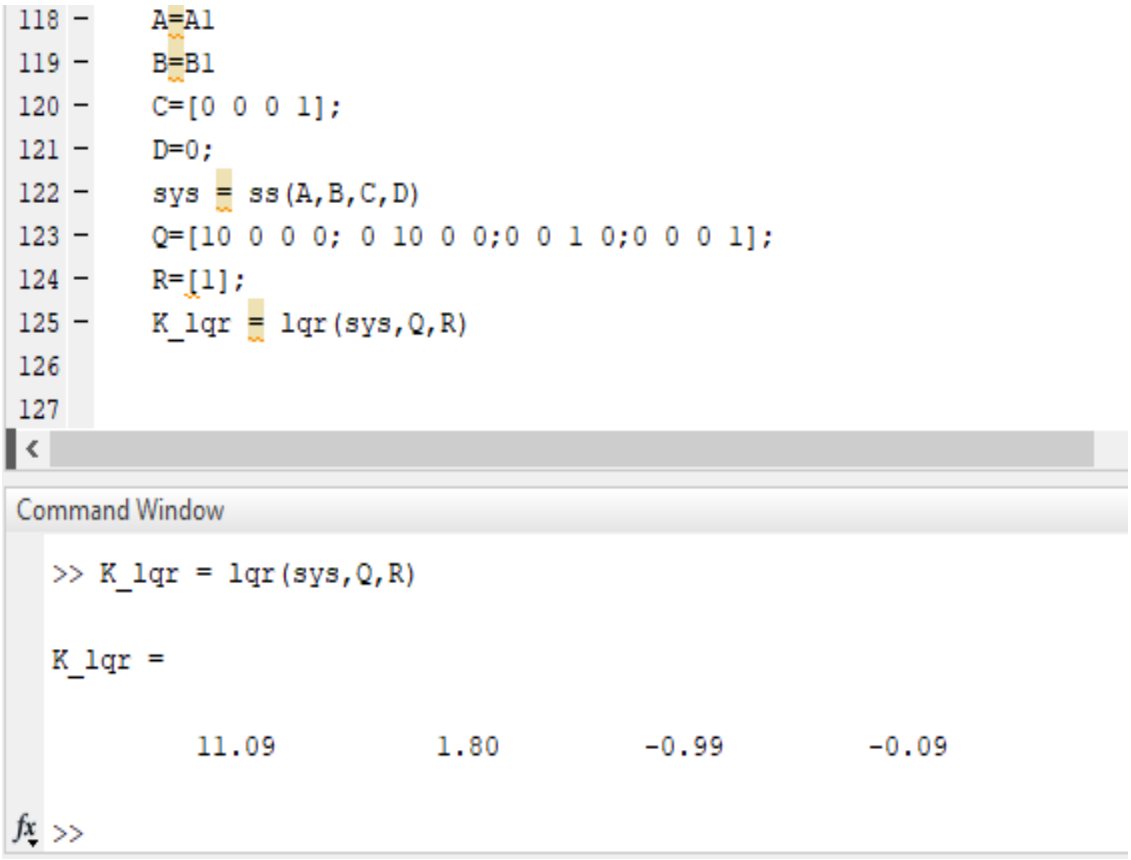


Figure 4.2: Calculation of LQR gain K_{Lqr}.

4.2.1 Open Loop Analysis:

The open loop setup for the SEPIC converter is built in Simulink, to perform the step response analysis. Figure 4.3 shows the open loop model setup in Simulink environment and figure 4.4 shows the step response of the open loop system of SEPIC, it can be seen that the system is highly unstable with huge steady state error.

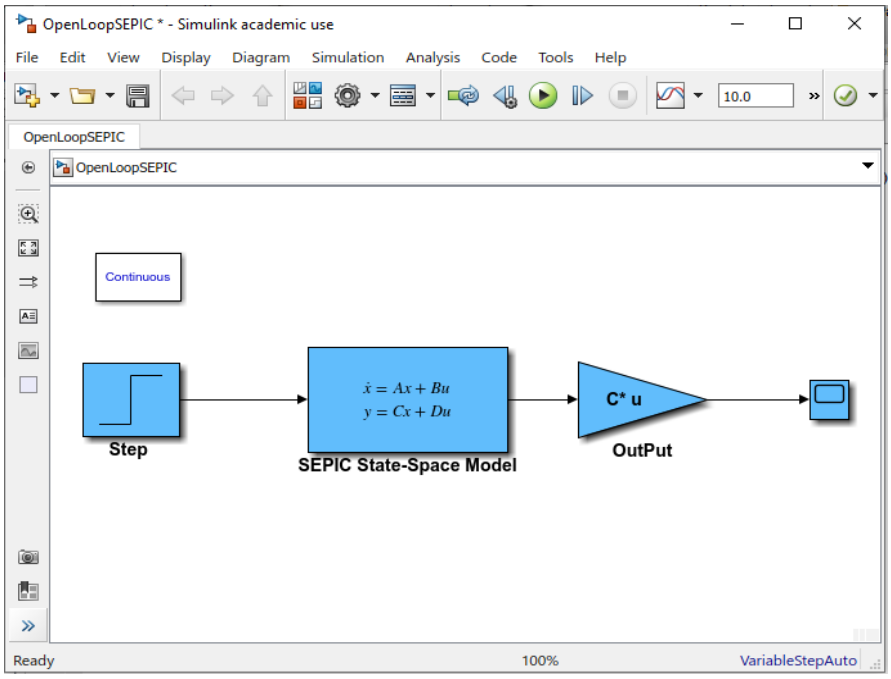


Figure 4.3: Open Loop Model of SEPIC.

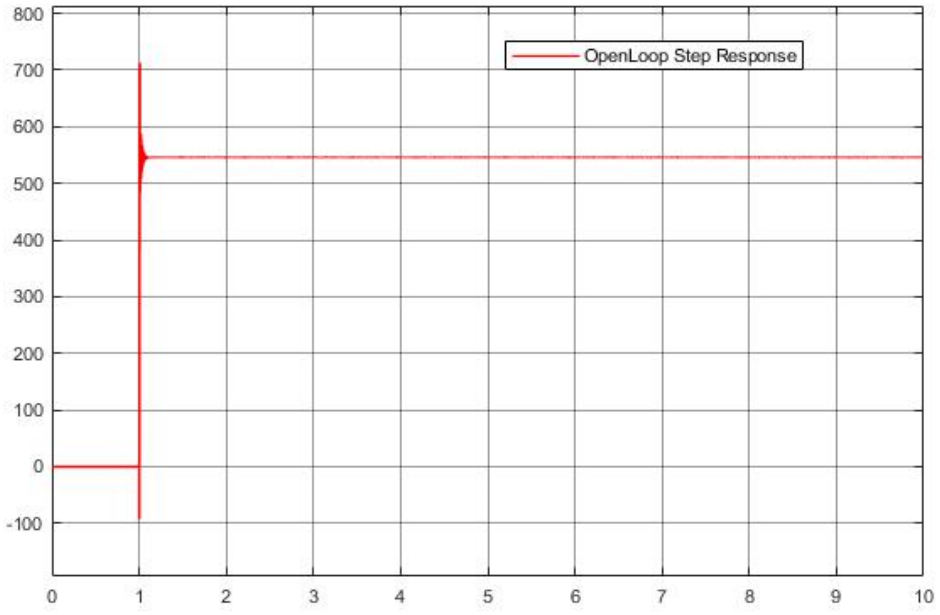


Figure 4.4: Step Response of Open Loop System of SEPIC.

The open loop system's step response exhibits an overshoot of 3.7 percent while the settling time is 8 ms, which is highly undesirable for the power system under consideration. More elaborated and detailed step response and frequency domain behavior is depicted in figure 4.4a and 4.4b respectively. The figure 4.4a shows step response having a steady state error of 191 and figure 4.4b exhibits frequency domain behavior with a negative gain margin of -32.1 and negative phase margin of -76.8. The figure 4.4b depicts that the system loop is unstable loop. The goal is to make the loop stable and both gain and phase margins positive.

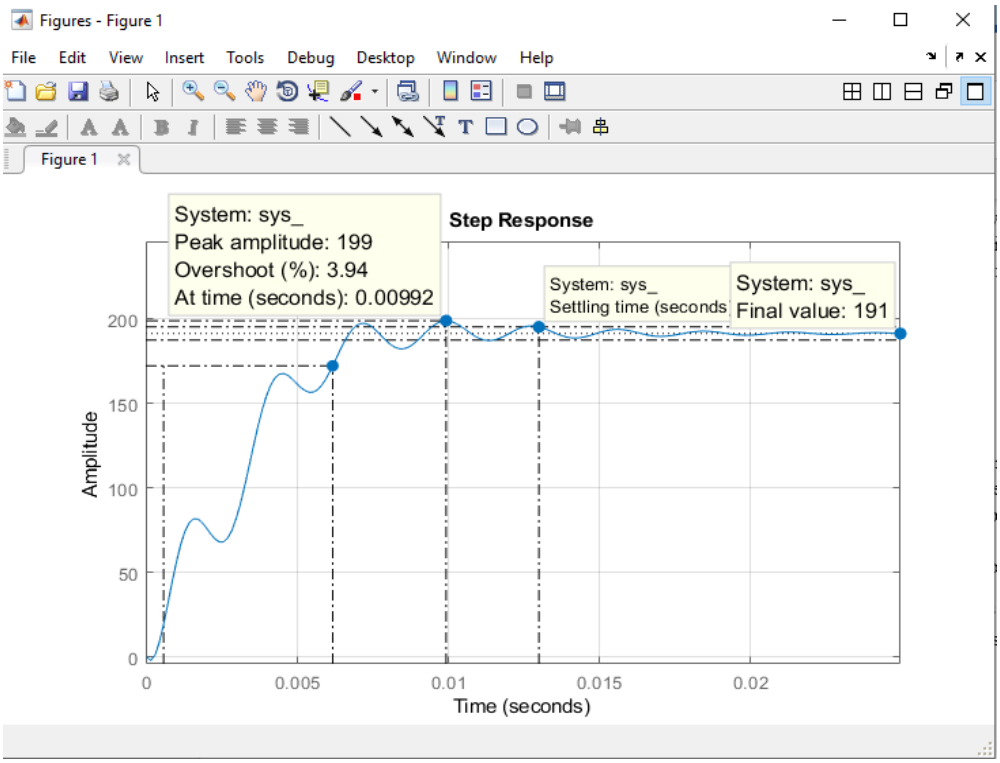


Figure 4.4a: Detailed Step Response of Open Loop SEPIC.

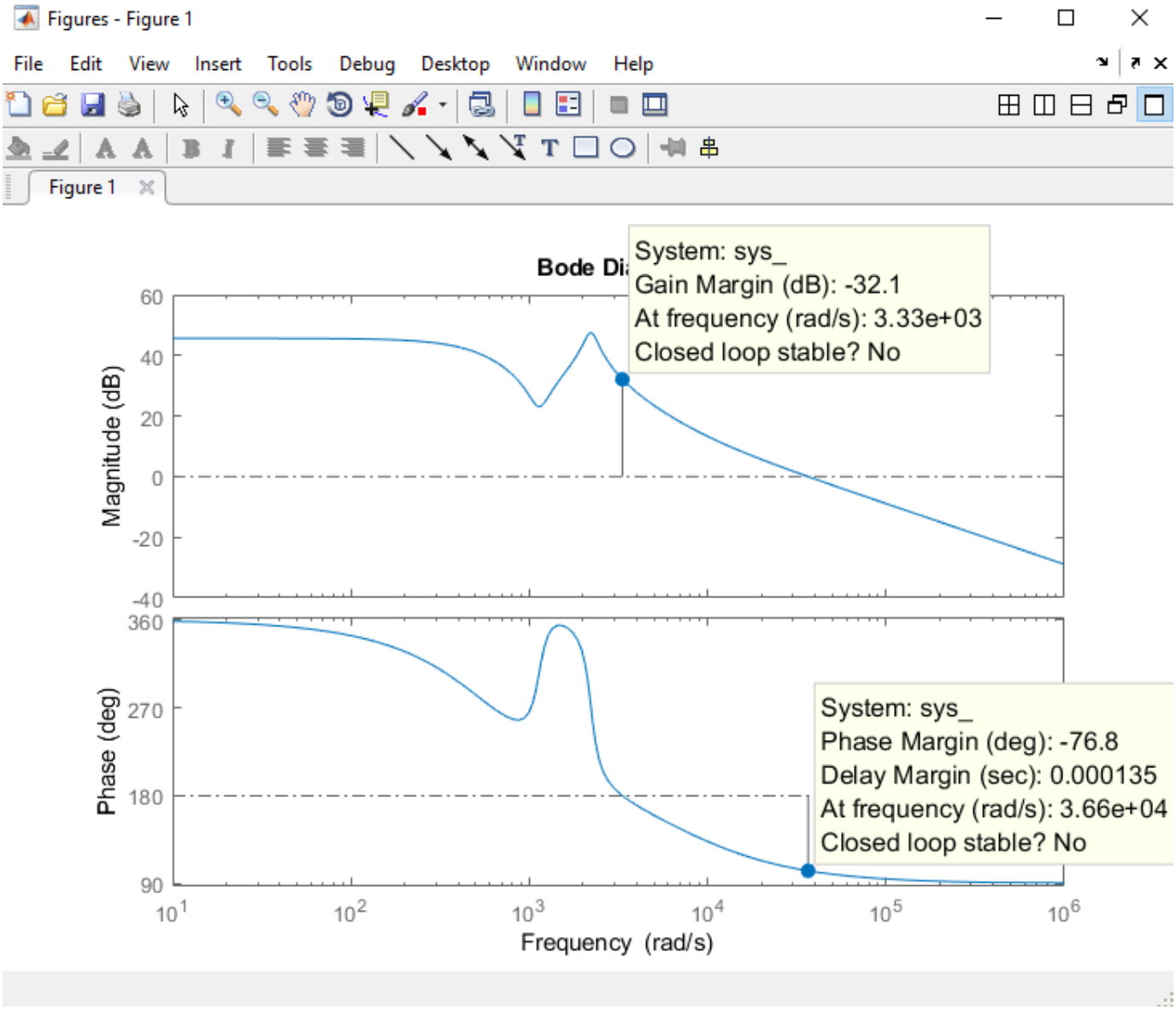


Figure 4.4b: Bode plot of Open Loop SEPIC.

4.2.2 Close Loop Analysis:

The close loop setup for the SEPIC converter is built in Simulink, to perform the step response analysis. Figure 4.5 shows the close loop model setup in Simulink environment, close loop model is realized by incorporating the LQR gain K_{lqr} in feedback loop of the state space model of SEPIC. Figure 4.6 shows the step response of the close loop system of SEPIC, it can be seen that the system response to the step input has significantly improved than the open loop step response.

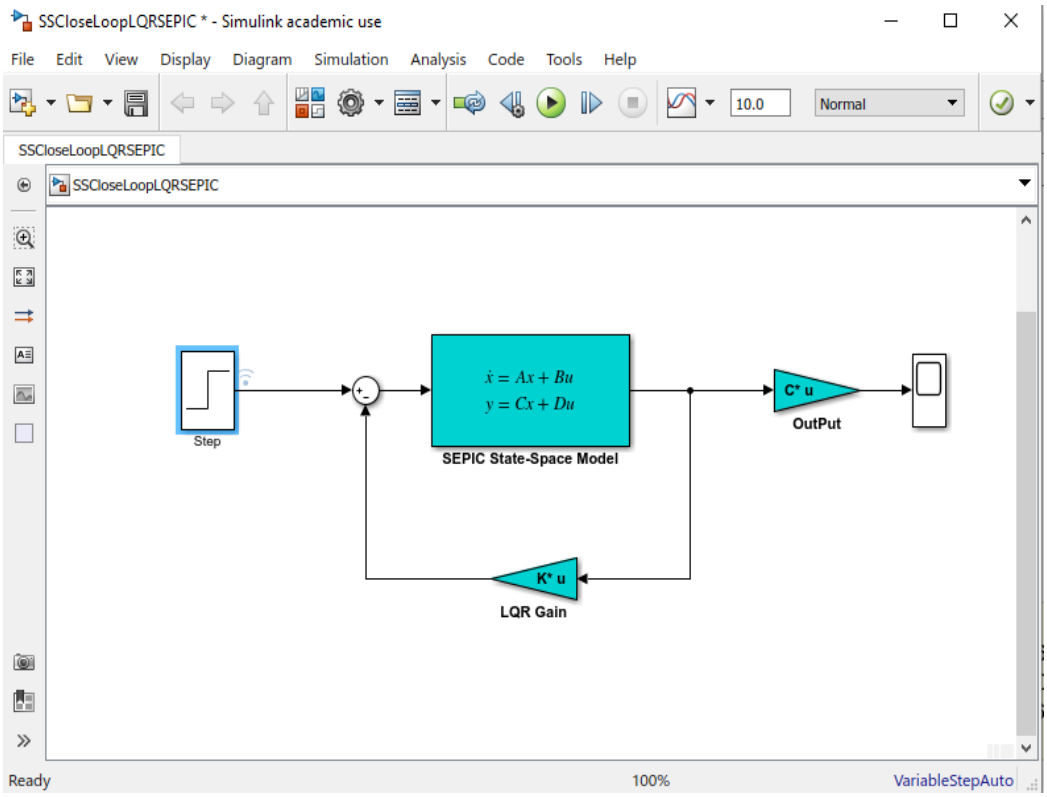


Figure 4.5: Close Loop Model of SEPIC.

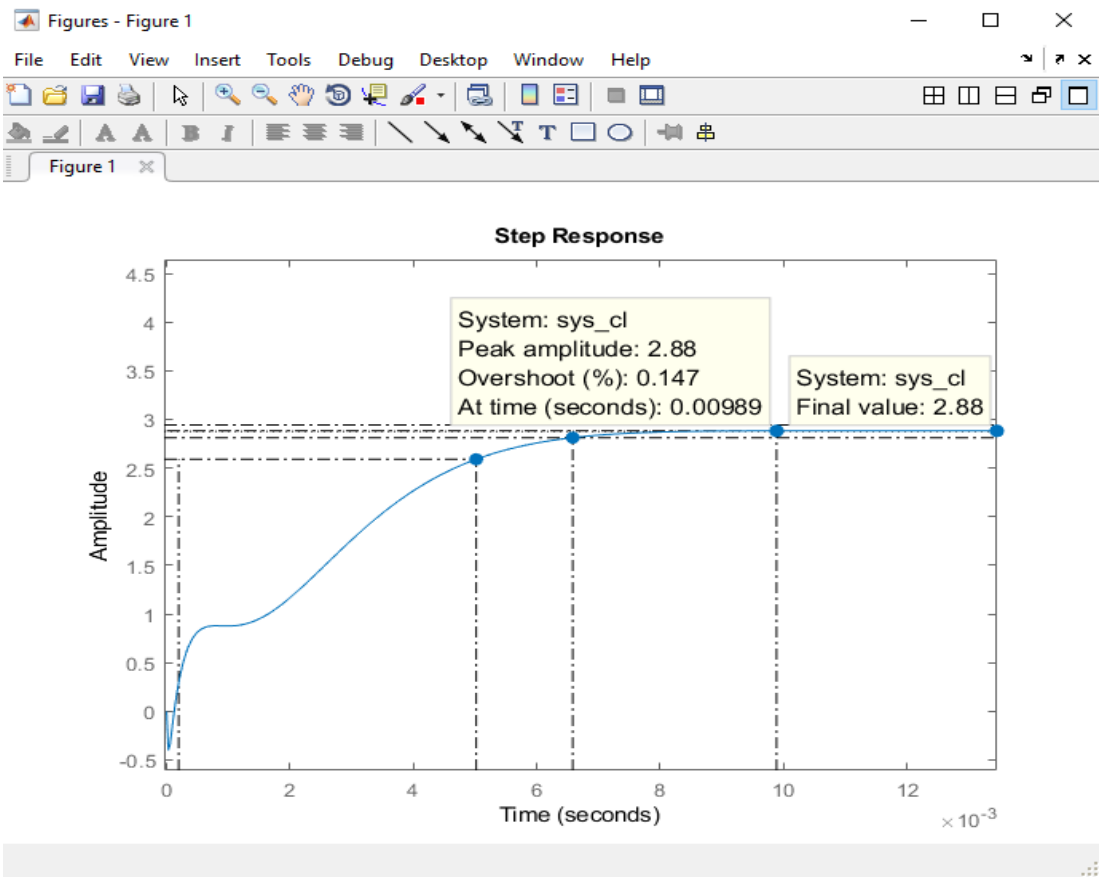


Figure 4.6: Detailed Step Response of Close Loop SEPIC.

Although the step response is improved to greater extent, the overshoot is dropped to 0.147% and the steady state error dropped to 2.8, however this steady state error $\mathbf{e_{ss}}$ is undesirable for the smooth operation SEPIC converter, to annihilate this $\mathbf{e_{ss}}$ an integral action is augmented into the closed loop state space model of SEPIC. The Integral action augmented into the close loop system is discussed in detail in next subsection. Also, the frequency domain analysis depicted in figure 4.7 indicates that the system is stable with gain margin of 4.65db at frequency 2.66e^4 rad/sec and with phase margin of 89.5 degree at 745 rad/sec frequency as shown in figure 4.7.

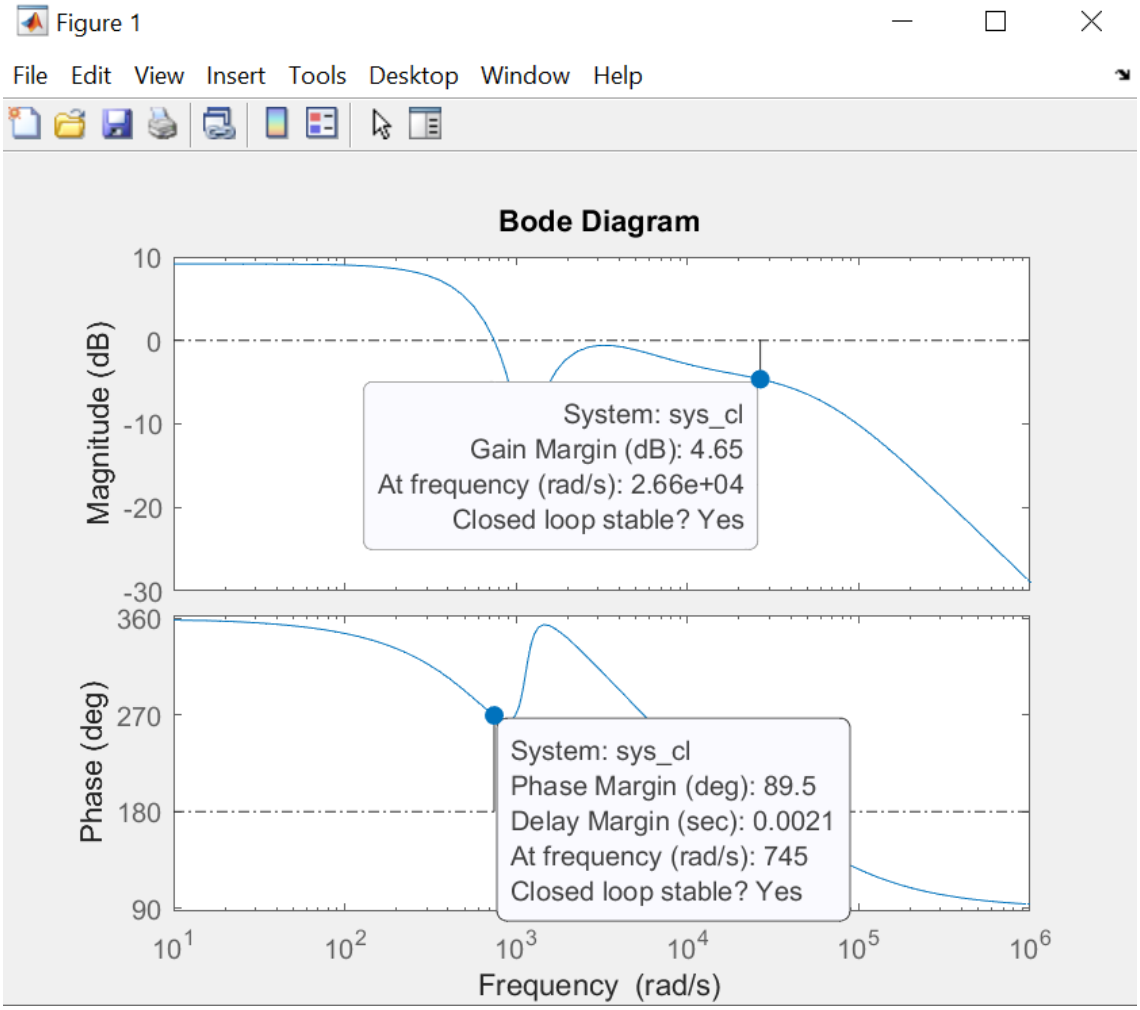


Figure 4.7: Frequency/Bode Plot of Close Loop SEPIC.

4.2.2.1 Integral Action:

Integral action is also known as Linear Quadratic Integral Controller LQI. Both LQR and LQI control schemes are state feedback controllers depending upon the augmented states of the system (System states and Integral of the error). This type of control scheme stabilizes the augmented system along with minimizing the cost function under the step input and step disturbances in the system. Control schemes depending on state feedback ensures the desired steady states under step input requires a careful computation in presence of reference input **r**. Hence it requires an exact and perfect model of the system in order to insure all the states of the systems and input signal satisfies the system dynamics. So an alternative to this computation and calibration is the designing and implementing the integral feedback. The main designing steps of the LQI is to augment a state with in the LQR controller that calibrates an integral of error, which is then feedback signal. To achieve this we augment a new state $\boldsymbol{e}$ in the state space equation of SEPIC converter in equation 3.24 as follow:

An integral of error can be represented as:

$$\boldsymbol{e(t)} = \int_{\mathbf{0}}^{\boldsymbol{t}} \boldsymbol{(r - y)dt} \qquad (4.1)$$

Or

$$\boldsymbol{\dot{e}(t)} = \boldsymbol{\dot{r} - Cx(t)} \qquad (4.2)$$

From equation 3.24 and 4.2 the augmented state space model of SEPIC can be written as:

$$\begin{bmatrix} \dot{x} \\ \dot{e} \end{bmatrix} = \begin{bmatrix} A & 0 \\ -C & 0 \end{bmatrix} \begin{bmatrix} X(t) \\ e(t) \end{bmatrix} + \begin{bmatrix} B \\ 0 \end{bmatrix} U(t) \qquad (4.3)$$

It can be seen that the new augmented state **e** is the integral error/mismatch between the actual output $\boldsymbol{y}$ and reference input $\boldsymbol{r}$. A careful designing of a compensator which ensures the stability of system, would certainly yield $\boldsymbol{\dot{e}(t) = 0}$ in it's steady state (ss) and as a result $\boldsymbol{y = r}$ in steady state as well. For this augmented system the control law is derived in usual fashion as follow:

$$u = -K_{LQR}(x - \tilde{x}) - K_i \mathrm{e}$$

Where,

K_{LQR}: previously designed state feedback gain of LQR controller.

x : Steady state values of the system's states.

$\tilde{x}$: Temporal/Instantaneous values of the system's states

K_i: Integral gain.

For a step input the resulting steady state (ss) point for the system is given as

$$x_{ss} = (A - BK_{LQR})^{-1}B\ (-K_i e_{ss})$$

The value of e_{ss} is not fixed, rather it will automatically be tuned to the value which sets $\dot{\boldsymbol{e}}(\boldsymbol{t}) = \dot{\boldsymbol{r}} - \boldsymbol{y} = \boldsymbol{0}$, which defines that at steady state the output of the system will be same as reference input that is zero steady state error. Also this implies that this action of control is independent of the state metrices (A,B and K) of system provided the system is stable (which is ensured in previous section by state feedback gain ($\boldsymbol{K_{LQR}}$).

Calculation of Integral K_i:

The procedure to calculate Integral gain is as same as calculation of LQR gain K_i, discussed in detail in section 4.1.1 of this chapter. However, since with the augmentation of new state/integral of error (e), the number of states of all over system has increased to 5 so, the state weighting matrix Q will be of 5th order as well subsequently the last element of the new matrix (Qi) will represent the weight of new state e.

The code below in figure 4.8 shows the steps performed in Matlab to calculate the gain K_i, using Matlab's built-in function (lqi).

```
Command Window
  Ki_=lqi(sys_,Qi,Ri)
  Ki_=Ki_';
  K_LQR=[Ki_(1,1) Ki_(2,1) Ki_(3,1) Ki_(4,1) ]
  K_LQI=Ki_(5,1)

  Ki_ =

            0.43         -0.25         -0.24


  K_LQR =

            0.43         -0.25         -0.24


  K_LQI =

          -70.71

fx >>
```

Figure 4.8: Calculation of gain Ki.

The Implementation of this control scheme is done in MatLab/Simulink environment and the step response of SEPIC state-space model after the integral action is added is shown in figure 4.9 and 4.10.

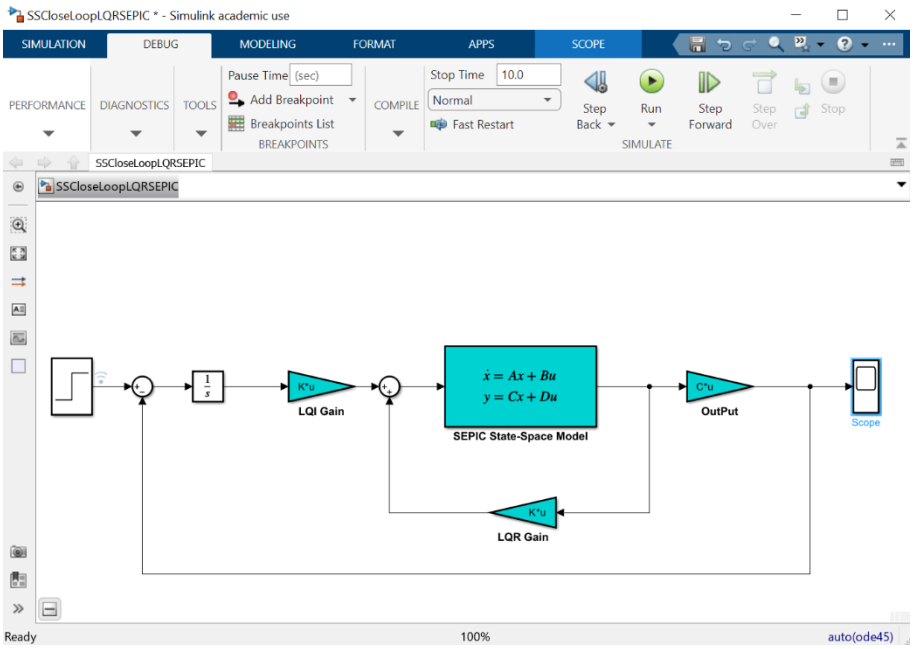


Figure 4.9: Augmented LQI in SEPIC State-Space Model.

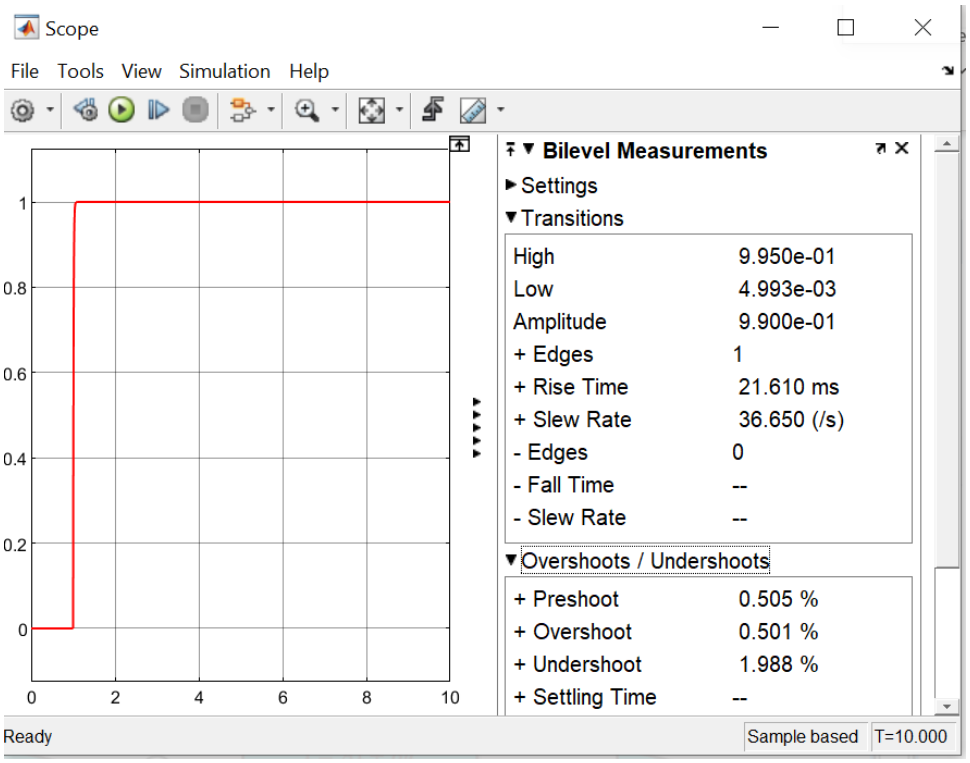


Figure 4.10: Step response of LQI augmented SEPIC model.

Figure 4.10 clearly shows that the controller now removes steady state error completely and the output completely tracks reference input.

4.3 Kalman Filter /Extended State Observer (ESO):

In many specific and practical scenarios to use a state of the system to generate a proper and optimal control input, might make the system complex, costly and vulnerable for example in a DC DC converter, measurement of an inductor current can be of importance to drive the converter switch properly, due to the cost of the sensors used, which are usually very expensive, and the precision of the measurement in essence, which is often affect susceptible to noise. Also, the measurement of input current itself might be distorted by system noises, which can lead to degradation of controller performance.

So, for this reason an Extended State Observer (ESO) also known as Kalman Filter (KF) is proposed. ESO is based Linear Quadratic State Estimator (LQE), provided a state-space model, specific type of measurements and the information regarding the environment surrounding the system [60].In early 1960s based on the work [62] of Nobert Wiener, Kalman Filter (KF) was basically built to give the estimation of the system states with attenuated measurements and

stochastic nature of inputs [61] but later on it was modified to work on state-space framework. The aim of KF is to give best possible estimation of dynamic system's state so, this also known as state estimator or an observer model. Its operation is subjected to the availability of the dynamic model of the system under consideration. The underlying assumption of Kalman Filter is that by means of sensors a dynamic system is measured along with a known control input provided to the dynamic system. With the knowledge of estimate of the dynamic system, known inputs, and measured outputs one can have an estimate of the state variables of the system and hence a feedback of estimated full state for controller can be generated. For this thesis/research the desired estimate is that of inductor currents ($\boldsymbol{i_{L1}}, \boldsymbol{i_{L2}}$) capacitor voltages ($\boldsymbol{V_{C\_out}}, \boldsymbol{V_{C1}}$) so that a controller may generate a suitable control signal that is duty cycle to maintain a desired voltage level at DC bus.

4.3.1 Kalman Filter Models:

The ESO/KF is based on several models, their aim is to determine the covariance and mean of the estimated system states. Kalman Filter uses four models as follow:

1) Dynamic Model of the system A_k
2) Model of Measurement C_k
3) Model of System/Process Noises W_k
4) Model of Measurement Noise V_k

It should be noted that the degree of exactness and workability between these four models defines what the Extended State Observer ESO output will show, the exact and true output of the SEPIC converter. These four models and their formulation according to the SEPIC converter model is described briefly in this section.

The ESO is typical of Kalman Filters, consists of two steps namely, measurement update and prediction update. As depicted in the figure 4.11

a) **Measurement update:** It is initiated whenever new sensor data is available. This step is basically responsible for error rectification based on the feedback mechanism using the current data given by sensors suing the equations as follow:

$$\left.\begin{aligned} K_{k\_Gain} &= P_k^- C_k^T [C_k P_k^- C_k^T + R_k]^{-1} \\ \hat{x}_{k+1}^+ &= \hat{x}_k^- + K_{k\_Gain}[y_k - C_k \hat{x}_k^-] \\ P_k^+ &= [1 - K_{k\_Gain} C_k] P_k^- \end{aligned}\right\} \quad \textbf{4.5}$$

b) **Prediction update:** It uses the dynamic model of the system and calculation of elapsed time to decide and predicts the states of the system. Prediction update, updates and moves forward the dynamics of the system using the following equation.

$$\left.\begin{aligned} \hat{x}_{k+1}^- &= A_k \hat{x}_k^+ \\ P_{k+1}^- &= A_k P_k^+ A_k^T + Q_k \end{aligned}\right\} \quad \textbf{4.6}$$

Where,

$\hat{x}_k^-$ **and** P_k^- **:** estimate of mean and covariance after prediction update step.

$\hat{x}_k^+$ **and** P_k^+**:** estimate of mean and covariance after measurement update step.

P_k**:** Covariance matrix of states of the system.

K_{k_Gain}**:** ESO/Kalman gain.

The terms K_{k_Gain} , Q_k and R_k are discussed in subsequent sections.

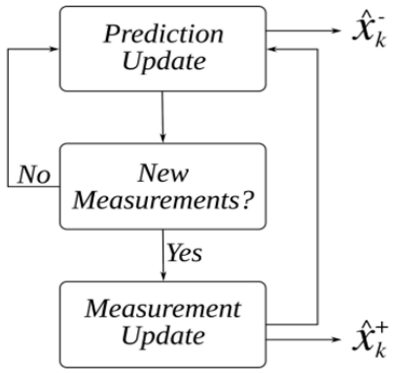


Figure 4.11: ESO/KF Algorithm.

Since the ESO used in this study for SEPIC converter is designed and implemented on a digital computer and is unavoidably in discrete time domain rather than in continuous time domain. Moreover the underlying assumption in formulation of simple Kalman Filter/ESO is that the system and measurement models involved are linear. The linearized and discretize form of system equations or more precisely the dynamic state equation 3.24 is given as follow:

$$\left.\begin{aligned} \dot{x}_{k+1} &= A_k x_k + B_k u + w_k \\ y_k &= C_K x_k + v_k \end{aligned}\right\} \qquad 4.4$$

Here,

A_k: Discrete time state transition matrix defining the state in the absence of input/noise and models the system dynamics at time $k+1$ to time k.

w_k: Process/System noise.

C_k: Measurement matrix.

v_k: Sensor measurement noise.

4.3.1.1 Dynamic Model of the system A_k:

In the absence of measurements, in order to forward propagate the system states in time, a dynamic model of a system is crucial and necessary. A creation of exactly perfect model is unachievable and even a nearly perfect model would slow down the response by increasing the computational complexity. A simplified model with large number of assumptions typically gives best results as crucial aspects of the dynamics of the system is considered and retained in the model.

A continuous time and non-linear model of the SEPIC converter is represented in form of matrix 3.23 in chapter 3.

4.3.1.2 Model of Measurement C_k:

C_k is the measurement matrix which relates the measurement from sensor data to state vector. The theory behind this model is that the measured sensor data has to have the same units and limits as

the state variable, in our case this state variable is $\boldsymbol{V_{C\_out}}$. Since there is one sensor in this case the measurement model matrix is given as follow:

$$\boldsymbol{C_k} = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{R_{Load}\, C_{out}} \end{bmatrix} \qquad \textbf{4.5}$$

4.3.1.3 Model of Noises ($\boldsymbol{W_k}$, $\boldsymbol{V_k}$):

The model involved in ESO are unforced models, so all input in steady state dynamics are considered to be disturbances/noises. The noise models are responsible for estimation of noises coming from the terms $\mathbf{w_k}$ and $\mathbf{v_k}$ in equation 4.4. The ESO comprises of two different models, one for system noise $\mathbf{w_k}$ and second for measurement noise $\mathbf{v_k}$. The system noise model is responsible for estimation of all the disturbances occurring due to assumptions made while modeling the system noise, linearization and environment effects, the measurement noise model compensates for the errors and uncertainties in sensor measurements. One of the key assumptions in modeling ESO is that all the noise has Gaussian distribution and with zero mean. The noise models are basically noise covariance matrices for each respective states of the system and measurement instruments/sensors.

The noise model for system noise is given by $\mathrm{W_k} = E[\mathrm{w_k}\, w_k^T]$, where $\mathrm{Q_k}$ is covariance matrix of the process showing to what extant and degrees noise is expected in the system and measurement noise model is given by $\mathrm{V_k} = E[\mathrm{v_k}\, v_k^T]$, where $\mathrm{V_k}$ is the covariance matrix of the expected disturbances/noise in the measuring instruments/sensors.

4.3.1.4 ESO/Kalman Gain ($\boldsymbol{K_{k\_Gain}}$):

The ESO or Kalman gain matrix mentioned in measurement update step in equation 4.5 essentially decides should the estimate rely more on model of the system or on the measurements.

The gain matrix given in 4.5 that is:

$$K_{k_{\_Gain}} = P_k^- C_k^T [C_k P_k^- C_k^T + V_k]^{-1}$$

Where,

$$P_{k+1}^- = A_k P_k^+ A_k^T + W_k$$

From the above equations it can be noticed that all the four models of ESO are responsible for the calculation of this gain matrix. In measurement update this gain matrix is multiplied with the difference between measured output and the estimated output of the system.

4.4 ESO Design:

For a predetermined problem where the noise associated with system is not considered, the state estimator is often known as observers. Such observers van be designed by selecting system poles which are relatively faster (placed in more deep left half plane) than the actual poles of the system. On the other hand in the presence of system/process as well as measurement noise, estimators which tends to minimize the errors in the estimated states based on the formulation of an optimization problem, leads to the need of development of a Kalman Filter, which is when deployed together with LQR based on state feedback theory is formally knowns as Linear Quadratic Gaussian (LQG) controller.

So, the proposed ESO design is divided into two sections namely, Observer design and LQG controller design.

4.4.1 Observer Design.

To successfully track the actual/real system states, an observer must be given with the information regarding the mismatch between the real system states and the observer output/estimated states ($y - \hat{y}$). This information is then given as feedback to the observer though a gain matrix L. This said process is depicted in figure 4.12.

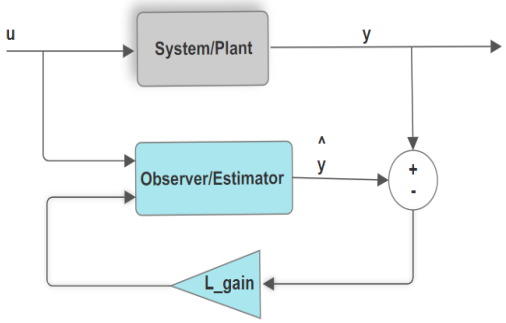


Figure 4.12: Observer/State Estimator.

From the figure 4.12 equations can be derived for observer as follow:

$$\hat{\dot{x}} = A\hat{x} + Bu + L(y - \hat{y}) \qquad \textbf{4.6}$$

$$\hat{y} = C\hat{x} \qquad \textbf{4.7}$$

Using 4.7 in 4.6 gives,

$$\hat{\dot{x}} = (A - LC)\hat{x} + [B \quad L]\begin{bmatrix} u \\ y \end{bmatrix} \qquad \textbf{4.8}$$

And defining an error vector $\tilde{\dot{\boldsymbol{e}}} = \boldsymbol{x} - \hat{\boldsymbol{x}}$ gives

$$\tilde{\dot{\boldsymbol{e}}} = (\boldsymbol{A} - \boldsymbol{LC})\tilde{\boldsymbol{e}} \qquad \textbf{4.9}$$

That being the case, the eigenvalues of 4.9 are determining factors of the error dynamics of the system and hence for a precise and robust estimation these dynamics should and must be faster than the dynamics of the original system/plant. For when eigen values are selected for (A-LC), the gain L can be calculated by a same process involved in computation of gain of LQR in section 4.1.1 of this chapter. The complete schematics of state observer with feedback is shown in below figure 4.13.

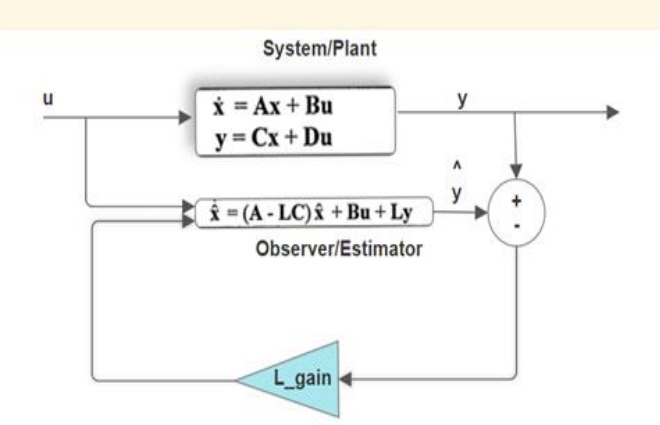


Figure 4.13: Observer with state feedback.

4.4.2 LQG Design.

The aim is to generate an optimal control input $u = -K_{ESO}x$, for the purpose of minimization of the cost function (quadratic function) along with maintaining the system's states to their respective initial states under the presence of system and measurement noises/disturbances. Such problem falls under the category of regulator problem that is, it is supposed to maintain the output of the system when there is no reference input. The disturbance induced system model is given in 4.4 and the quadratic cost function and it's associated weight matrices, Q and R, are as same as defined in LQR design in section 4.1, however only for the purpose of distinction the gain for LQG is represented with different notation that is K_{ESO}.

As for the system/measurement noises covariance matrices are concerned, since the variations/ripples in current is more critical than that of variations/ripples in voltages also based on the fact that in the calculation and designing of power converters more ripple in voltage is accepted than that of ripples in current, so the parametric/system noise matrix W_k is chosen for each states where noise variance per states ($x_{1,}x_2$) or inductor currents ($iL_{1,}iL_{2,}$) is kept 0.01A and 1V for noise variance per states ($x_{3,}x_{4,}$) or capacitor voltages($V_{c1,}V_{c\_out}$).

$$W_k = \begin{bmatrix} 0.01 \\ 0.01 \\ 1 \\ 1 \end{bmatrix}$$

While for the measurement noise V_k, a voltage sensor with low resolution is chosen, which measures the voltage output with a large error variance.

$$V_k = 0.1$$

The impact of the noise or variance over the states of the system was chosen R_{vv} is chosen as given below:

$$R_{vv} = 1 * 10^{-3} * \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

The parameter R_{vv} is chosen based on the measurement noise variance matrix, since if the measured noise V_k is equal to 0.1, the variance or noise importance parameter for the states must be equal to $(0.1)^2 \approx 0.001$, since it is a switched converter, the most relevant noise that most

affects its operation will be the switching noise with this parameter ensured, The filter gain can be any, since the noise gain is limited to that variance, therefore to increase the matrices and thus be able to estimate the noise model and filter shape, the band-bound noise parameters were used:
B_w =1, A_w=2*π*f; with f equal to the frequency of the converter, C_w=1 and D_w=0.
The noise model in MatLab script is shown figure 4.14 and the augmentation of this model into state-space model of SEPIC in MatLab environment is shown in figure 4.15, the process of augmentation is similar to the process involved in designing of LQI control. Using these parameters, the overall system matrices were constructed, and the gain for filter K_{ESO} is calculated using the LQR function of Matlab and is given below. The below figure 4.14 shows the augmentation of noise model to system model and the calculation of the extended state observer gain K_ESO.

```
130  format bank
131  %K_ESO Calculation
132  f_sw=50e3;%Switching frequency;
133  w0=2*pi*f_sw;
134  A_w= -w0;
135  B_w= 1;
136  C_w= 1;
137  D_w=0;
```

Figure 4.14: Noise Model

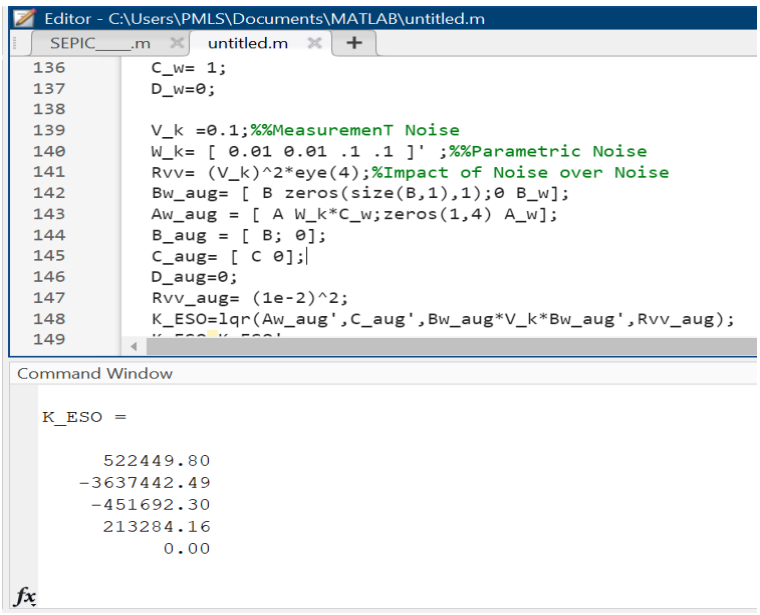


Figure 4.15: Calculation of ESO gain K_ESO

$$K_{ESO} = [522449.80 \quad -3637442.4 \quad -451692.3 \quad 213284.1]$$

Now using the calculated ESO gain, the close loop system for SEPIC is designed by pole placement method and matrices are extracted from this close loop system for the purpose of implementation of ESO for SEPIC in MatLab/Simulink environment. The stated is shown in figure 4.16.

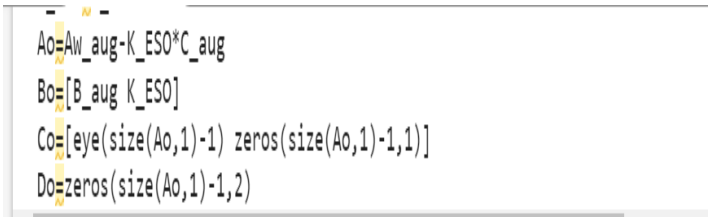


Figure 4.16: SEPIC-ESO close loop system.

4.5 Implementation of ESO to SEPIC

The implementation of ESO to state space model/block of SEPIC converter is performed in Simulink and the results are discussed in this section. The below figure 4.17 shows the implementation of ESO under a step response.

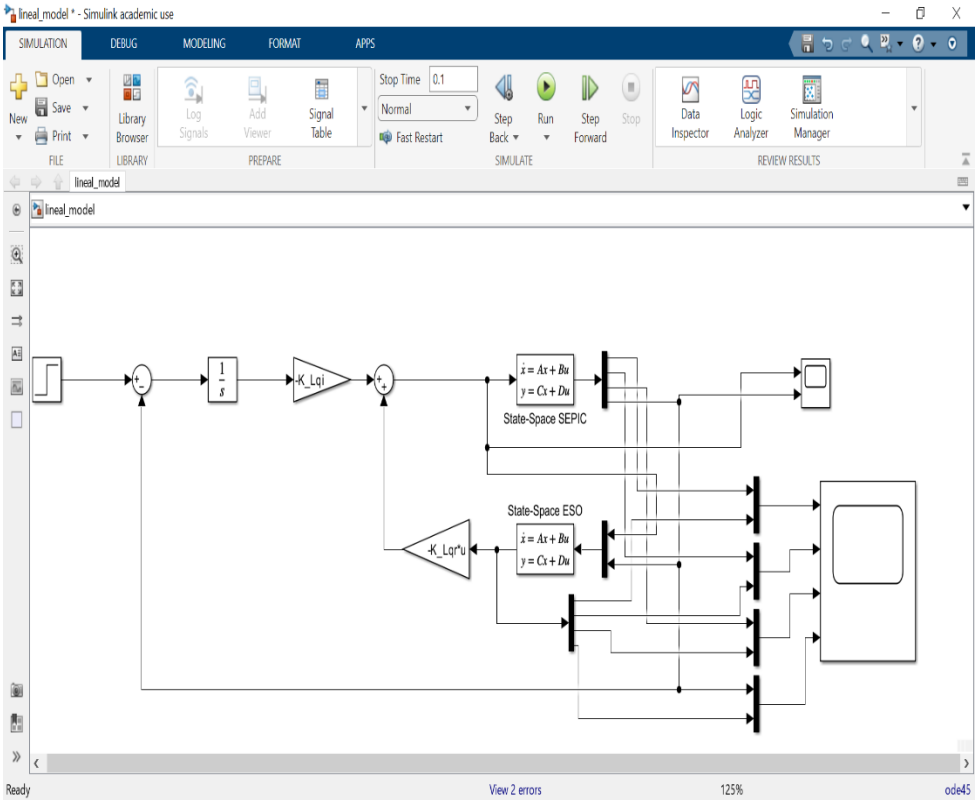


Figure 4.17: Implementation of ESO in state-space SEPIC model.

The upper limit for step input is kept 25 and lower limit is set to 20 as shown in figure 4.18, figure 4.18 shows the output of the system after the implementation of ESO.

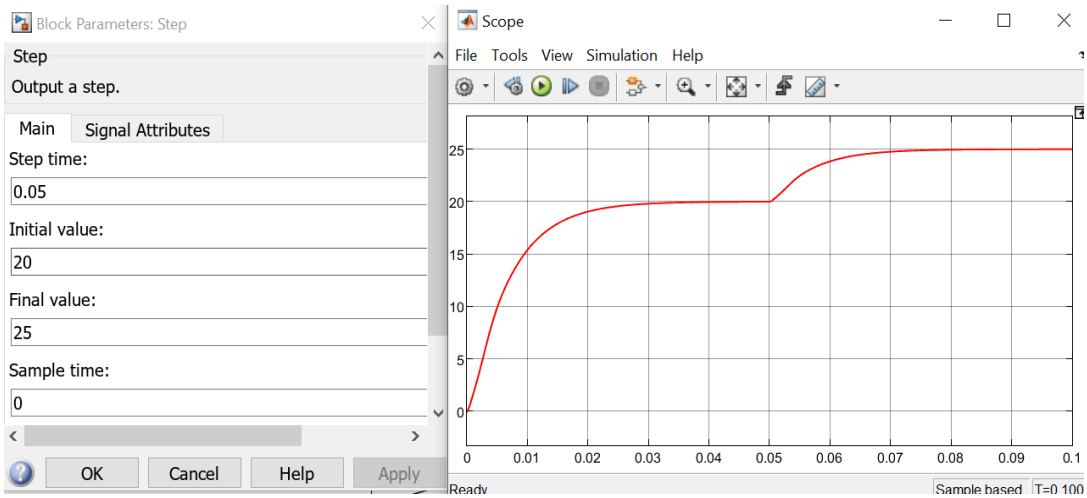


Figure 4.18: Step response of ESO-SEPIC

It can be noticed from above figure that the step response of ESO deployed SEPIC has no overshoots and steady state error.

The effectiveness of Extended State Observer designed can be verified from the below figure 4.19. It can be seen that, all the three states are completely inline with their predicted/estimated states.

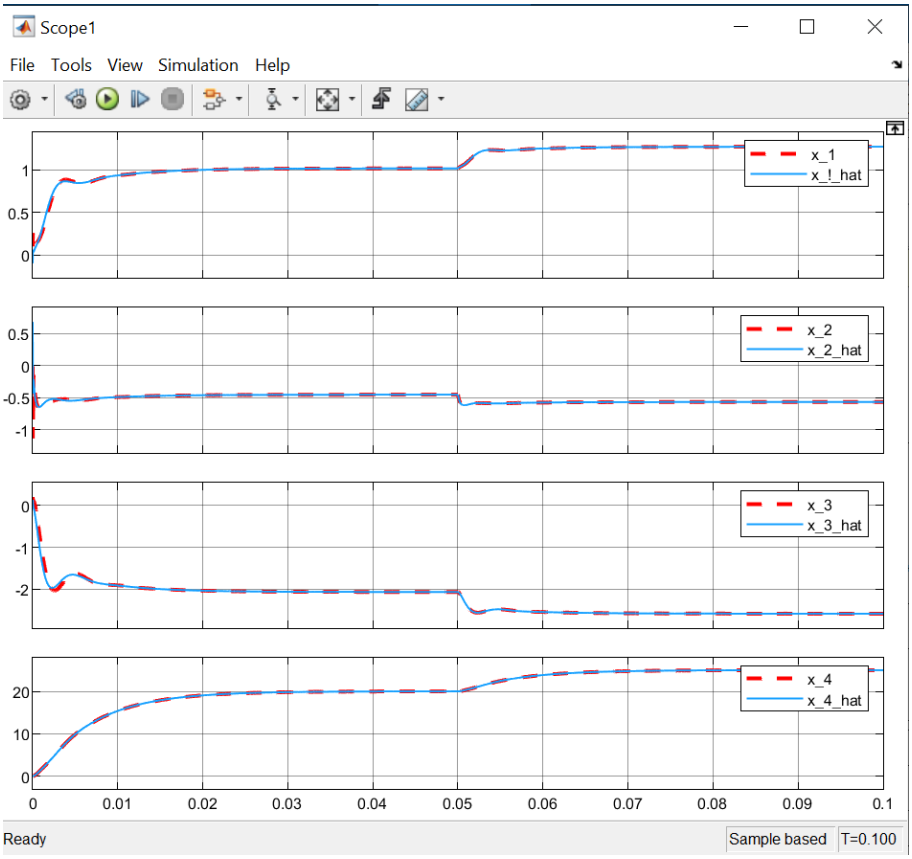


Figure 4.19: Response of each state of ESO-SEPIC to step input.

The red doted line in above figure shows the actual/instantaneous values of the states while the blue solid line represents the estimated values for the states, it clearly depicts the effectiveness of the ESO/Kalman filter for the SEPIC under measurement and parametric noises, all the states are recovered perfectly under the presence of noises/disturbances.

Chapter 5

Implementation of proposed control scheme in parallel operation of SEPIC, forming a DC micro-grid.

In this chapter, simulation results of the two SEPIC parallelly connected converters and operating as a micro-grid is presented. The scheme of control proposed in the preceding chapters is used to design and develop the simulation model. Firstly, the operation of the parallelly connected converters forming a DC micro-grid is simulated. Secondly, the micro-grid is simulated for different voltage references and loading condition is investigated and the transients and stability of the system is verified. For the simulation purposes the model of the SEPIC converter derived in previous chapters is implemented. Below figures represents the connection as well as control scheme implemented for simulation purposes in Matlab/Simulink environment.

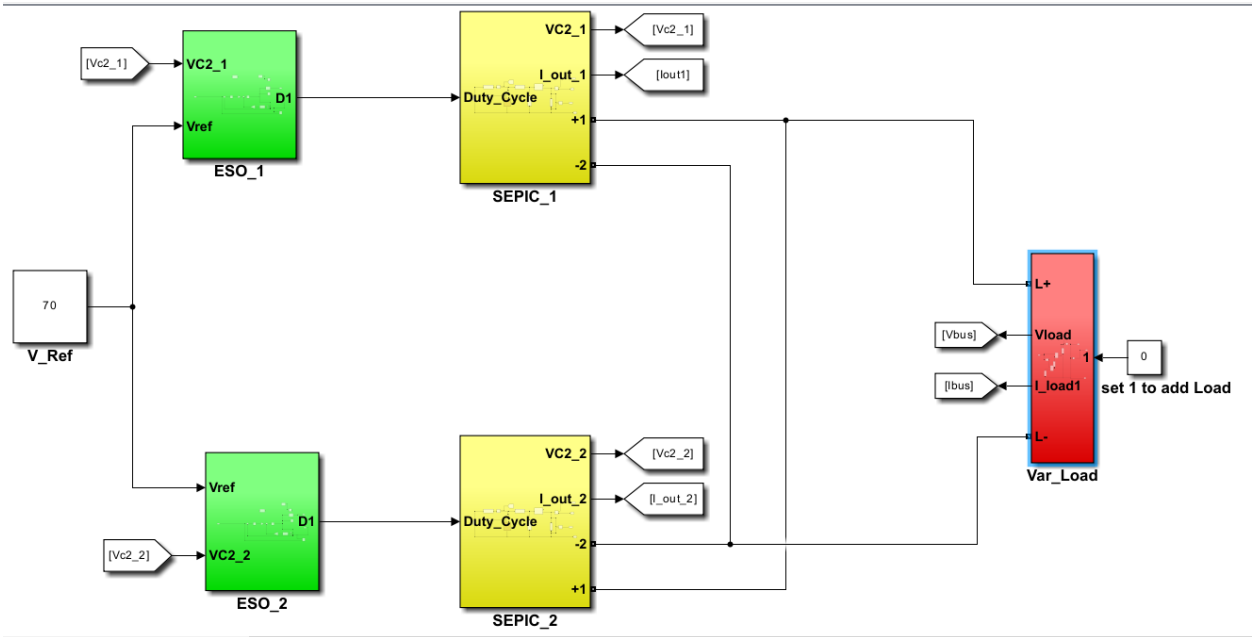


Figure 5.1: Parallel connected SEPIC converters acting as micro-grid.

In the above figure 5.1 two SEPIC converters are shown connected in parallel forming a DC microgrid, with each having control scheme for each converter with a common variable load connected on DC bus represented in red.

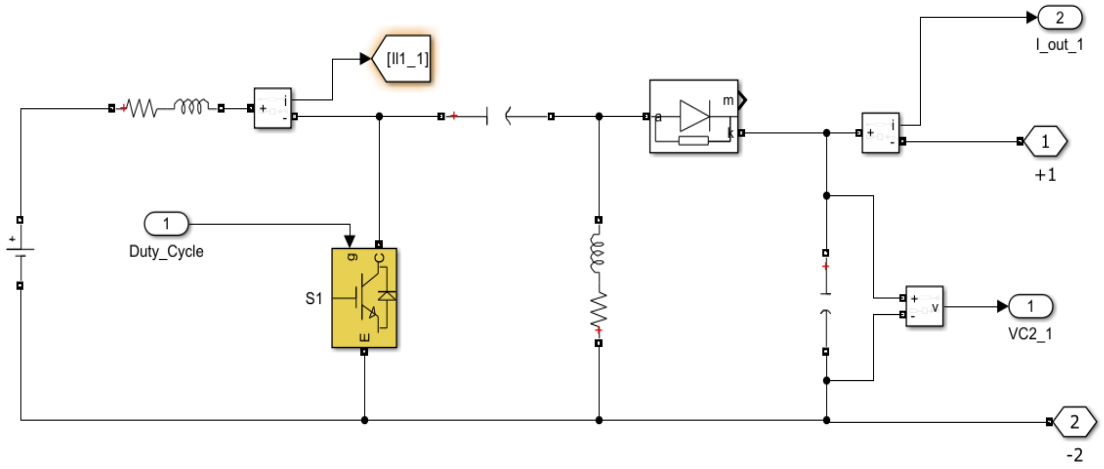


Figure 5.1(a): switch model of SEPIC.

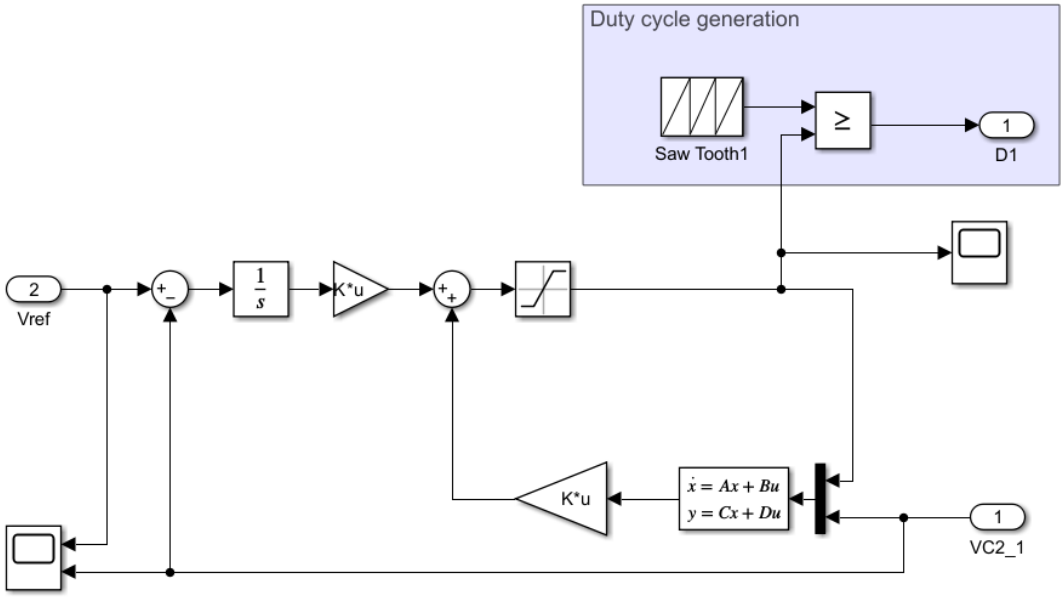


Figure 5.1(b): Extended State Observer-ESO model.

The above figures 5.1 (a) and (b) represents the average model of SEPIC and ESO model built for simulations respectively.

5.1 Simulation results.

The system is tested for two cases that are Buck and Boost modes both modes also tested for the increased load and verified the robustness and effectiveness of the proposed system for the independency of the system performance against the load profile on the DC bus.

A) Buck Mode

At first the simulation is performed for buck mode operation, keeping values of components and input voltages for both converters identical as shown in table 1. The subsequent results are shown and discussed below.

Table 2: Converter Specifications for Buck Mode.

Inductance L1, L2	2.3e-3H
L1 ESR rL1	2.34ohm
L2 ESR rl2	0.234ohm
Capacitance C1, C2	190e-6F
Vin	100V
V_ref	70V
Load	50ohm+50ohm

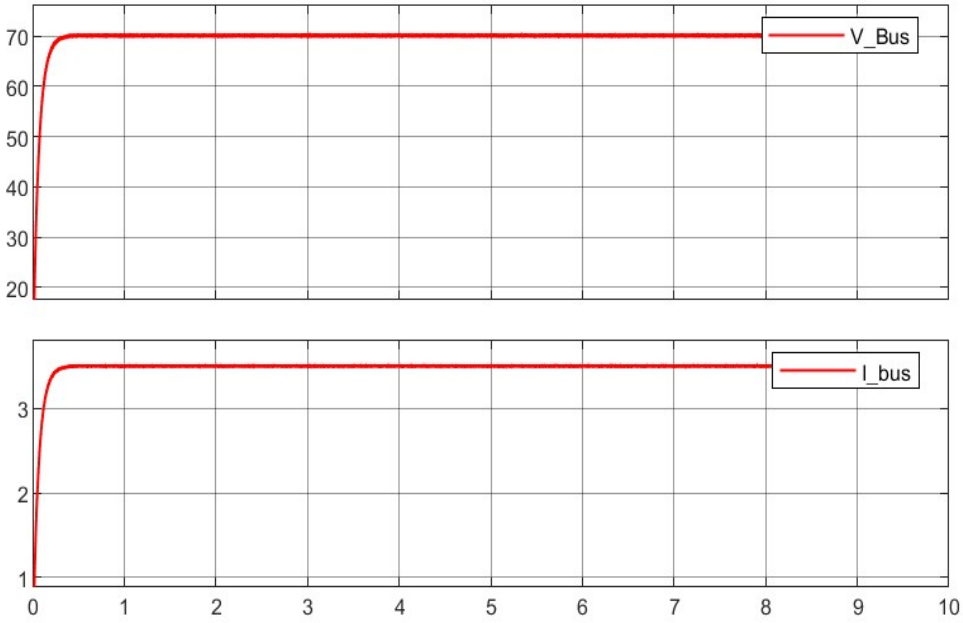


Figure 5.2: DC bus voltage and current of a microgrid under buck mode.

Figure 5.2(a): Voltage and current of first module of DC microgrid under buck mode.

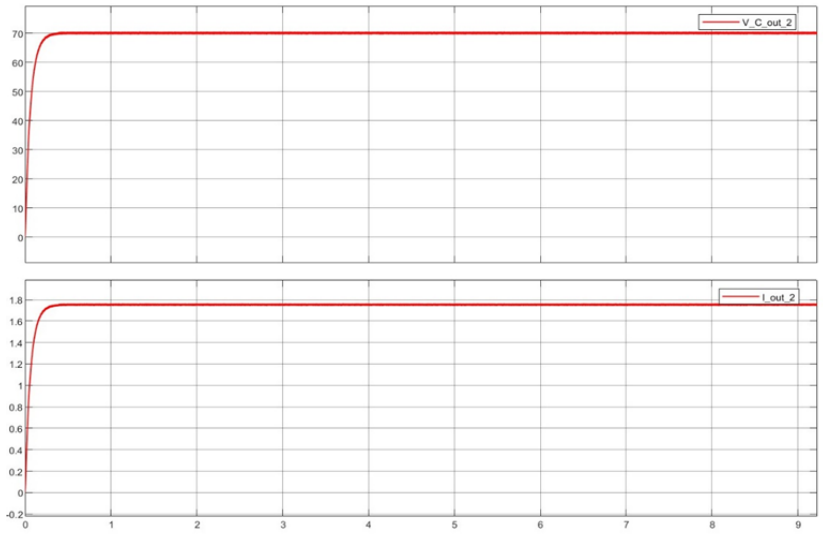


Figure 5.2(b): Voltage and current of second module of DC microgrid under buck mode.

From the above figure 5.2 it can be noted that the parallel connected SEPIC converter forming a DC micro-grid, perfectly achieves the desired voltage output and equal sharing of load current at DC bus side. Also form the figures 5.2(a and b) it can be seen that both converters are working perfectly for regulation of voltage at DC bus side as well as equal sharing of load current without any current control loop or current information sharing mechanism. Moreover the below figure 5.3 validates the system capability of the proposed system to tackle the increased load from 50 ohm to additional 50 ohm in parallel at T=6.314s time interval.

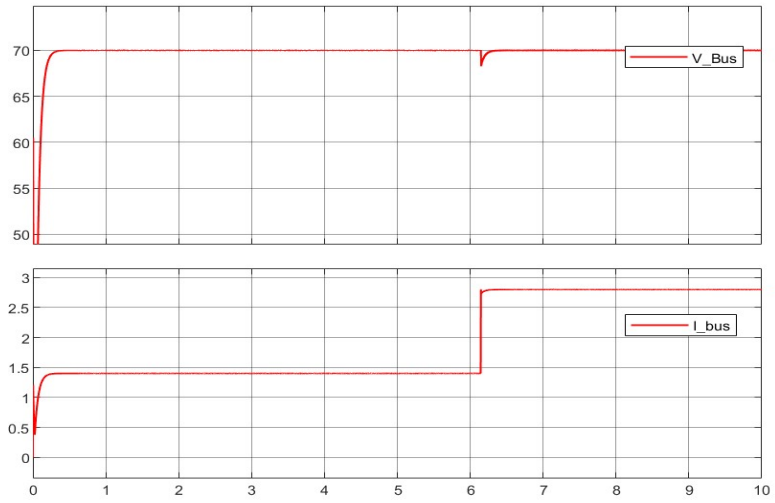


Figure 5.3: Voltage and Current of DCMG under buck mode for increased load.

B) Boost Mode

Simulation is performed for boost mode operation, keeping values of components and input voltages for both converters identical as shown in table 3. The subsequent results are shown and discussed below.

Table 3: Converter Specifications for Boost Mode

Inductance L1, L2	2.3e-3H
L1 ESR rL1	2.34ohm
L2 ESR rl2	0.234ohm
Capacitance C1, C2	190e-6F
Vin	100V
V_ref	120V-220V
Load	50ohm+50ohm

To test the effectiveness of the proposed control scheme different voltage references in the range of (120Volts to 220Volts) are given to the system to track the voltages at DC bus. Figures 5.4, 5.4a and 5.4b validates the system performance under different voltage set points and equal sharing of load current and voltage regulation of each convert respectively. Figure 5.5 shows the response of boost mode under varied load.

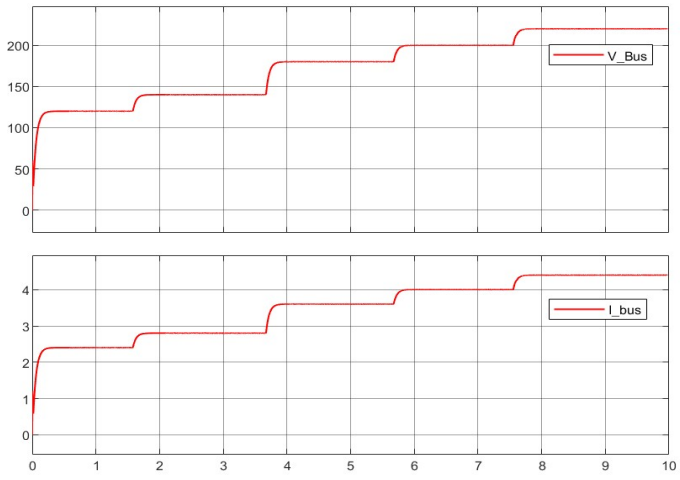


Figure 5.4: Desired boosted voltage levels and current of DCMG.

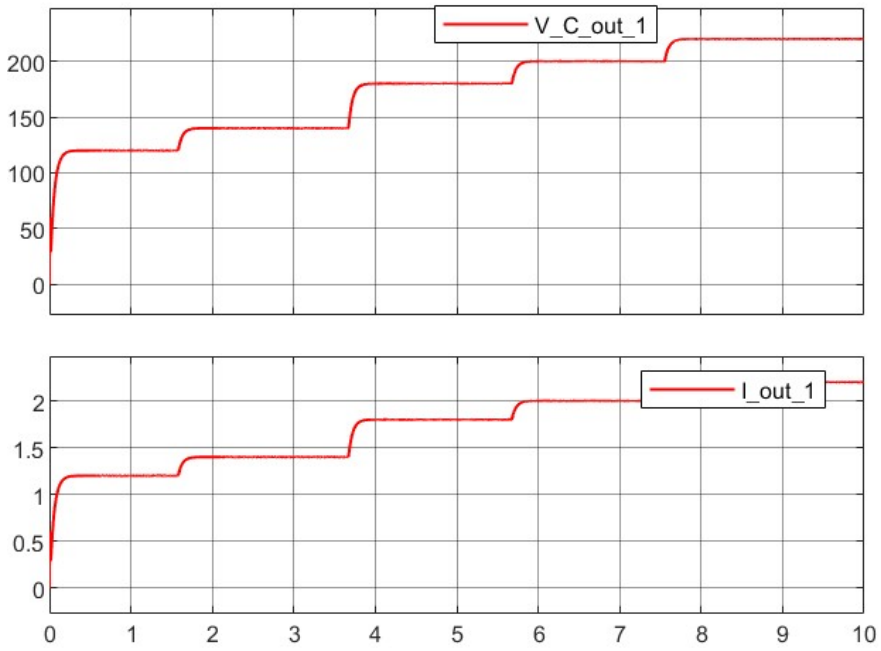


Figure 5.4a: Voltage and Current of 1st Module of DCMG under Boost Operation.

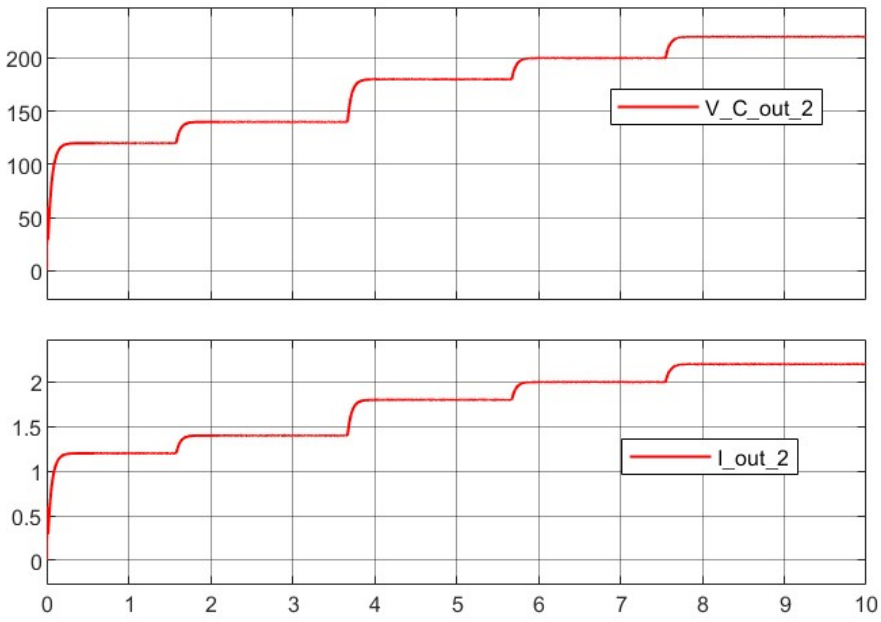


Figure 5.4b: Voltage and Current of 2nd Module of DCMG under Boost Operation.

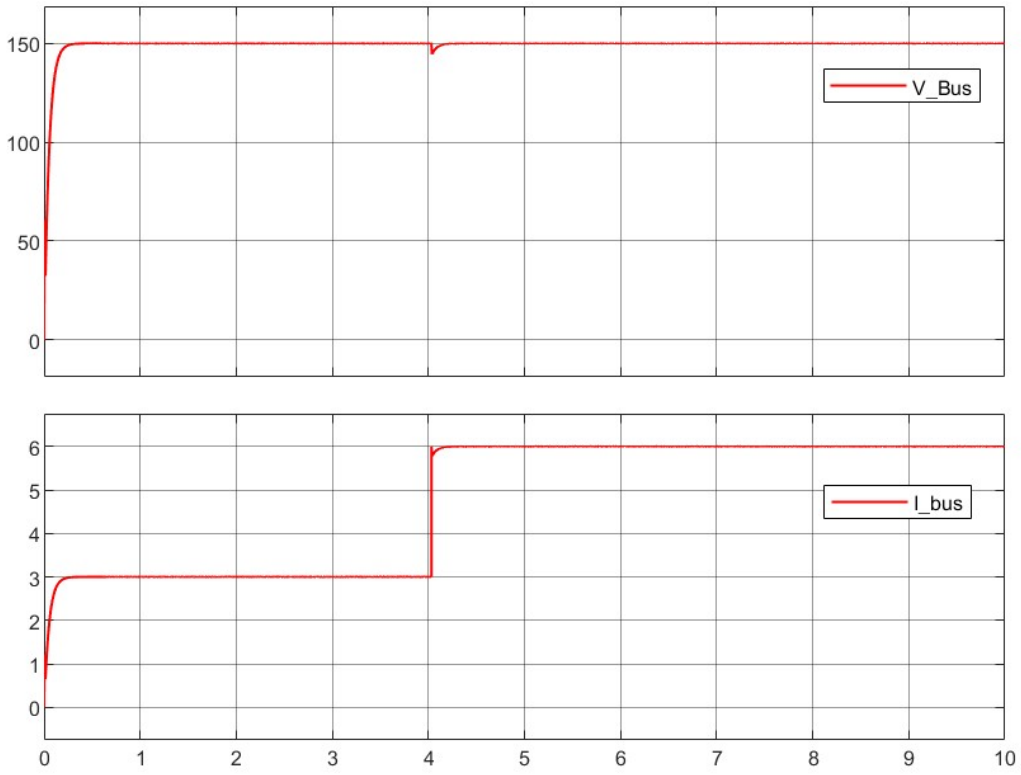


Figure 5.5: Voltage and Current DCMG under increased load in Boost Operation.

Given the simulation results from figures 5.4 to 5.5, one can easily verify the effectiveness of the proposed system.

5.2 Comparison of proposed scheme with conventional controller.

The controller used for the comparison is PID controller, The gains of the PID controller were selected using the Simulink transfer function based autotuning method and are shown figure 5.5, the overall conventional scheme is also shown in below figure 5.6 and it's results are discussed below:

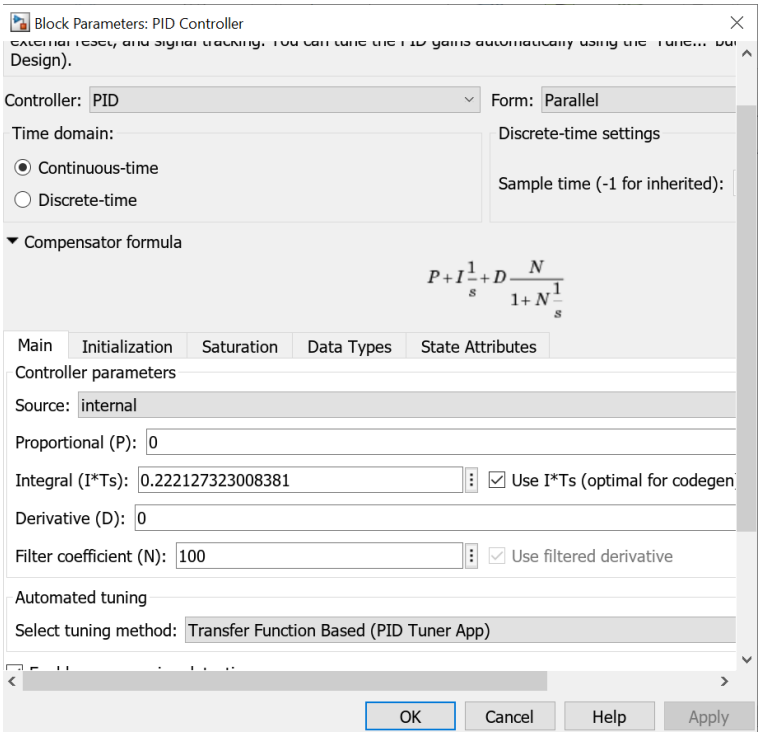


Figure 5.6: Tunned PID gains.

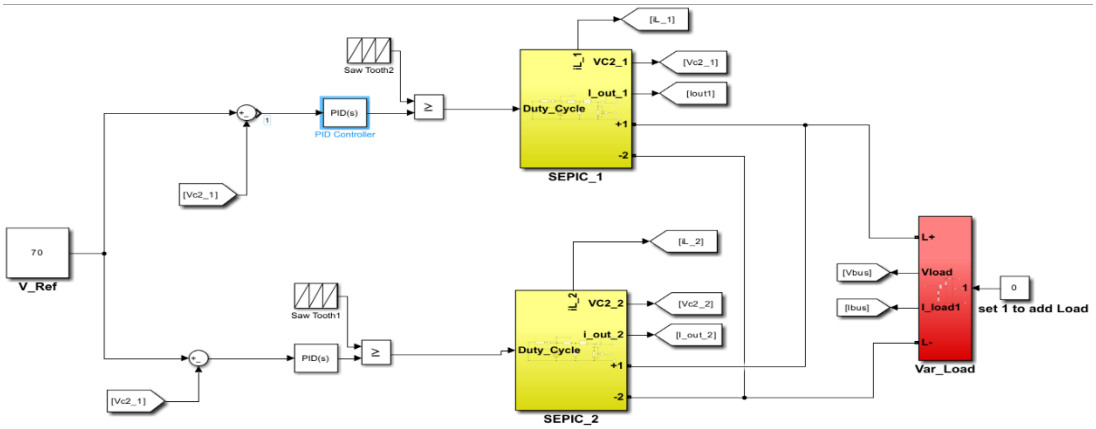


Figure 5.7: Conventional control scheme.

The reference/desired voltage to be realized at dc buss is 70 volts, the first batch of simulation are carried out keeping the input voltages identical for each module. The simulation results shown in figure 5.7 depicts that the proposed scheme is superior than conventional control scheme in terms of ripple factor control, reference tracking and regulation of voltage. One can easily observe the performance difference between the conventional and proposed control schemes from results shown below.

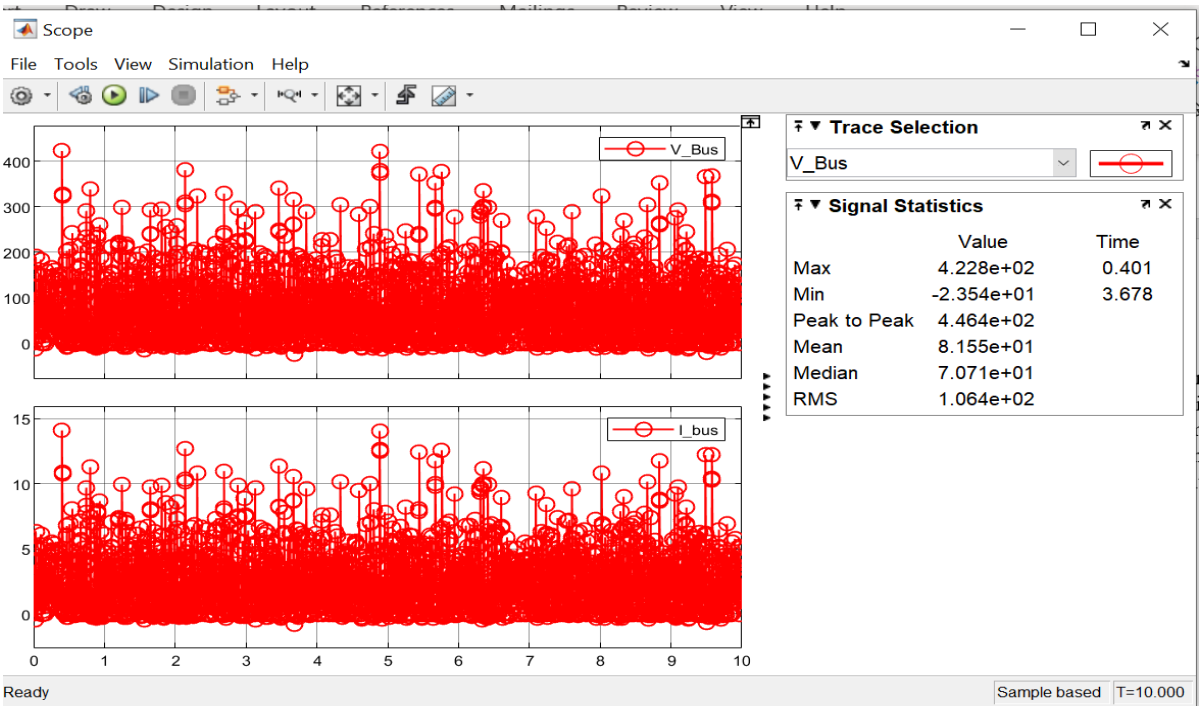


Figure 5.8: PID controlled DC microgrid, voltage and current at DC bus.

Since first batch of simulation for PID control scheme depicts the inferiority of this scheme so, simulating further for increased load in buck and boost operation demand would be of no benefit.

5.2 Hardware Implementation/Results.

5.2.1 Hardware Implementation.

The hardware implementation of this research focuses on a laboratory-based setup with two parallel-connected SEPIC (Single-Ended Primary-Inductor Converter) converters designed to operate with a nominal input voltage of 12V and a variable output voltage ranging from a maximum of 19V to a minimum of 9V. The setup is designed to supply a total load current of 1.2A, which is shared almost equally between the two SEPIC converters. One converter delivers approximately 0.55A, while the other delivers 0.56A, thereby ensuring balanced current sharing between the converters.

5.2.2 Power Supply and Load

The input to the SEPIC converters is sourced from a 12V DC power supply, which is a typical voltage in many DC microgrid applications. The output voltage of the converters is designed to be adjustable based on the load requirements, ranging between 9V and 19V. The total output power of the system is governed by the load conditions. At the nominal output of 12V and a total load current of 1.2A, the output power is approximately:

$P\text{out}=V\text{out}\times I\text{load}=12\text{Vx}1.2\text{A}=14.4\text{W}$

At the maximum output voltage of 19V and the same load current of 1.2A, the system delivers:

$P\text{out}=19\text{V}\times 1.2\text{A}=22.8\text{W}$

Similarly, at the minimum output voltage of 9V:

$P\text{out}=9\text{Vx}1.2\text{A}=10.8\text{W}$

4.2. SEPIC Converter Design.

The SEPIC converters were designed to regulate the output voltage while ensuring stable current sharing. Each SEPIC converter is capable of operating in Continuous Conduction Mode (CCM), providing smooth output with minimal ripple. The feedback control is critical in achieving precise voltage regulation and equal current sharing between the converters.

To down sample the output voltage for interfacing with the controller, a resistive voltage divider is used. This consists of a 10kΩ variable resistor and a 270Ω fixed resistor, which

scales the maximum output voltage of 19V down to a measurable range suitable for the microcontroller's ADC (Analog-to-Digital Converter) input. The scaled output ensures that the maximum voltage of 19V is reduced to around 1.14V for safe measurement by the controller.

5.2.3. Control System and Interfacing

The control system for the SEPIC converters was developed and implemented through MATLAB/Simulink and executed using an Arduino UNO microcontroller. The control algorithm leverages a linear quadratic regulator (LQR) combined with integral action to achieve stable voltage regulation and equal current sharing between the two converters. The algorithm was designed and simulated in Simulink, with real-time implementation on the Arduino UNO.

The PWM signals necessary for driving the SEPIC converters are generated by the Arduino UNO based on the control outputs from Simulink. These PWM signals control the duty cycle of each SEPIC converter's MOSFET switch, thereby regulating the output voltage.

5.2.4. Arduino and Simulink Integration.

The Arduino UNO is interfaced with Simulink using the Arduino Support Package, allowing real-time execution of the control algorithm. This integration enables the seamless transition from simulation to hardware implementation. The duty cycle for each converter is calculated in real time based on feedback from the output voltages, and the PWM signals are generated accordingly.

5.2.5. Performance and Results

The hardware setup successfully demonstrated the capability to regulate the output voltage and maintain balanced current sharing between the SEPIC converters. At an output voltage of 12V and a load current of 1.2A, the two converters shared the load,

with one supplying 0.55A and the other 0.56A. This performance was achieved under various load conditions, and the system showed resilience in maintaining stability even with changes in the load. The feedback control system ensured minimal deviation from the target voltage under these conditions, demonstrating robust and effective performance. The results are given in Figures below.

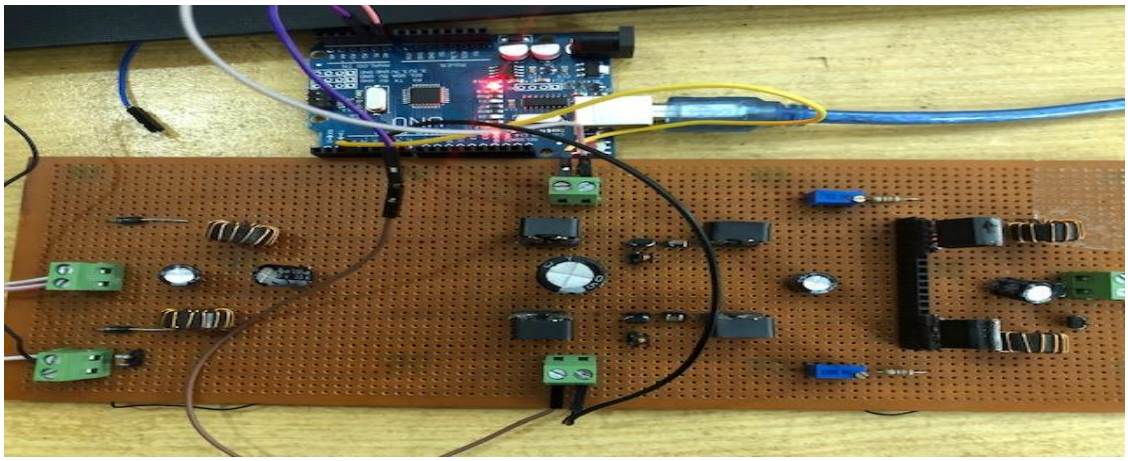


Figure 5.9: Hardware Setup.

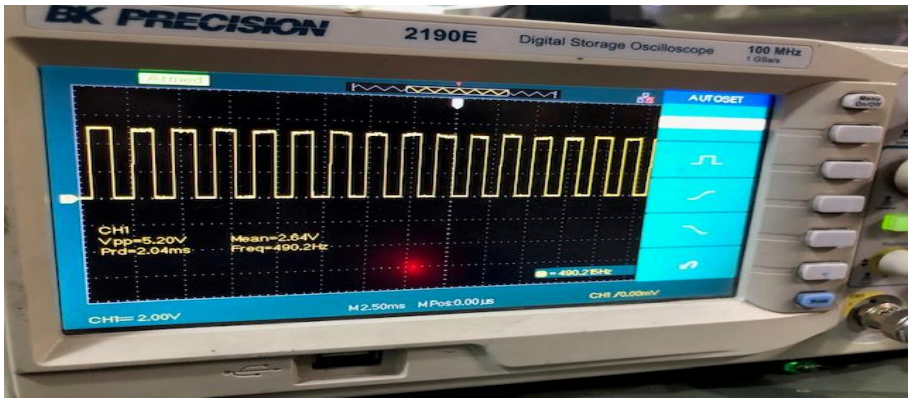


Figure 5.10: PWM Generation.

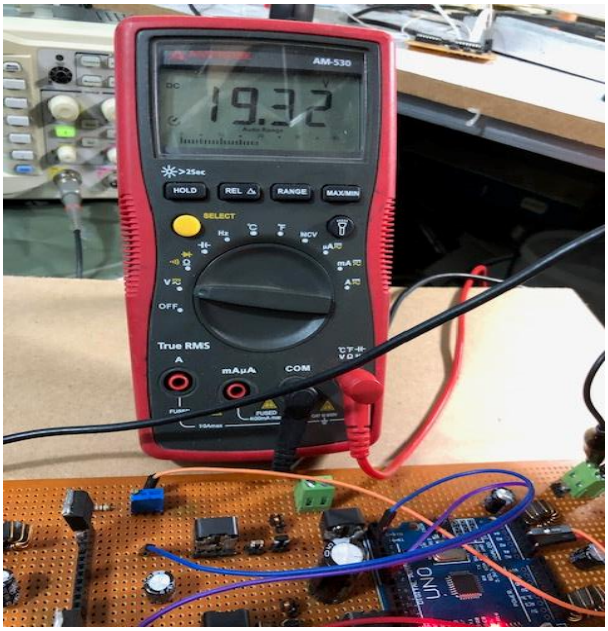


Figure 5.11: Load Voltage.

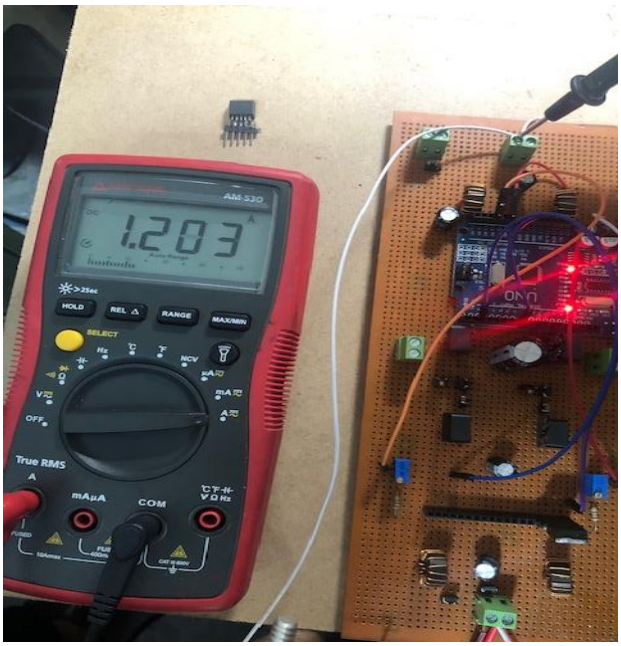


Figure 5.12: Load Current.

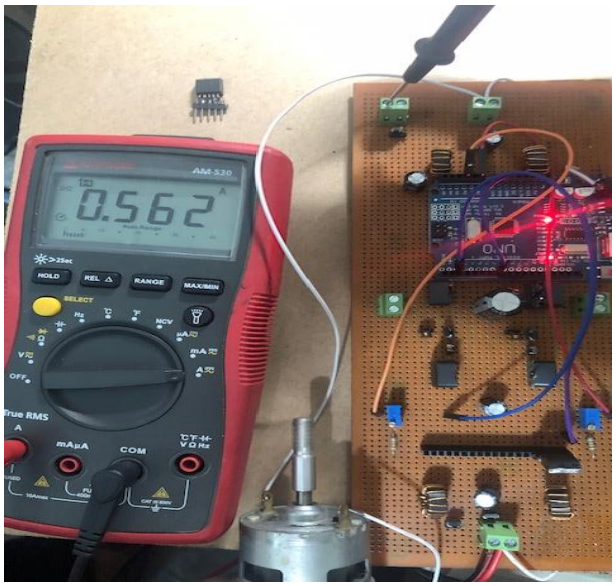


Figure 5.12a: 1st Module Load Current**.**

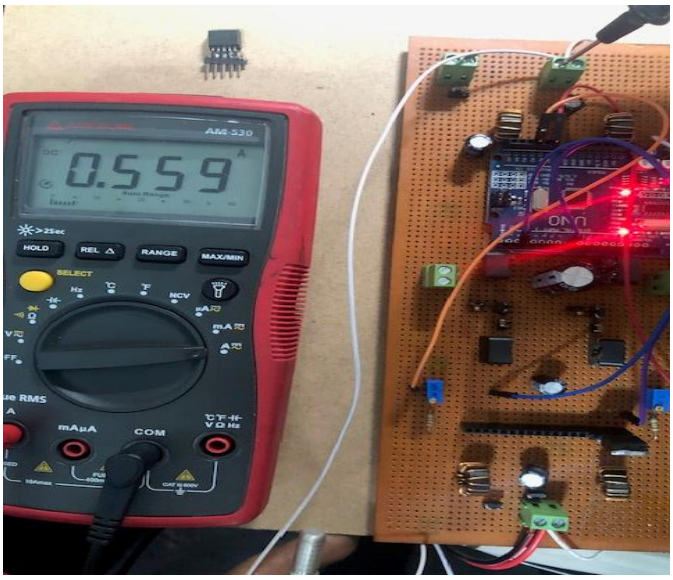


Figure 5.12b: 2nd Module Load Current.

Chapter 6

Outcomes and Conclusion

One of the major outcomes of this work is that the input source for this scheme can be renewable form of voltage sources provided the input voltage is given in parallel. This allows to deploy metaheuristic algorithms or other efficient algorithms for maximum extraction of renewable energy for an instance MPPT techniques in solar based renewable energy. The control scheme developed for the parallel-connected SEPIC converters, based on LQR and LQG design, successfully achieved both precise voltage regulation and equal current sharing under varying load conditions. This robust control approach efficiently handled switching noise and maintained system stability, with the converters sharing the load almost equally while delivering the required output voltage across a range of 9V to 19V. The integration of Simulink with Arduino UNO provided seamless real-time control, demonstrating the viability of this approach for decentralized control in DC microgrid applications. Future work could involve extending the control scheme to accommodate more converters, optimizing real-time performance with faster microcontrollers, and incorporating adaptive algorithms to improve resilience under dynamic load conditions or system faults. Additionally, investigating the control of different converter topologies within the same microgrid could enhance the flexibility and scalability of the system.

Based on the simulation results this proposed method can be used with any algorithm of Machine learning (ML) and Artificial Intelligence (AI) for generation of reference voltage extracting maximum energy point from renewable sources like solar energy. An extension of this work is done in the area of bidirectional SEPIC converter using the proposed scheme in this work for buck operation in smart buildings, is performed in another study and the results of this were very promising which further weights and seconds this study's outcomes and results. Since only the ESR of inductors are considered in the modeling of the SEPIC converter further extension of this work can be done including the ESRs of capacitors.

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