Fast Transient Dual Mode Low Dropout Regulator for Power Management in SoCs

By

Shirin Qaisar

361368

Department of Electrical Engineering

A thesis submitted in conformity with the requirements for the degree of *Master of Science* in Electrical Engineering

In

School of Electrical Engineering and Computer Sciences (SEECS), National University of Sciences and Technology (NUST), Islamabad, Pakistan

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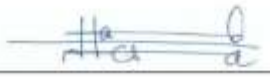
Signature: 

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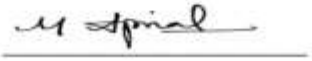
Signature (Dean/Principal): 

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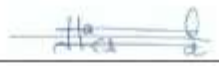
Signature: 

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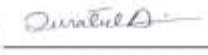
Signature: 

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Dedication

This thesis is dedicated to my *parents*.

Acknowledgement

All praise is to Allah Almighty, who bestowed knowledge and wisdom on humanity. First and foremost, I would like to express my gratitude to Allah, who gave me the courage to achieve my goal.

Additionally, I sincerely thank Dr. Hammad M. Cheema, my research supervisor, Dr. Sohmyung Ha and Dr. M. Abrar Akram for their unwavering support, strong attention to detail, and inspiring leadership throughout every stage of my work, all of which made it possible for me to finish my thesis.

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Abstract

This work presents an Analog-assisted Fast-transient Digital Low Dropout (LDO) regulator for power management systems through an innovative integration of Analog and Digital control loop methodologies. The design contains a charge-pump-based fine loop to provide accurate voltage regulation, attaining an output voltage ripple of merely 0.14 mV. The Digital LDO, on the other hand, indicates steady-state voltage ripples (V_{RIPP}) below 140 μV and functions with a minimum dropout voltage of 20 mV, making it suitable for both noise-sensitive analog circuits and power-efficient digital regulators in system-on-chip (SoC) devices.

A key feature of this architecture is the steady-state control system making use of a voltage-to-interval converter and a charge pump. This method successfully eliminates V_{RIPP}, giving improved stability in steady-state conditions. The rapid transient response of the regulator is achieved by combining dual-edge-triggered shift registers (DTSR) in the coarse loop, facilitating quick adjustments to abrupt variations in load current (I_{LOAD}). Additionally, the design adds an Analog-assisted (AA) loop, which is necessary for reducing voltage undershoots during load variations, hence providing definitive performance in dynamic settings.

Digital LDO regulator is designed in 180-nm CMOS technology, occupying an active area of 0.253 mm². Simulated results demonstrate a line regulation of 8 mV/V and a load regulation of 0.081 mV/mA. This LDO regulator is capable to deliver a maximum load current of 75 mA with a peak current efficiency of 99.93%, rendering it an efficient and feasible option for modern power management needs.

This architecture attains rapid transient response and minimum voltage ripples, creating a new standard in voltage regulation. Its distinctive properties make it suitable for complex applications in portable electronics, high-speed processors, and other systems needing stable, efficient, and noise-free power supply. It enhances ripple suppression and transient performance, making itself a state-of-the-art solution for next-generation power management in SoC devices.

Keywords: Low Dropout Regulator (LDO), Digital LDO (DLDO), Analog LDO (ALDO), Hybrid LDO (HLDO), Dual-Edge-Triggered Shift Registers (DTSR), Analog Assisted (AA) Loop

Chapter 1

Introduction

In today's rapidly advancing technological world, the demand for high-performance, energy-efficient electronic devices has never been greater. With the increasing prevalence of Internet of Things (IoT) devices, wearable technology, and AI accelerators, the importance of efficient power management systems has become critical. Ensuring that these systems can provide reliable, noise-free power while maximizing overall efficiency is fundamental to their performance and sustainability.

At the core of mobile phones and similar devices lies the System-on-Chip (SoC), which integrates a variety of components such as digital, analog, and radio frequency (RF) circuits. Each of these circuits requires a stable and precise power source to function effectively. Power management units (PMUs) are responsible for ensuring that every component of the SoC receives the appropriate power supply. In addition to the main power source, SoCs often rely on compact, on-chip secondary regulators to distribute and regulate voltage for individual components, ensuring both stability and precision across the entire system [1].

Power supplies in these systems frequently experience fluctuations in both voltage and current due to varying operational demands. Voltage regulators are therefore essential in converting these unstable supplies into a stable, constant, and load-independent voltage. This ensures that all components of the SoC, regardless of their function, receive the necessary power to operate optimally without disruptions or inefficiencies [2].

In modern SoC (System-on-Chip) designs, efficient power management is critical for ensuring optimal performance and stability. Fig. 1.1 shows how DC-DC converters supply various subsystems like digital, analog, and RF components through Low Dropout Regulators (LDOs). These regulators refine the power delivered to different blocks, ensuring a stable, noise-free voltage supply even under varying load conditions. This structure is crucial for maintaining efficiency and performance in devices such as mobile phones and IoT applications, where consistent power delivery is vital for reliable operation [3-8].

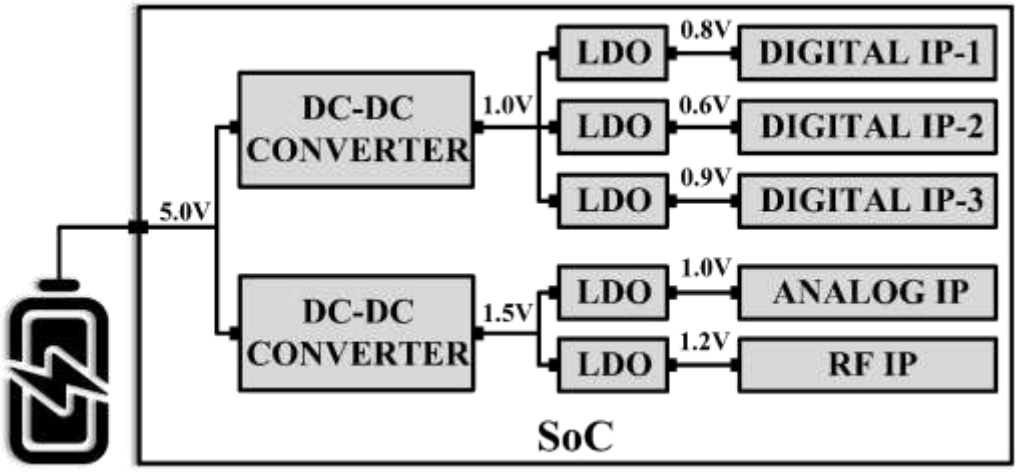


Figure 1.1: Power Management Unit in a SoC.

1.1 On chip DC-DC Converters

In the realm of integrated circuit (IC) design, the importance of power management cannot be overstated, especially as modern technology continues to demand more from electronic devices. DC-DC converters, which transform direct current (DC) from one voltage level to another, have been pivotal in meeting these demands. These converters are crucial for providing the necessary voltages to various components within a system, enhancing energy efficiency, and ensuring the optimal functioning of sensitive electronic parts. Integrating DC-DC converters on a chip has become increasingly common due to their ability to achieve efficiencies often exceeding 90%, which is vital for extending the battery life of portable devices such as smartphones and laptops. This high efficiency minimizes energy wastage, thereby maximizing the operational longevity of battery-powered gadgets [5, 8].

One of the primary advantages of on-chip DC-DC converters is their capacity to provide stable and precise voltage levels, maintaining consistent power supply despite fluctuations in input voltage. This stability is critical for the reliable performance of various IC components. Moreover, the integration of these converters directly on the IC helps reduce the size and weight of power supplies, a significant advantage in the design of compact, portable electronics, electric vehicles, and aerospace systems where space and weight savings are paramount. Embedding these converters on the IC also eliminates the need for external components, leading to more compact and reliable designs. Different types of DC-DC converters cater to various application needs. Buck converters step down voltage, making them suitable for applications requiring a lower output voltage than the input. Boost converters, on the other hand, step up the voltage, ideal for scenarios where a higher output voltage is needed. Buck-boost converters offer flexibility by either stepping up or stepping down the voltage as required,

while flyback and forward converters provide electrical isolation and are often used in power supply designs needing multiple output voltages.

Cost efficiency is another notable benefit of on-chip DC-DC converters, as they decrease the need for multiple distinct power supplies, thereby lowering overall system costs. Their flexibility allows for the optimization of performance and efficiency across different system components, making them essential in complex IC designs. In renewable energy applications, such as solar power systems, these converters play a crucial role in maximizing energy extraction and efficient power management [9].

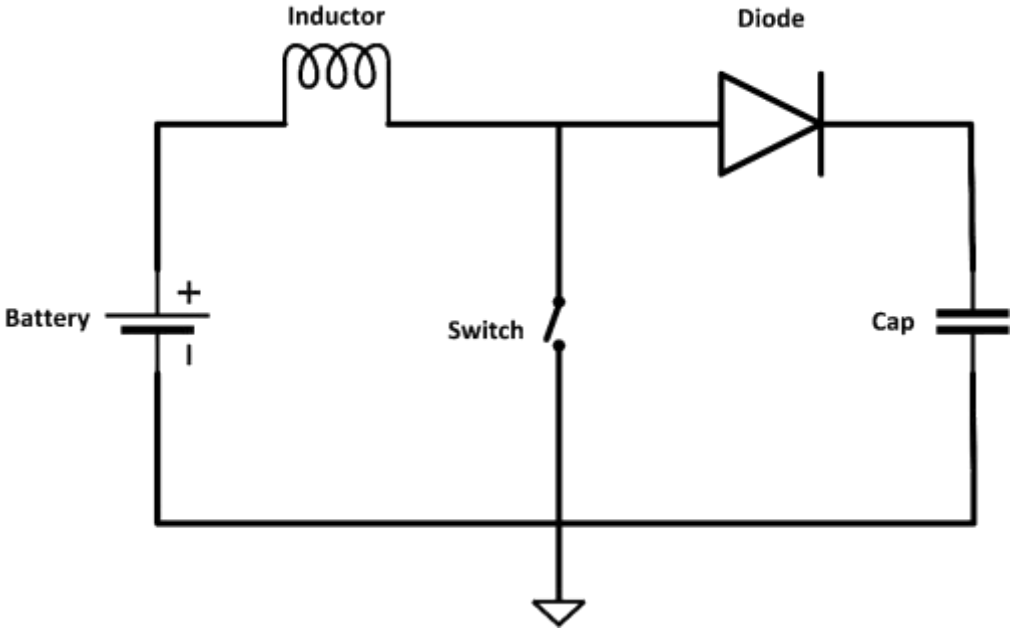


Figure 1.2: DC-DC Converter.

Fig 1.2 illustrates the boost DC-DC converter. A Boost DC-DC converter is a power converter that increases the input voltage to a higher output voltage. It is frequently utilized in scenarios where the input voltage is insufficient for the load's requirements. The operation of a Boost converter relies on the notion of energy storage in an inductor, which is subsequently released to the load at an elevated voltage upon the opening of the switch. The primary elements of the circuit consist of an inductor, a switch (often a MOSFET), a diode, and a capacitor. The inductor accumulates energy when the switch is closed and discharges it when opening the switch, resulting in an elevated voltage. The diode inhibits reverse current flow into the inductor, while the capacitor mitigates output fluctuations to diminish ripple. Efficiency is an essential factor in the performance of Boost converters, with losses primarily arising from the switch, diode, and inductor. The switching frequency, component quality, and control

methodology substantially influence efficiency. Boost converters are extensively utilized in portable electronics, renewable energy systems, and LED drivers because of their capacity to effectively elevate voltage. Nonetheless, they face obstacles including electromagnetic interference (EMI), output voltage ripple, and design complexity. Considering these constraints, Boost converters are essential components of contemporary power management systems, providing a compact and dependable method of voltage conversion. Progress in component technology and control methodologies persistently enhances their efficiency and performance [10].

However, despite their numerous advantages, on-chip DC-DC converters encounter significant challenges, especially in low-voltage operations. The complexity of their design and implementation can be daunting, requiring precise engineering to ensure both efficiency and reliability. Additionally, they can generate electromagnetic interference (EMI), potentially affecting nearby electronic devices if not properly managed. The initial cost of developing high-quality on-chip DC-DC converters can be substantial, although this is often offset by the long-term benefits in energy savings and system efficiency. Moreover, integrating DC-DC converters on a chip requires more silicon area, which can be a limitation in space-constrained designs. When these converters are not integrated on the chip, these introduce transient delays, which can impact the performance of the system.

In contrast to above mentioned DC-DC convertors, low Dropout Regulators (LDOs) [11] have been demonstrated as a superior alternative to DC-DC converters for on-chip power management in low-voltage applications. LDOs offer simpler design, lower noise, and faster transient response compared to their DC-DC counterparts, making them more suitable for specific applications where these attributes are critical. Furthermore, LDOs require less silicon area compared to DC-DC converters, which is advantageous in space-constrained IC designs. They also avoid the transient delays associated with off-chip power management solutions, leading to improved overall system performance. In the subsequent chapters, we will delve deeper into the advantages of LDOs, exploring how they overcome the limitations of DC-DC converters in low-voltage scenarios and detailing the advancements that make LDOs an increasingly viable choice for modern IC designs. This exploration will provide a comprehensive understanding of why LDOs are not only a feasible but often preferable option for on-chip power management.

1.2 Low Dropout Regulator

In the realm of integrated circuit (IC) design, efficient power management is critical as modern technology increasingly demands more from electronic devices. Low dropout regulators (LDOs) have emerged as a vital component in this context, providing a simpler and more effective alternative to DC-DC converters, particularly in low-voltage applications where space, noise, and transient response are crucial considerations. LDOs are designed to offer highly efficient voltage regulation with minimal complexity, making them ideal for integrating directly into a chip. LDOs function by maintaining a consistent output voltage even when the input voltage drops close to the output level. This capability is crucial for the reliable operation of sensitive electronic components that require stable voltage. By integrating LDOs on a chip, designers can achieve a more compact and efficient power management system. Unlike DC-DC converters, which often necessitate numerous external components and complex designs, LDOs simplify the overall architecture, reducing both the size and cost of the system [11].

One of the key benefits of LDOs is their ability to provide a clean, low-noise output, which is essential for applications involving sensitive analog circuits. This low noise characteristic is particularly beneficial in RF and audio systems, where high signal integrity is required. Furthermore, LDOs exhibit fast transient response times, allowing them to quickly adapt to changes in load conditions and ensuring stable operation of fast-switching digital circuits. This rapid adjustment capability is a significant advantage over DC-DC converters, which may introduce delays [12-15].

Different types of LDOs cater to various application needs. Standard LDOs offer basic voltage regulation suitable for general-purpose use, while low-noise LDOs are tailored for applications sensitive to voltage fluctuations. High-PSRR LDOs are designed to reject input supply noise effectively, making them ideal for delicate analog circuits. Ultra-low quiescent current LDOs excel in battery-powered applications by minimizing current consumption during standby periods, thus extending battery life. Each type of LDO addresses specific requirements, enhancing its applicability across diverse fields. Despite these advantages, LDOs also present some challenges. Its efficiency can decrease when there is a significant difference between input and output voltage, leading to higher power dissipation and heat generation. This limitation requires careful thermal management, especially in high-power applications. Additionally, LDOs are efficient for small voltage differences but are not suitable for applications needing large voltage step-downs, whereas DC-DC converters might be more appropriate [16-18].

Recent advancements have introduced digital LDOs, which leverage digital control loops instead of traditional analog feedback mechanisms. Digital LDOs offer several enhancements over analog counterparts, including improved transient response, better stability, and easier integration with digital systems. The precise control afforded by digital mechanisms allows for more efficient and scalable voltage regulation, making digital LDOs particularly well-suited for modern IC designs. Its compatibility with digital processes simplifies integration, facilitating more sophisticated power management strategies within complex systems.

In summary, while DC-DC converters have traditionally been employed to meet various power requirements, LDOs, particularly digital LDOs, offer significant advantages for on-chip power management in low-voltage applications. Its simplicity, low noise output, rapid transient response, and compact size make them ideal for a wide range of applications. Although it has limitations regarding efficiency at high dropout voltages, the advancements in digital LDO technology provide solutions that enhance overall performance. The following chapters will delve deeper into these advantages, elucidating why LDOs, especially digital LDOs, are increasingly integral to modern IC design.

1.3 Types of LDOs

In the domain of system-on-chips (SoCs) and other integrated circuits, low dropout (LDO) regulators are essential for ensuring stable voltage supply to various electronic subsystems. LDOs can be broadly categorized into analog LDOs (ALDOs) and digital LDOs (DLDOs), each tailored to meet specific operational requirements. Analog LDOs utilize analog control loops typically involving operational amplifiers (op-amps) to regulate output voltage. These regulators are renowned for excellent stability and low output voltage noise, making it ideal for powering sensitive analog circuits such as analog-to-digital converters (ADCs) and radiofrequency (RF) components. However, ALDOs often come with higher dropout voltages and larger physical footprints compared to its digital counterparts [19].

Digital LDOs (DLDOs), in contrast, employ digital control techniques to regulate output voltage. These regulators utilize digital-to-analog converters (DACs) and sophisticated control algorithms to adjust the output voltage dynamically based on load requirements. DLDOs are favored for their compact size, fast transient response, and lower dropout voltages, making them well-suited for powering digital circuits in SoCs where space and power efficiency are critical considerations [11, 20-23].

Within DLDOs, various design approaches exist to optimize performance. Fixed-gain dual-loop DLDO architectures, for example, employ nested feedback loops to achieve rapid response times and efficient power management. These designs adjust output voltage by manipulating either the reference voltage or the current through the output transistor. Despite their effectiveness in many applications, fixed-gain DLDOs can exhibit drawbacks such as voltage ripples and compromised power-supply rejection ratios (PSRR) [21-24].

Fig 1.3 shows the basic structure of a Digital Low-Dropout (LDO) regulator. It includes a feedback loop where the comparator (COMP) compares the reference voltage with the output voltage (V_{OUT}) on this comparison, the comparator controls a series of transistors (Q1, Q2, etc.) in the Binary LDO SR block to adjust the current and stabilize the output. The LDO ensures that the output voltage remains stable even with variations in the input or load, which is essential in digital circuits where precise voltage control is required to maintain performance and reduce noise.

This regulated control is crucial for systems that require efficient and stable voltage regulation at lower power levels, such as in power-sensitive SoCs (System on Chips).

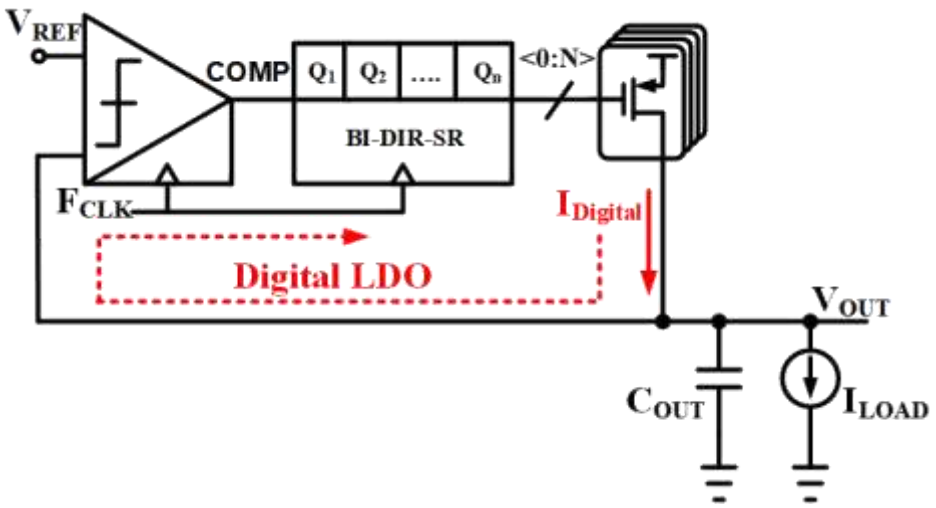


Figure 1.3: Block diagram of a Digital LDO Regulator showing feedback control and regulation of the output voltage.

Analog LDO regulators have traditionally been the dominant choice for power management because of their accurate voltage regulation and minimal noise properties [25]. Nevertheless, as CMOS technologies have scaled down, digital LDOs (DLDOs) have gained popularity because of their compact footprint, quicker transient response, and seamless integration with digital circuits. The design of low-dropout regulators (LDOs) for system-on-chips (SoCs)

requires careful consideration of various important variables, such as dropout voltage (V_{DO}), power efficiency, noise performance, and transient responsiveness. The trade-offs mentioned are particularly noticeable in digital LDO devices. The discontinuous nature of control generates quantization noise, while switching activities result in substantial voltage ripples (V_{RIPP}) [26-29].

Fig 1.4 shows the working of an Analog Low-Dropout (LDO) regulator. The error amplifier (EA) compares the V_{REF} with the V_{OUT} and adjusts the gate of a pass transistor to regulate the current flow (I_{Analog}) and maintains a steady V_{OUT}. The output capacitor (C_{OUT}) helps filter voltage noise, ensuring a smooth and stable supply to the load. Analog LDOs are widely used for their fast response and precise regulation of power in analog circuits.

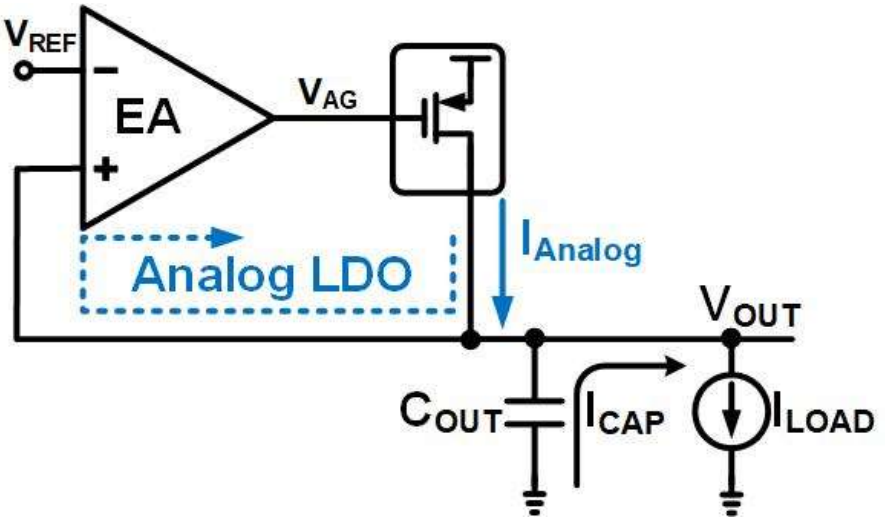


Figure 1.4: Block diagram of an Analog LDO regulator used for stable voltage output.

Hybrid DLDO configurations integrate both digital and analog control loops to harness the advantages of each approach. By leveraging digital control for fast adjustments and analog feedback for stability, hybrid DLDOs aim to mitigate the limitations inherent in pure digital or analog designs. These regulators often incorporate complex circuitry comprising error amplifiers, feedback networks, and precision voltage references to ensure precise regulation across varying load conditions [18, 28, 30, 31].

Fig 1.5 shows a power management unit that combines both Analog and Digital Low-Dropout (LDO) regulators for efficient voltage regulation. The Analog LDO (in blue) uses an error amplifier (EA) to compare the reference voltage (V_{REF})with the output and regulates the analog current (I_{Analog}). The Digital LDO (in red) leverages digital components to adjust the pass transistor and regulate the digital current ($I_{Digital}$). The combination of both analog and digital

LDOs ensures stable and efficient power delivery to different types of loads, optimizing performance in various system applications.

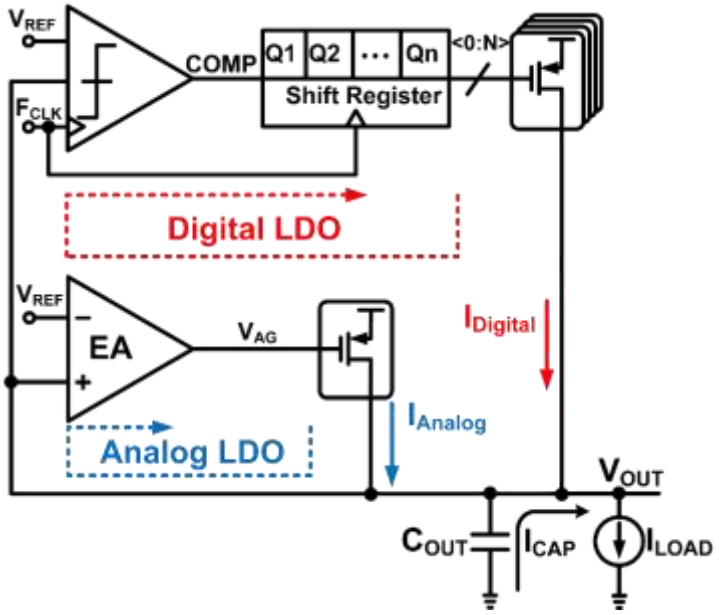


Figure 1.5: Combined Analog and Digital LDOs for voltage regulation.

1.4 Basic Operating Principle and Terminologies

Fundamentally, the operation of an LDO regulator revolves around maintaining a stable output voltage irrespective of variations in input voltage and load conditions. At its core, an LDO consists of a pass transistor, a feedback network, and a reference voltage source. The pass transistor acts as a variable resistor controlled by the feedback network, which compares the actual output voltage to a reference voltage set by the reference source. The feedback network adjusts the gate or base voltage of the pass transistor to maintain the desired output voltage despite changes in load current or input voltage.

Key terminologies essential to understanding LDO operation include dropout voltage (V_{DO}), which represents the minimum input-to-output voltage differential required for the LDO to regulate the output voltage effectively. Low dropout voltage is critical for maximizing power efficiency, particularly in battery-operated devices where minimizing power loss is paramount. Load regulation refers to the LDO's ability to maintain a stable output voltage even as the load current varies. Power-supply rejection ratio (PSRR) measures the LDO's capability to reject noise and fluctuations from the input voltage source, ensuring a clean and stable output voltage free from interference. The selection of components and the topology of the control circuit significantly influence the performance of an LDO regulator. Advanced techniques such as charge-pump-based fine loops and voltage-to-interval converters are employed to enhance

transient response and minimize output voltage ripple, addressing critical challenges faced by traditional DLDO designs. By integrating these innovations, modern LDO regulators aim to deliver superior performance metrics in terms of stability, efficiency, and reliability for demanding electronic applications.

1.5 Thesis Motivation and Objectives

LDOs play such an important role in power management applications and the handling of noise sensitive applications. due to which the demand for low dropout (LDO) regulators in modern system-on-chip (SoC) devices has substantially increased. The limits that are experienced with conventional digital low-dropout regulators (DLDOs) when they are included into these complex system-on-chip (SoC) environments are the primary source of inspiration for this thesis. Traditional DLDOs have several inherent drawbacks, including noticeable voltage ripples during steady-state operation (V_{RIPP}), inadequate power-supply rejection (PSR), and limited voltage regulation ranges. However, they do have some advantages, such as a quick transient response, a reduced silicon area, and the ability to scale.

1.5.1 Motivation

Due to advancements in semiconductor technologies and the shrinking size of electronic components, it has become more difficult to maintain power efficiency and provide resistance to noise. DLDOs are commonly chosen for digital loads because of their low quiescent current (I_Q) and compatibility with CMOS technologies. Nevertheless, the noise performance of the system, as measured by V_{RIPP}, is negatively affected by the discrete-time control loop and the characteristics of the digital switching components [11, 32]. Consequently, there is a requirement for a DLDO (Dual Loop Digital Low-Dropout) that may provide both high efficiency and low noise properties, which are suited for mixed-signal SoCs (System-on-Chips) that serve both digital and analog domains simultaneously. DLDOs are specifically engineered to accommodate swiftly fluctuating loads, particularly in situations where the load can transition from a few milliamperes to tens of milliamperes in a matter of nanoseconds [21]. Traditional designs may not adequately handle the fast changes, resulting in unwanted voltage drops or spikes that could endanger the stable functioning of the entire system. To provide a rapid reaction to quickly changing load currents (I_{LOAD}) and minimize voltage undershoots or overshoots (ΔV_{OUT}), enhanced architecture is required [20, 22, 23, 33, 34].

A significant issue in DLDOs is the low power supply rejection (PSR), which poses a problem when providing power to analog circuits or mixed-signal settings. In such cases, the power

supply noise can readily transfer to analog circuitry, leading to a decline in performance. Conventional DLDO systems face challenges in achieving high Power Supply Rejection (PSR) as with which noise from the supply voltage (V_{DD}) can enter the output voltage (V_{OUT}), especially when power transistors are operating in the deep-triode region. A method to improve PSR is required while keeping V_{RIPP} and V_{DO} at a low level.

Utilizing analog aid in DLDO designs has demonstrated promise in enhancing power supply rejection (PSR) and diminishing output voltage ripples. By integrating an analog-assisted (AA) loop, it is possible to promptly implement corrective measures during load transients, thereby minimizing voltage undershoots and decreasing the time required for recovery. This hybrid technique utilizes the benefits of both digital and analog control systems, hence improving the overall stability and performance of the regulator.

1.5.2 Goals

The purpose of the thesis is to develop a novel DLDO regulator chip that combines complex approaches to overcome the limitations discussed above. The specified goals include the following:

- A tri-loop structure should be incorporated into the DLDO that should consist of a digital coarse loop, a fine loop that is formed by a charge pump, and an analog-assisted loop. This combination is intended to provide a state of equilibrium that is characterized by rapid transient responsiveness, reduced voltage ripple, and enhanced power supply rejection levels.
- It is necessary for the design to achieve a steady-state voltage (V_{RIPP}) at a value lower than 140 µV and a dropout voltage (V_{DO}) of 20 mV or lower. This is done with the intention of achieving a higher degree of power efficiency and ensuring that the output has a low amount of noise. Therefore, the regulator is suitable for circuits that are sensitive to noise in analog signals and demand efficient power utilization in digital loads due to its programmability. This is because the regulator is programmable.
- It is recommended that the DLDO can achieve a Power Supply Rejection (PSR) of -30 dB at low frequencies, such as 1 kHz, to effectively suppress noise that originates from the input supply. Overall, the performance of fragile circuits that are supplied by the LDO would be improved because of this intervention.
- Achieving a maximum current efficiency of 99.93% while decreasing the I_Q required. Adjustments should also be made to the design to reduce the silicon area. This will ensure

that the integration into complex System-on-Chip (SoC) designs is as cost-effective as possible.

- It is recommended that a simulation of the proposed DLDO architecture be carried out to evaluate its performance in respect to the objectives that have been specified. With the help of a 180-nm CMOS process, one should design and validate the simulated results and then carry out exhaustive measurements to validate the efficiency of the design in a variety of different operational scenarios.

1.6 Thesis Structure

This thesis is organized as follows:

Chapter 1: Introduction to different Low dropout regulators and basis for this DLDO.

Chapter 2: Discuss the State of the Art and Operational Principles of the Proposed DLDO

This chapter provides a detailed explanation of how the new DLDO design operates. It delves into the functionalities of the voltage-to-interval converter and the charge-pump fine loop, illustrating how these components work together to stabilize and filter the output voltage. Additionally, it discusses the integration of dual-edge triggered shift-registers and segmented power transistors within this new design framework.

Chapter 3: Design and Simulated Results

This chapter presents the results of extensive testing conducted to evaluate the performance of the proposed DLDO. It includes detailed analyses, charts, and numerical data demonstrating the stability of output voltage, noise reduction capabilities, transient response times, and power efficiency metrics. These findings provide empirical evidence of the effectiveness and practical applicability of the new DLDO design in meeting the stringent requirements of modern SoCs.

Chapter 4: Conclusion and Future Directions

The concluding chapter summarizes the key findings and contributions of this thesis. It discusses the potential impact of the proposed DLDO architecture on advancing the field of low dropout regulators for SoCs. Furthermore, it outlines avenues for future research and development aimed at further enhancing the performance and versatility of DLDO technologies. By addressing the inherent challenges of traditional DLDO designs and introducing innovative solutions, this thesis aims to push the boundaries of LDO technology,

paving the way for more efficient and reliable power management solutions in next-generation electronic systems.

Chapter 5 serves as the conclusion of the thesis report. In addition to summarizing the key findings and contributions of the research, it offers insights into future work of the thesis.

Chapter 2

Literature Review

In today's advanced electronic devices, low dropout (LDO) regulators play a crucial role in ensuring stable power supply to different components within system-on-chips (SoCs). These regulators come into action after primary power conversion is performed by switching regulators. Their primary job is to maintain steady voltages with minimal fluctuations, which is essential for the reliable operation of both analog and digital circuits, particularly in environments sensitive to electrical noise [11].

Digital LDOs (DLDOs) have gained popularity due to it’s compact size, efficient power management, and ability to quickly adjust voltage based on the demands of the device. However, they face several challenges [7], [8]. To address these challenges, engineers have explored various design approaches as one approach involves using fixed-gain dual-loop systems, which is designed to respond quickly to changes in power requirements while optimizing power consumption. However, these systems can introduce voltage ripples due to its discrete control mechanisms during operation [20, 22, 23, 32]. Another strategy involves freezing digital output when the voltage is stable to minimize ripples. While effective in stabilizing voltage output, this method can sometimes cause slight over-voltage or under-voltage conditions when the system is under low power demand [32, 35-37]. Hybrid DLDO designs combine digital and analog control loops to leverage the strengths of both technologies. These designs aim to stabilize voltage output and minimize noise interference. However, they often require higher dropout voltages and may not operate efficiently across a wide range of voltage levels [26, 27, 38].

The literature review chapter provides a comprehensive analysis of the digital low dropout (DLDO) regulator architectures that are currently in use, as well as their evolution over the course of time and the advancements that have been made to address issues concerning noise performance, transient response, power-supply rejection ratio (PSR), and voltage regulation. The investigation begins with a straightforward evaluation of DLDO designs, and then moves on to more complex configurations, such as dual-loop designs, freezer circuits, and hybrid architecture, ending in the proposed tri-loop architecture that is described in this thesis.

2.1 Baseline Design

The baseline design of DLDO illustrated in Fig 2.1. Initial development of DLDO regulators was motivated by the need to overcome the limitations of analog LDOs, particularly regarding the integration of these regulators with digital circuits, speed, and scalability features. The primary motivation behind the development of DLDOs was to make use of the advantages that digital control offers, such as a more rapid response to transients, a more compact design, and compatibility with more highly developed CMOS technologies. Baseline direct current (DLDO) systems typically make use of a single digital feedback loop to operate a set of pass transistors to regulate the output voltage (V_{OUT}) [39]. The following are the fundamental components that make up a baseline DLDO:

1. The digital error amplifier is a component that generates a digital error signal by comparing the output voltage (V_{OUT}) to a reference voltage (V_{REF}) and then producing the result of this comparison.
2. Switch Register or Binary-Weighted Array: The error signal is then controlled by either a shift registers or a binary-weighted array. Both options are available. The output voltage can be controlled through this manipulation by adjusting the number of active power transistors such that it is constant.
3. A collection of pass transistors, typically PMOS that are responsible for delivering the regulated output, is referred to as a power transistor array. To modify the output voltage (V_{OUT}), digital control is responsible for regulating the number of functioning transistors.

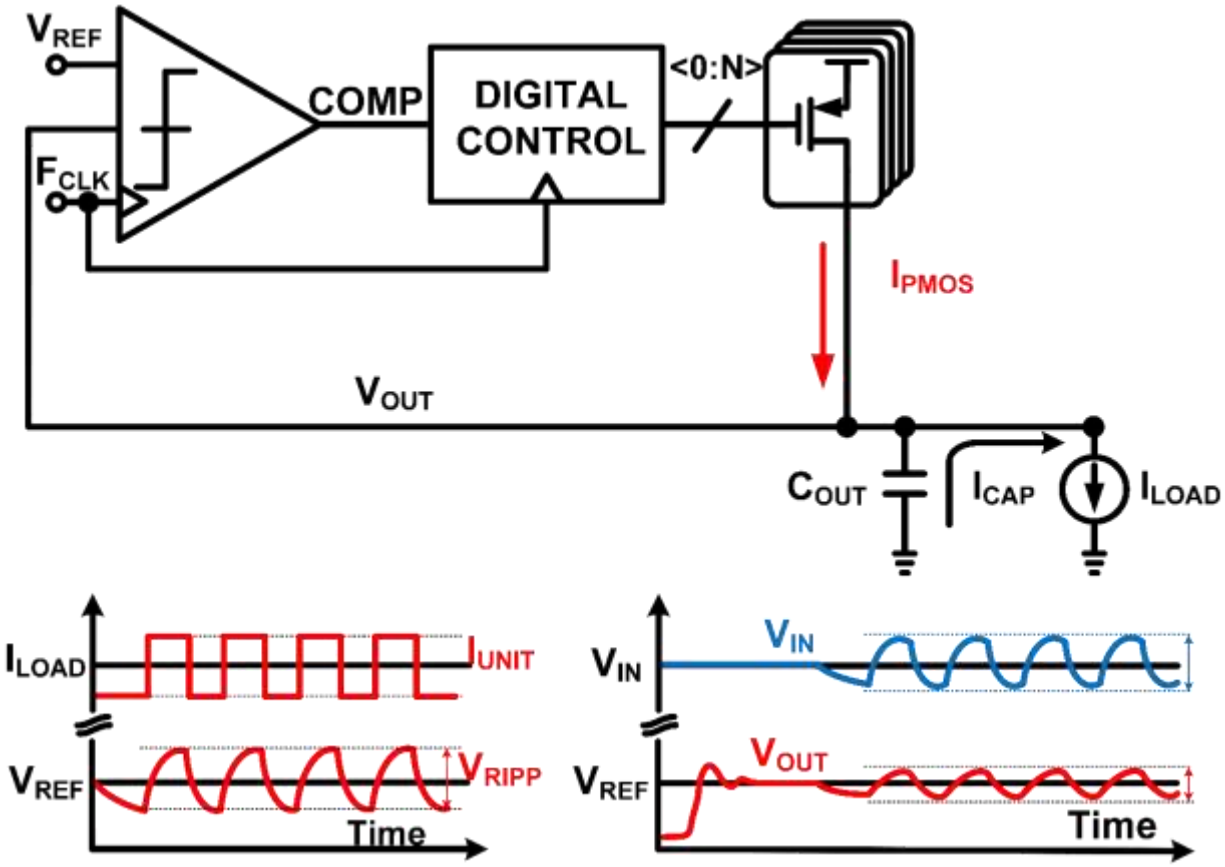


Figure 2.1: Baseline DLDO.

Even though these preliminary designs offered improvements in terms of size and response speed, they were not without significant drawbacks:

1. The discrete-time structure of the digital control loop and the switching of the power transistors are the two factors that allow baseline DLDOs to have notable voltage fluctuations in the steady state. This phenomenon is referred to as steady-state voltage ripples (V_{RIPP}). Considering that analog circuits are extremely sensitive to noise, this degree of ripple is undesirable.
2. The digital structure of the control renders it sensitive to the coupling of noise from the supply voltage (V_{DD}) to the output voltage, which results in a drop in power supply rejection (PSR). This is referred to as inadequate power supply rejection (PSR).

2.2 Digital LDO

Throughout the years, numerous recommended enhancements have been proposed in order to alleviate the limitations that are associated with typical DLDO systems. The dual-loop

topologies, freezer circuits, and hybrid systems that integrate digital and analog control techniques are all included in this category as shown in Fig 2.5.

2.2.1 Fixed Gain Dual Loop DLDO

The fixed gain dual loop DLDO shown in Fig 2.2 was developed with the intention of improving the steady-state performance of digital LDOs as well as their responsiveness to transients. The following feedback loops are included in this architectural design:

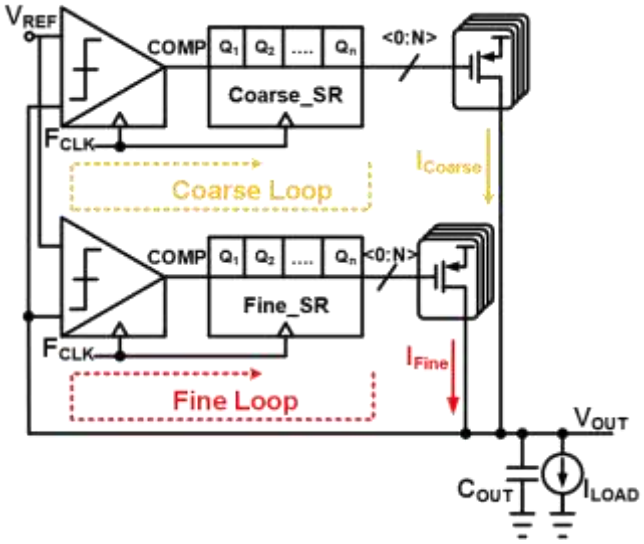
1. **Coarse Loop:** The coarse loop is a high-speed control system that swiftly adjusts the output voltage by rapidly toggling multiple power transistors between ON and OFF states. This allows the coarse loop to quickly modify the output voltage. It operates at high frequencies with the purpose of managing sufficient load transients.
2. **Fine Loop:** This loop operates at a lower frequency and adjusts the output voltage that is more exact than other loops. Through the manipulation of the number of active transistors, it contributes to the reduction of fluctuations in the steady-state voltage over time.

The coarse loop is responsible for making rapid adjustments to the number of active power transistors if load transients occur. This is done in order to bring the output voltage into alignment with the reference voltage. At the point that the output voltage reaches a particular range that is quite near to the reference voltage, the fine loop becomes active and begins to perform modifications that are more precise and smaller in order to reduce V_{RIPP} and maintain the output that was intended [21-24].

The dual-loop architecture in the DLDO allows the system to adapt quickly to significant variations in load, enhancing the overall transient response. The coarse loop manages these large fluctuations efficiently, while the fine loop provides more precise control, resulting in reduced voltage ripple (V_{RIPP}) compared to more conventional designs. However, while these improvements are notable, the system still exhibits limitations, particularly in its Power Supply Rejection (PSR). This limitation means that noise in the input supply can still affect the output, especially when the system operates primarily in the coarse loop [21-24].

Moreover, the inherent complexity of the dual-loop design increases the control logic's difficulty. Both loops must be precisely tuned to ensure stability and optimal performance, which can present challenges, particularly when noise or other external disturbances are present

in the system. This observation aligns with findings from previous research**,** which also reported that noise susceptibility remains an issue in similar architectures [22].



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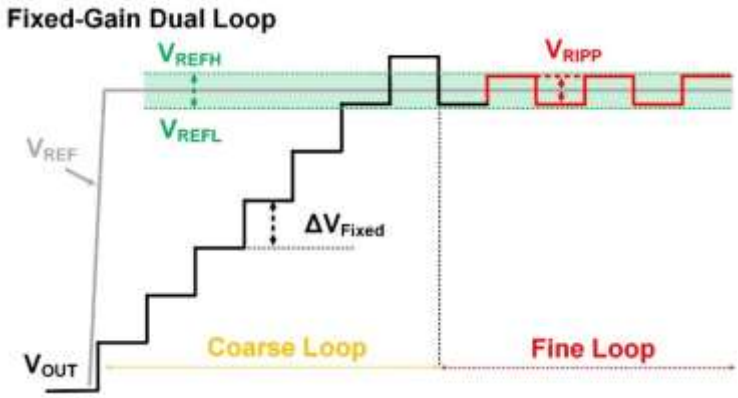


(b)

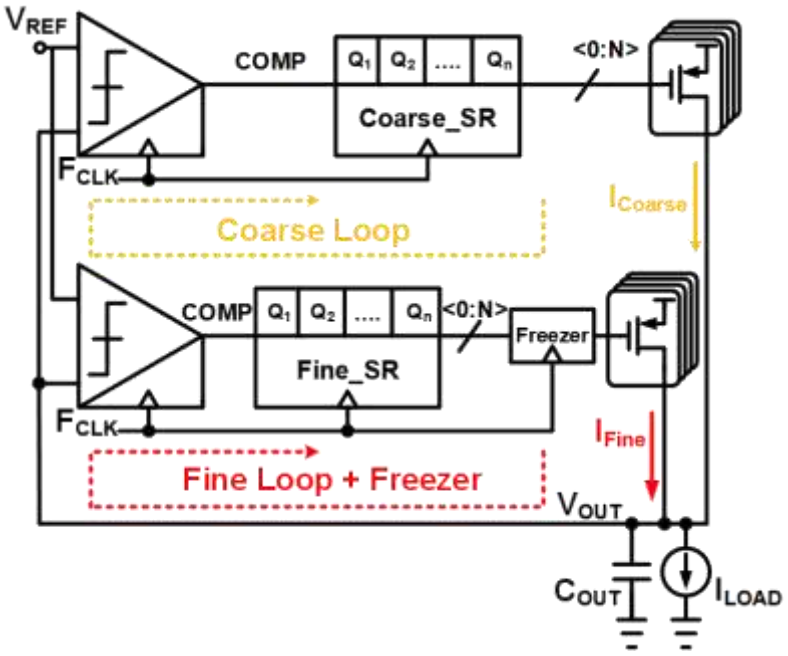
Figure 2.2: Fixed-Gain Dual Loop DLDO (a) internal circuit (b) graphical representation.

2.2.2 Fixed Gain Dual Loop with Freezer

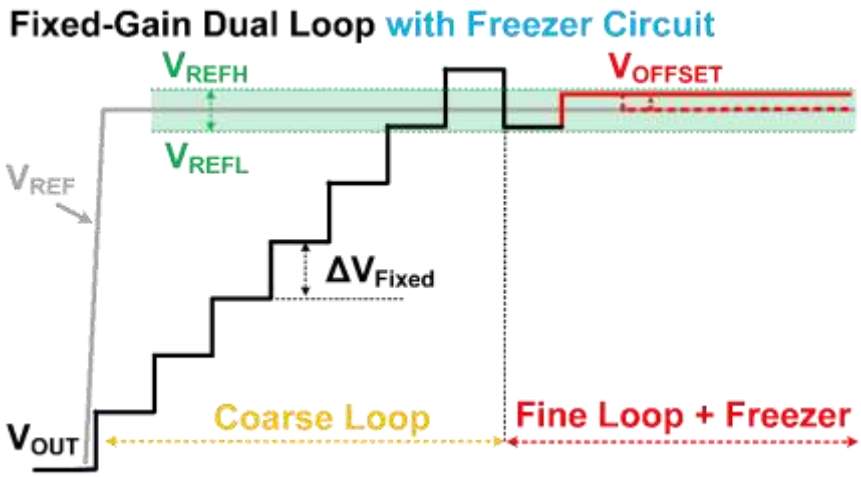
A "freezer" circuit was incorporated into the fixed gain dual-loop architecture shown in Fig 2.3 to enhance the steady-state performance of dual-level dual-range oscillators (DLDOs). When the output voltage is within a small range of the reference voltage (V_{REF}), the freezer circuit shuts off the switching of power transistors. This is done with the intention of reducing the number of voltage fluctuations that occur. There is constant monitoring of the voltage that is produced as output by the freezer circuit when it is really operating. The switching of the power transistors is halted or stopped by the freezer circuit when the output voltage falls within

a specified range that is almost equal to the V_{REF}. This procedure inhibits wasteful switching, which is the primary cause of ripples in digital regulators, which results in a decrease in the steady-state voltage ripple in the voltage (V_{RIPP}) [23].

By effectively reducing switching noise, the freezer circuit can effectively attenuate voltage ripples in a steady state, which ultimately results in a large reduction in ripples produced. By decreasing the frequency of switching, the quiescent current (I_Q) is also decreased, which results in an overall improvement in power efficiency. This is referred to as "Enhanced Efficiency." The freezer circuit generates a zone around VREF in which there are no voltage changes. This region has the potential to induce a deviation in the output voltage, which could potentially influence the precision of the voltage control. Although the freezer circuit reduces Voltage Ripple and Input Power Supply Rejection, it does not have a significant impact on Power Supply Rejection. This is because the output can still be affected by noise from the Voltage Drain-to-Drain due to the absence of continuous analog control. Despite this, the freezer circuit does significantly improve Power Supply Rejection.



(a)



(b)

Figure 2.3: Fixed-Gain Dual Loop with Freezer Circuit (a) internal circuit (b) graphical representation.

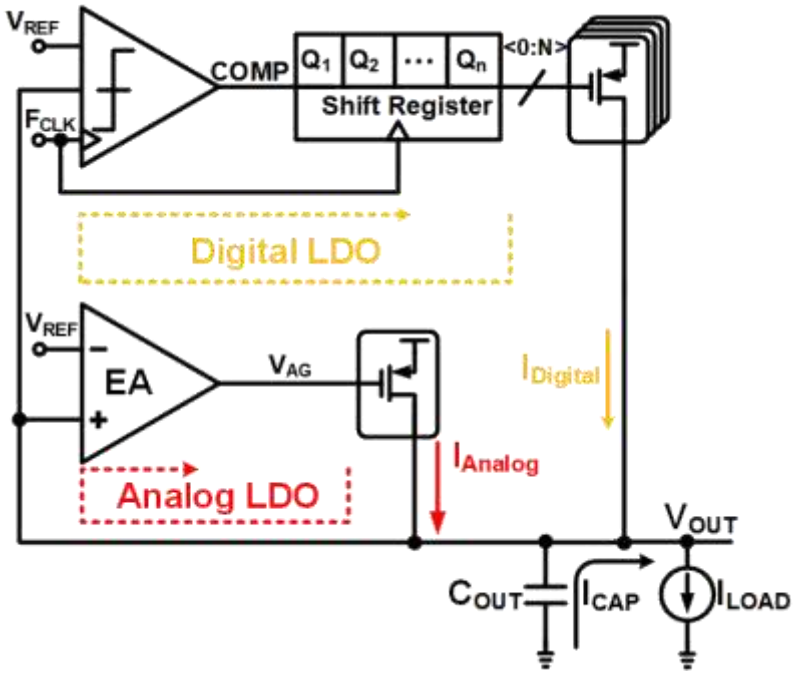
2.2.3 Hybrid LDO

To address the limitations of entirely digital DLDO systems as shown in Fig 2.4, the hybrid LDO design offers significant improvement. The advantages of both digital and analog control loops are utilized in a synergic manner by this architecture to achieve higher performance in terms of transient responsiveness, voltage regulation, output ripple and noise rejection, and power supply rejection. A rapid response to severe load changes is provided by the digital coarse loop, which operates in a manner that is analogous to the coarse loop of dual-loop direct current devices [40].

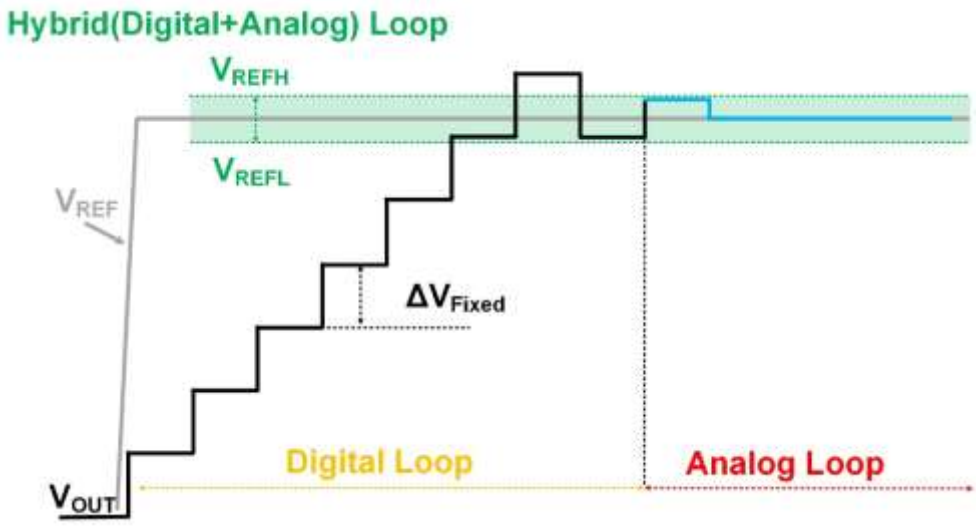
The Analog Fine Loop is a control loop that operates continuously and is responsible for making accurate adjustments to the output voltage. The assistance it provides in minimizing any disturbances and compensating for fluctuations caused by noise or rapid changes in load is a significant benefit. Accurate voltage regulation is made possible by the power transistor array, which is a collection of power transistors that can be controlled by both digital and analog signals. Through the rapid modification of the amount of active power transistors, the digital coarse loop is able to effectively manage substantial load transients. This is accomplished by aligning V_{OUT} with V_{REF}. The analog fine loop provides feedback and correction in a continuous manner, hence lowering the V_{RIPP} and increasing the PSR. This is accomplished by dynamically compensating for noise and other variations [35, 36].

The uninterrupted characteristic of the analog loop considerably boosts the Power Supply Rejection (PSR), making the hybrid Low Dropout (LDO) regulator appropriate for analog loads

that are sensitive to noise. The analog fine loop can successfully minimize voltage ripples by ensuring that the output voltage is controlled in a consistent and uninterrupted manner. The digital coarse loop can provide a rapid response to severe load changes by utilizing the benefits that are associated with both digital and analog control. However, hybrid design comprises supplemental components and control circuitry, which results in an increased overall complexity and silicon area requirement. The incorporation of an analog error amplifier and other analog components might result in an increase in the dropout voltage, which has the potential to reduce power efficiency. This possibility is a consequence of the inclusion of these components [32, 37].



(a)



(b)

Figure 2.4: Hybrid LDO (a) internal circuit (b) graphical representation.

2.3 Summary

The table presents a comparison of various LDO designs that have been explored in the literature review. These designs in Fig 2.5 include the baseline DLDO, fixed gain dual loop, freezer circuit, and hybrid LDOs. The table provides a concise overview of the main characteristics, benefits, drawbacks, and performance measurements (such as V_{RIPP}, PSR, transient response, etc.).

Table 1: Comparison summary of various LDO Designs.

Design	Advantages	Disadvantages	Key Metrics
Baseline DLDO	Fast transient response, small area	High V_{RIPP}, poor PSR	V_{RIPP}: High, PSR: Low
Fixed Gain Dual Loop DLDO	Improved transient response, reduced V_{RIPP}	Low PSR, complex control	V_{RIPP}: Medium, PSR: Low
Fixed Gain Dual Loop with Freezer	Minimal V_{RIPP}, reduced I_Q	Output voltage offset, limited PSR improvement	V_{RIPP}: Low, PSR: Medium
Hybrid LDO	Low V_{RIPP}, high PSR	Increased complexity and area, higher V_{DO}	V_{RIPP}: Low, PSR: High

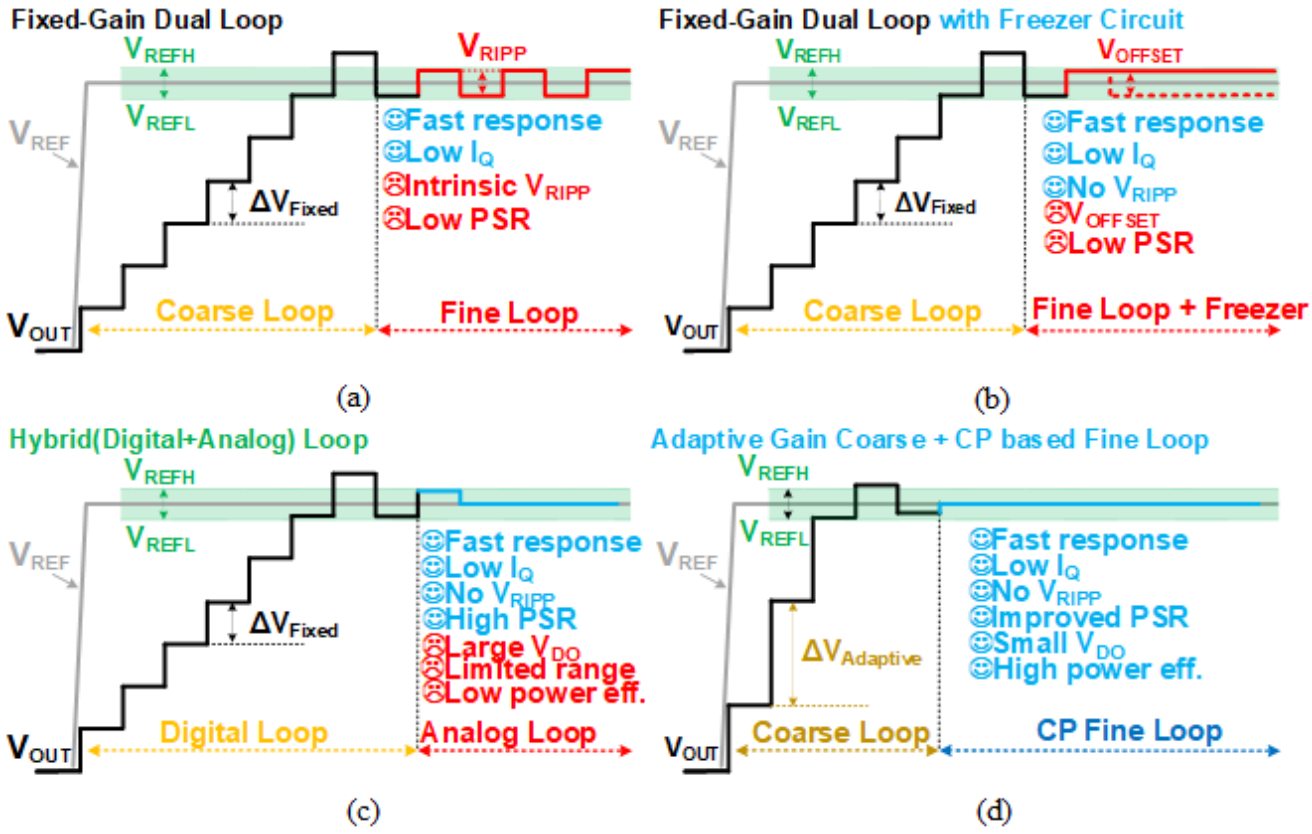


Figure 2.5: Start-up response and steady-state VRIPP comparison of various DLDO configurations, including (a) fixed-gain dual loop, (b) fixed-gain dual loop with freezer circuit, (c) hybrid (digital + analog) loop, and (4) the proposed adaptive-gain coarse and charge-pump-based fine loops.

To achieve the highest possible level of performance in contemporary System-on-Chip (SoC) environments, the development of DLDO designs is a demonstration of the ongoing effort to establish the optimal balance between digital and analog control techniques. Despite the progress made in LDO design, current solutions continue to face challenges in achieving an ideal equilibrium between V_{RIPP}, PSR, transient response, and power efficiency. This thesis aims to fill these deficiencies by introducing a new tri-loop design that combines digital, analog, and charge-pump control methods.

The inclusion of a freezer circuit in the fixed gain dual loop effectively decreases V_{RIPP}. However, this also introduces a dead zone that causes output voltage offsets, which can have negative effects in applications that require high precision. In addition, hybrid low-dropout (LDO) designs, although enhancing power supply rejection (PSR), also introduce greater design intricacy and occupies more silicon area, rendering them less preferable for highly integrated System-on-Chips (SoCs).

Initial digital designs were hampered by high voltage ripples and poor power supply rejection. Despite this, these were the basis for rapid expansion. Even though they were able to improve transient response and reduce ripples, fixed gain dual-loop topologies were not without share of difficulties in terms of noise performance. V_{RIPP} has been lowered even further under steady-state conditions because of the use of freezer circuits; however, this comes with the drawback of potential output voltage variations and limited benefits in power supply rejection [11, 20-24, 32-37]. When it comes to DLDO topologies, hybrid LDO designs are the most cutting-edge options. To deliver greater transient responsiveness, reduced voltage ripples, and enhanced power supply rejection, they mix digital and analog techniques.

The purpose of the research that is discussed in this thesis is to design a one-of-a-kind tri-loop DLDO architecture with the intention of enhancing the rapid transient response, low voltage ripple and noise, enhanced power supply rejection, and minimal voltage drop are all achieved by the integration of a digital coarse loop, a charge-pump-based fine loop, and an analog-assisted loop in this architecture.

This thesis introduces an innovative DLDO design aimed at overcoming these limitations. The proposed design incorporates a voltage-to-interval converter (VIC), and a charge-pump (CP)-based fine loop to achieve superior performance. These innovations not only eliminate voltage ripples and enhance noise rejection capabilities but also reduce the additional voltage required for the regulator to function effectively.

Table 2: Literature Review Table.

Ref.	**Year**	**Publication**	**CMOS [nm]**	**V_{IN} [V]**	**V_{REG} [V]**	**Max I_{load} [mA]**	**I_q [µA]**	**Total C_{load} [nF]**	**I_{SR} [mA/ns]**	**ΔV_{OUT} [mV]@ $\Delta I_{load,max}$ [mA], V_{OUT}[V]**	**Peak I Eff. [%]**	**FOM ****
[41]	2021	Electronics (MDPI)	180	1-1.2	0.95	100	34.68	0.5	40/1	36@40,0.95	99.64	0.05
[42]	2021	IEEE Access	90	0.35	0.3	2.4	5	N.A.	N.A.	N.A.	99.8	N.A.
[43]	2021	IEEE Access	55	0.8-1.5	0.76-1.46	5	3.18	0.022	4.5 / 1	85 @ 4.5, 1.456	99.996	N.A.
[44]	2020	TCAS-II	65	0.6-1.0	0.55-0.95	4.5	10.2	1	4.4 / 10	118 @ 4.4, 0.55	99.7	13.39
[45]	2020	IEEE Access	28	0.5-1	0.45-0.95	10	3.7	0.1	9.5* /1*	52*@9.5*, 0.95	99.97	N.A.

Ref.	Year	Publication	CMOS [nm]	V_{IN} [V]	V_{REG} [V]	Max I_{load} [mA]	Iq [µA]	Total C_{load} [nF]	I_{SR} [mA/ns]	ΔV_{OUT} [mV]@ $\Delta I_{load,max}$ [mA], V_{OUT}[V]	Peak I Eff. [%]	FOM **
[46]	2020	TPE	65	0.6-1.2	0.55-1.15	25	21.35	0.00084	24.5/20	96 @ 24.5, 1.15	99.91	225µ
[47]	2020	Etri Journal	65	0.6-1.2	0.5-1.0	100	75	1	90 / 20	47 @ 90, 1	99.93	0.09
[48]	2019	VLSI	14	0.5-0.85	0.45-0.8	11	0.69	0.1	10/4	122 @10,0.45*	N.A.	0.075
[49]	2019	ISSC	65	0.5-1	0.45-0.95	25	127	0.1	20/400	47@20, 0.45	N.A.	0.06
[50]	2019	TPE	130	0.5-1.22	0.35-1.17	145	N.A.	1.5	40/0.1	280@40,0.92*	97.8	6.88
[51]	2019	Electronics	55	0.5	0.45	1	2.3	0.0001	0.79 / 40	40 @ 0.79*, 0.45	99.99	0.4

Ref.	Year	Publication	CMOS [nm]	V_{IN} [V]	V_{REG} [V]	Max I_{load} [mA]	Iq [µA]	Total C_{load} [nF]	I_{SR} [mA/ns]	ΔV_{OUT} [mV]@ $\Delta I_{load,max}$ [mA], V_{OUT}[V]	Peak I Eff. [%]	FOM **
[52]	2019	CICC	130	0.83-1	0.6-0.8	25	N.A.	0.8	25 / 0.1	160 @ 25,0.8	99.4	N.A.
[53]	2019	JSSC	65	0.5-1	0.45-0.95	105	4.9	0.042	100/10	88 @ 100,0.5	99.995	150µ - 818µ
[54]	2018	ISCAS	28	0.5-1	0.45-0.95	33.2	10.5	0.1	30.7 / 20	101.7 @ 30.7,0.45	99.97	0.055
[22]	2018	JSSC	65	0.9-1.2	0.5-1.1	19	131	0.2	3/90	80@3,1	99.3	73.66
[55]	2018	JSSC	65	0.6-1.2	0.4-1.1	100	1070	0.04	50/1240*	108@50,0.8	99.5	0.30
[56]	2017	JSSC	65	0.5-1	0.3-0.45	<2	14	0.4	1.06/1	40@1.06,0.45	99.8	43µ
[57]	2017	TPE	65	0.7-1.2	0.6-1.1	25	6	1	23.5/2080*	200@23.5,0.6	99.97	0.47
[58]	2017	VLSI	130	0.84-1.24	0.6-1	50	400	0.5	40/10	250@40,0.6	99.2	2.15
[59]	2016	TPE	130	0.5-1.2	0.45-1.14	4.6	N.A.	0.9	N.A.	90@1.4,0.45	98.3	N.A.

Ref.	Year	Publication	CMOS [nm]	V_{IN} [V]	V_{REG} [V]	Max I_{load} [mA]	Iq [µA]	Total C_{load} [nF]	I_{SR} [mA/ns]	ΔV_{OUT} [mV]@ $\Delta I_{load,max}$ [mA], V_{OUT}[V]	Peak I Eff. [%]	FOM **
[60]	2015	TPE	130	0.45-1.2	0.35-1.15	1.5	8.9	1	1.48/50*	100 @ 1.48, 0.45	99.9	N.A.
[61]	2014	VLSI	110	0.6-1.2	0.5-0.9	80	32	1	80/25000	53@80,0.5	N.A.	0.03

*Values estimated from the graphs

**Normal value of FOM, the smaller the value the better the FOM.

Chapter 3

Circuit Design

An in-depth examination of the complex architecture of the tri-loop digital low dropout (DLDO) regulator is presented in Chapter 3. The major design challenges including rapid transient response, minimal voltage ripples (V_{RIPP}), enhanced power-supply rejection ratio (PSR), and low dropout voltage (V_{DO}) are discussed. A few innovative components and approaches have been incorporated into the design to achieve these objectives.

3.1 Conventional DLDO Architecture

3.1.1 Digital LDO

Digital LDO's rapid transient response, low silicon footprint, and ability to operate with conventional CMOS processes are highly preferred in the field of power management for SoC applications. The digital low-dropout regulator (DLDO) is a type of regulator that typically includes a digital error amplifier, a shift registers or binary-weighted digital-to-analog converter (DAC) for control, and a group of power transistors (often PMOS transistors) that modify the output voltage (V_{OUT}) in accordance with the control signals.

The operation of a conventional DLDO is accomplished by the utilization of a digital feedback loop, which is used to adjust the gate voltages of the power transistors to maintain a constant output voltage (V_{OUT}). If there is a disparity between the quantity of active power transistors and the reference voltage (V_{REF}), the digital controller will adjust the quantity of active power transistors to bring the voltage output (V_{OUT}) back to the level that was intended. Even though this technique is effective for digital loads, it has a few downsides, including excessive voltage ripple and low power supply rejection. Additionally, due to the discrete nature of digital control, it is wasteful when applied to low load currents.

3.1.2 Limitations of Conventional Design

Even though ordinary DLDOs have several advantages, they are also subject to a number of significant limitations:

- Steady-State Voltage Ripples (V_{RIPP}): The discrete switching of power transistors in digital control loops causes ordinary DLDOs to have high V_{RIPP}, which renders them unsuitable for analog loads that are sensitive to noise.
- Power-Supply Rejection (PSR) that is Inadequate: The noise in the supply voltage (V_{DD}) can easily transfer to the output voltage (V_{OUT}) because the fully activated power transistors are running in the deep-triode state, which results in a PSR that is below par.
- Restricted Regulatory Scope and Precision: Due to the discrete nature of digital control, the precision of voltage adjustments is restricted, which results in a limited range of regulation and accuracy.
- High Dropout Voltage: When it comes to digital systems, the dropout voltage is typically larger than in analog systems. This is because the on-resistance of fully activated power transistors cause the dropout voltage to be higher. It is possible that this will lead to a reduction in overall power efficiency.

These limitations necessitate a new way for designing DLDO (Digitally Controlled Low Dropout) regulators considering these constraints. This proposed new method should combine the benefits of digital control with enhancements in V_{RIPP} (Voltage Ripple and Power Supply Rejection Ratio), PSR (Power Supply Rejection), and transient response. This ultimately results in the tri-loop architecture that was suggested.

3.2 Proposed Tri Loop Architecture and sub-components

A digital coarse loop, a charge-pump-based fine loop, and an analog-assisted (AA) loop are all incorporated into the DLDO architecture that has been proposed.

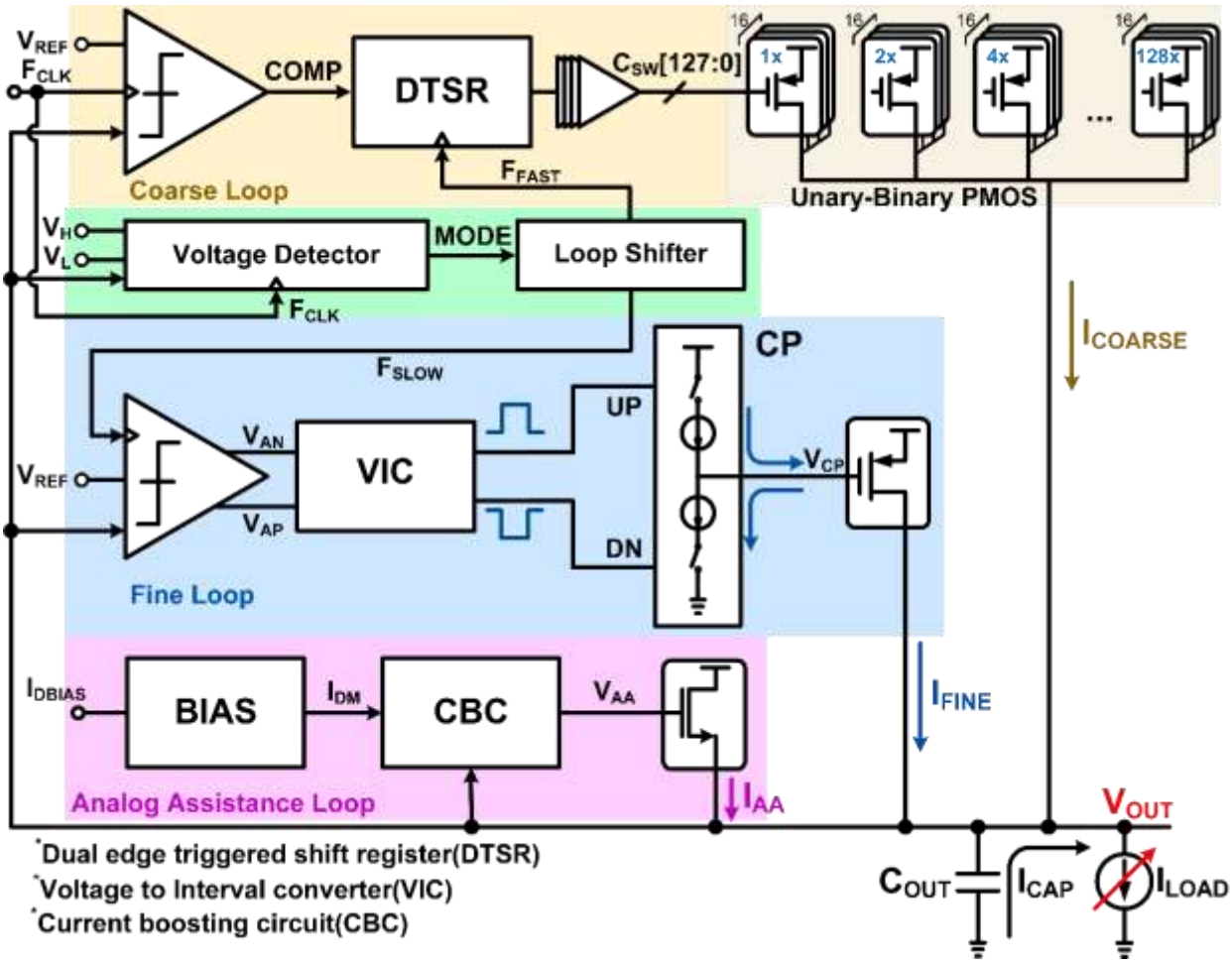


Figure 3.1: Detailed block diagram.

This tri-loop design is unique as it combines all three loops. The purpose of this innovative combination is to overcome the constraints that are inherent in conventional systems while simultaneously achieving maximum performance for both digital and analog loads. Fig 3.1 shows a detailed block diagram of the proposed ripple-less DLDO and Fig 3.2 shows its operational waveforms. The proposed DLDO includes three loops: two clock-operated loops (coarse and fine loops) and one clock-less analog-assisted (AA) loop. The proposed AA loop is implemented to supply an instant dynamic current (I_{AA}) to I_{LOAD} to effectively suppress voltage undershoots (ΔV_{OUT}) during I_{LOAD} transients.

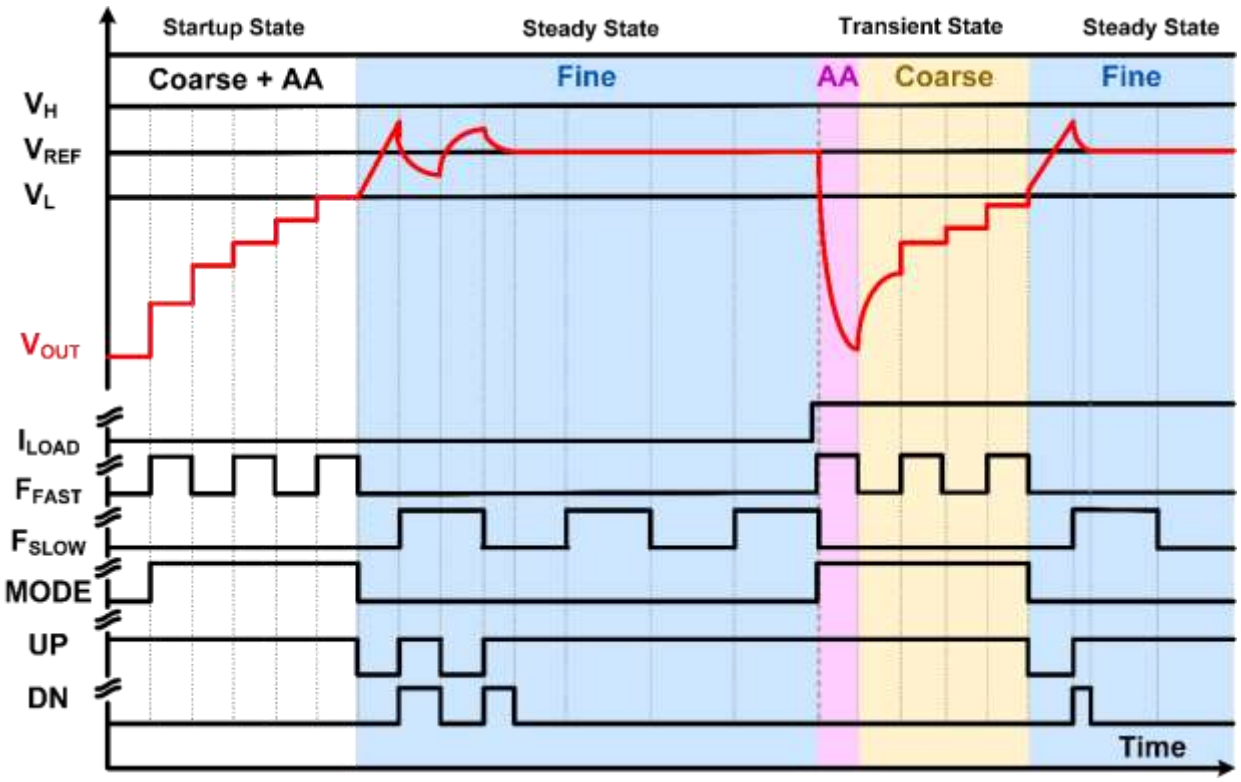


Figure 3.2: Overall operational waveforms over different states of the proposed DLDO.

3.2.1 Dynamic Latch Comparator

The proposed design makes use of a dynamic latch comparator as shown in Fig 3.3 to accomplish a speedy and efficient comparison of voltage while also reducing the amount of power that is consumed. The output voltage (V_{OUT}) is compared to a reference voltage (V_{REF}) for the comparator to perform its purpose. The comparator then generates a digital output that indicates whether the V_{OUT} is above or falling below the V_{REF}. This comparator is necessary for both the coarse and fine loops, as it enables the power transistors to be regulated in a timely and precise manner. The dynamic latch design decreases the amount of power consumed at the maximum supply voltage of 1.2 V from 13.91 µW to 1 µW when the circuit is idle, which makes it well-suited for applications that require low power consumption. Also, the comparator demonstrates a rapid reaction to differences in V_{OUT}, which makes it possible to make timely modifications in the control loops.

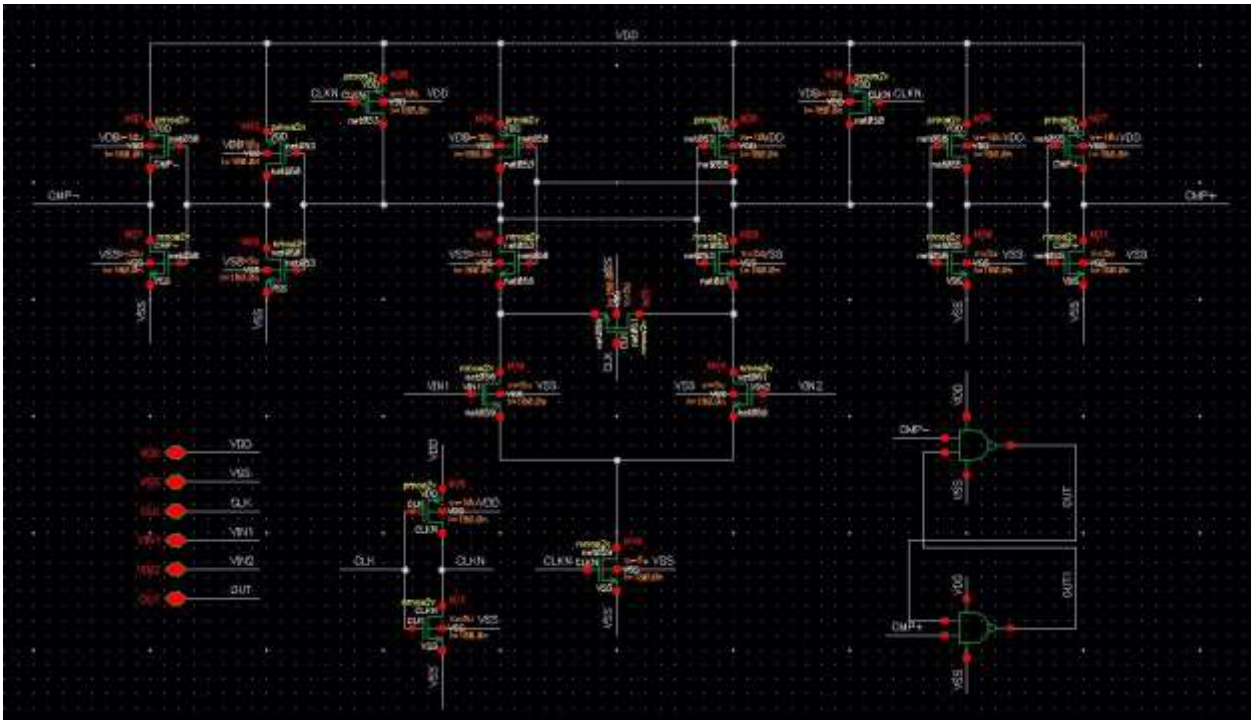
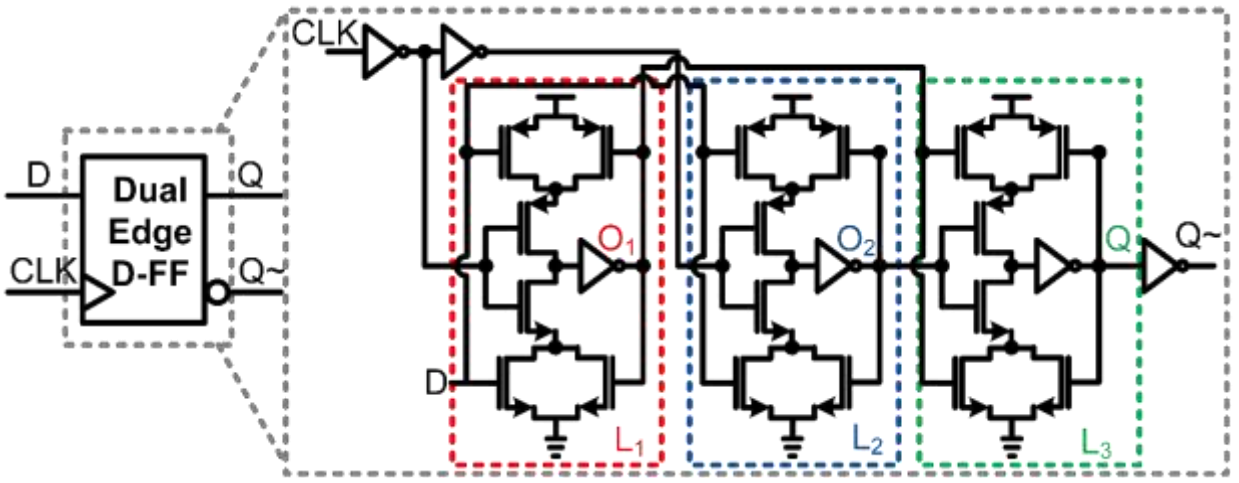


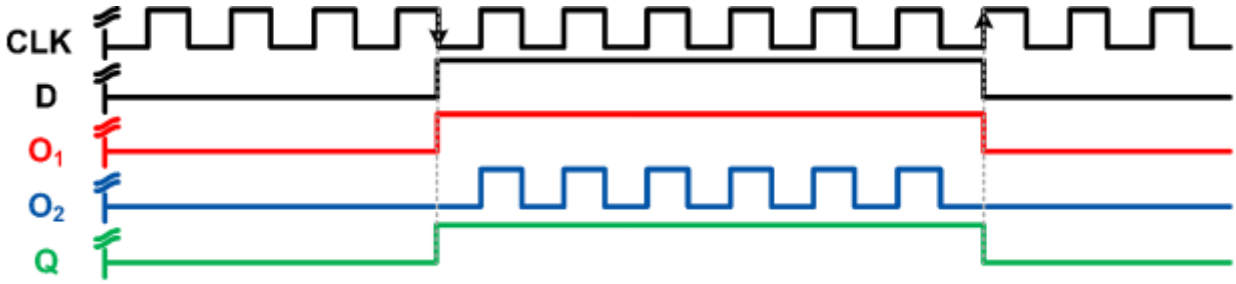
Figure 3.3: Dynamic Latch Comparator Schematic.

3.2.2 Dual Edge Triggered Flip Flop

One of the most important components of the digital coarse loop is the dual edge triggered flip-flop, also known as the DFF shown in Fig 3.4 and 3.5. This component makes it possible for the DLDO to operate at twice the speed of conventional designs having transient time of 590 µs. Through essentially doubling the frequency of operation without affecting the clock frequency, the DFF can improve the transient response of the coarse loop to 300 ns. Recording data on the rising and falling edges of the clock signal is the method that is utilized to accomplish this goal. The DFF makes it possible to make rapid adjustments to control signals, which is a vital component for swiftly reacting to strong load transients. The utilization of dual-edge operation helps to reduce the influence of clock jitter, which ultimately results in an improvement in the loop's overall stability. It consumes maximum power of 0.45 µW at supply voltage 1.2 V.



(a)



(b)

Figure 3.4: Dual Edge triggered Flip Flop (a) circuit diagram (b) operational waveforms

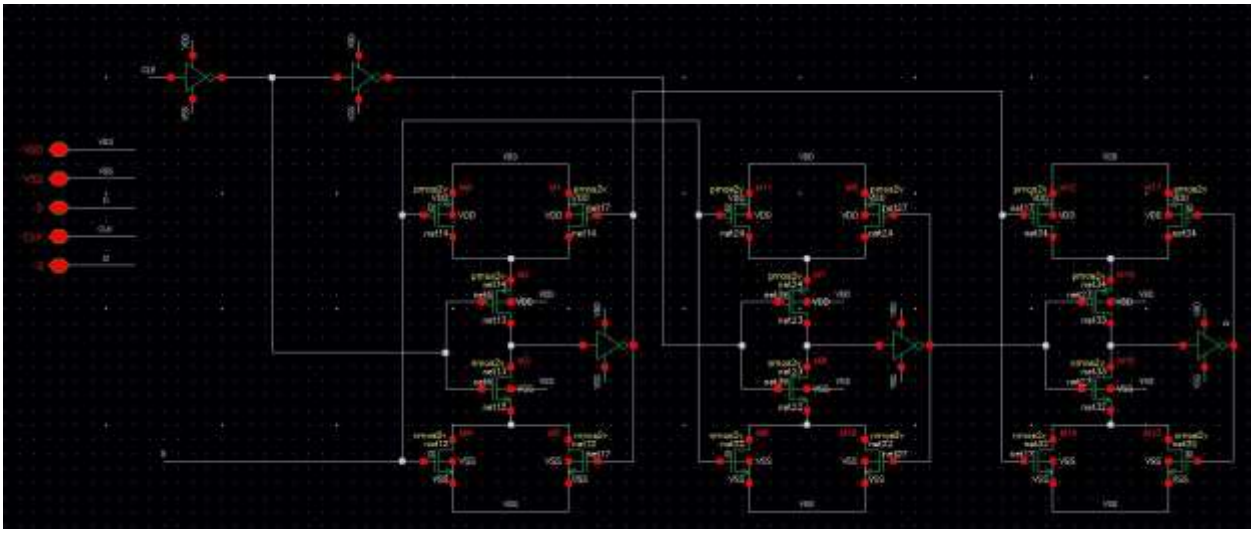
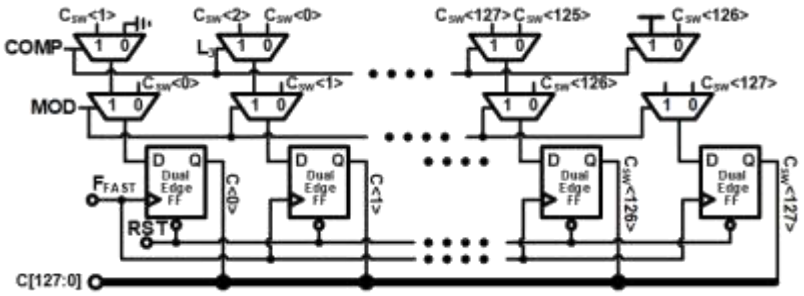


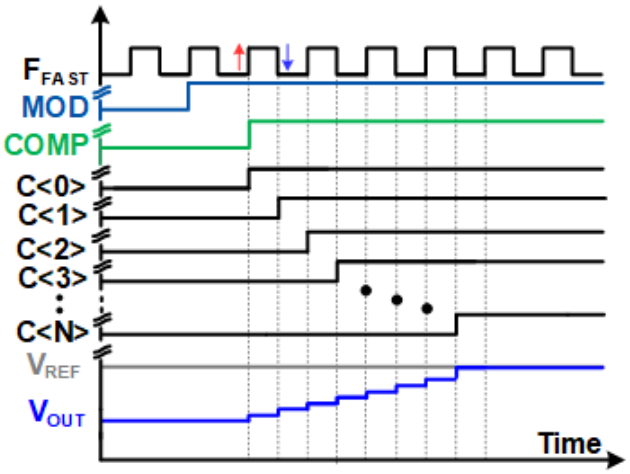
Figure 3.5: Dual Edge triggered Flip Flop Schematic.

3.2.3 Dual Edge Triggered Bi-Directional Shift Register

In the digital coarse loop, the DBSR shown in Fig 3.6, which is a dual edge triggered bi-directional shift register, serves as the mechanism that is responsible for providing central control. The quantity of operational power transistors is modulated by the system in accordance with the digital signal that is generated by the dynamic latch comparator. One of the capabilities of the DBSR is its ability to shift in both ways, either increasing or decreasing the number of active transistors. This is made possible by its bi-directional capacity. Having this feature allows for more precise control over V_{OUT} as well. Bi-Directional control enables the power transistor array to be manipulated in both the upward and downward directions, which makes it easier to determine the exact value of the voltage output (V_{OUT}). Moreover, the Dual-Edge Triggering technique enhances both the velocity and the reactivity of the system by identifying changes on both clock edges.



(a)



(b)

Figure 3.6: Dual Edge triggered Bidirectional shift register (a)circuit diagram (b) operational waveforms

3.2.4 Voltage to Interval Converter

One of the most important components of the charge-pump-based fine loop is the voltage-to-time converter. Also known as the VIC, it has the capability to convert the difference in voltage between V_{OUT} and V_{REF} into a time period that is responsible for regulating the duration of the charge-pump's operation. The use of this time-based control technique makes it possible to make precise adjustments to V_{OUT}, which ultimately leads to a reduction in V_{RIPP} to levels that are minimum. Fig. 3.7 and 3.8 shows the schematic and operational waveforms of the proposed fine loop. As shown in Fig. 3.7(a), the clocked comparator compares V_{REF} and V_{OUT} and generates OUT1 and OUT2. Both signals are then fed to the VIC which generates the proportional digital pulses of UP and DN.

These digital pulses serve as the current-sourcing and current-sinking signals into the CP, generating a modulated output voltage VCP. This voltage controls the gate voltage of NMOS power transistor. The operational waveforms of the fine loop are illustrated in Fig. 3.3(b). The key features are as follows:

- **Exceptional Accuracy**: This feature converts minute fluctuations in voltage into precise time periods, which enables the V_{OUT} to be meticulously regulated.
- **Integration with Charge Pump**: This feature enables a direct connection to be made with the charge pump, which in turn makes it possible to modulate the gate voltage of the power transistor. Moreover, because of this, it effectively improves the suppression of V_{RIPP}.

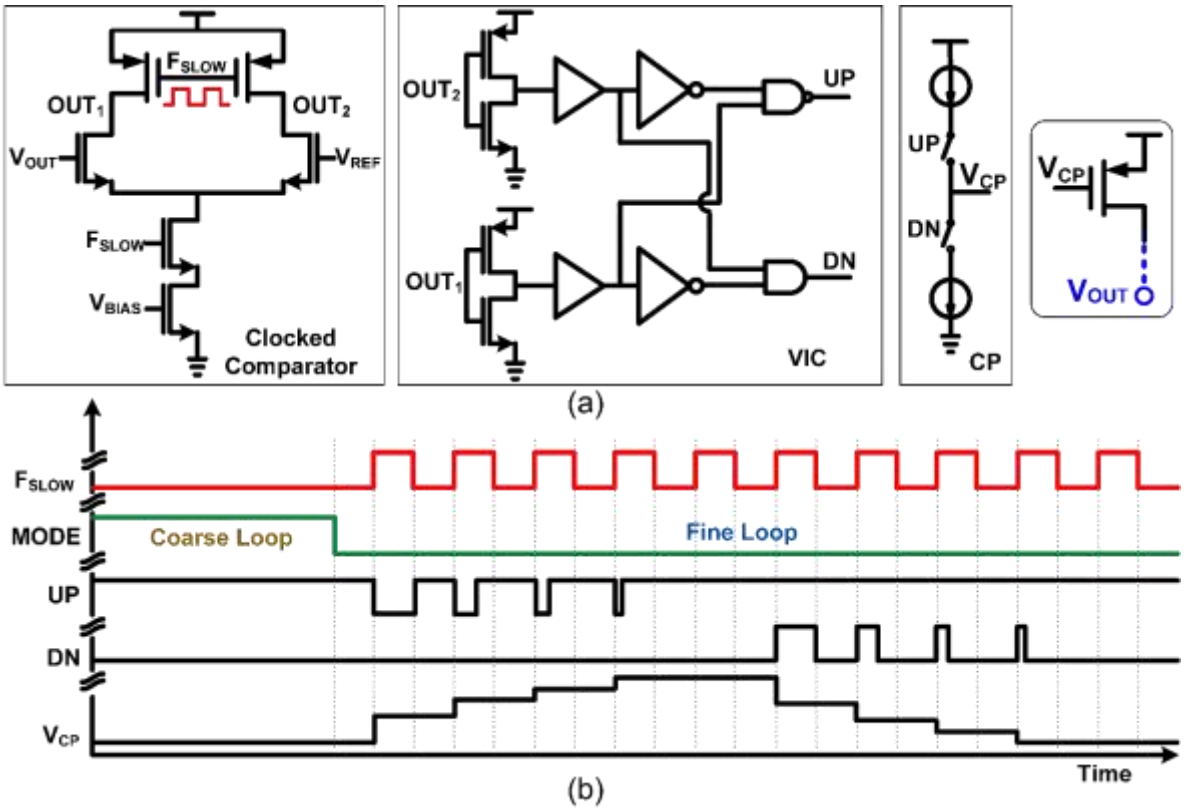


Figure 3.7: The proposed fine loop: (a) circuit diagram and (b) operational waveforms.

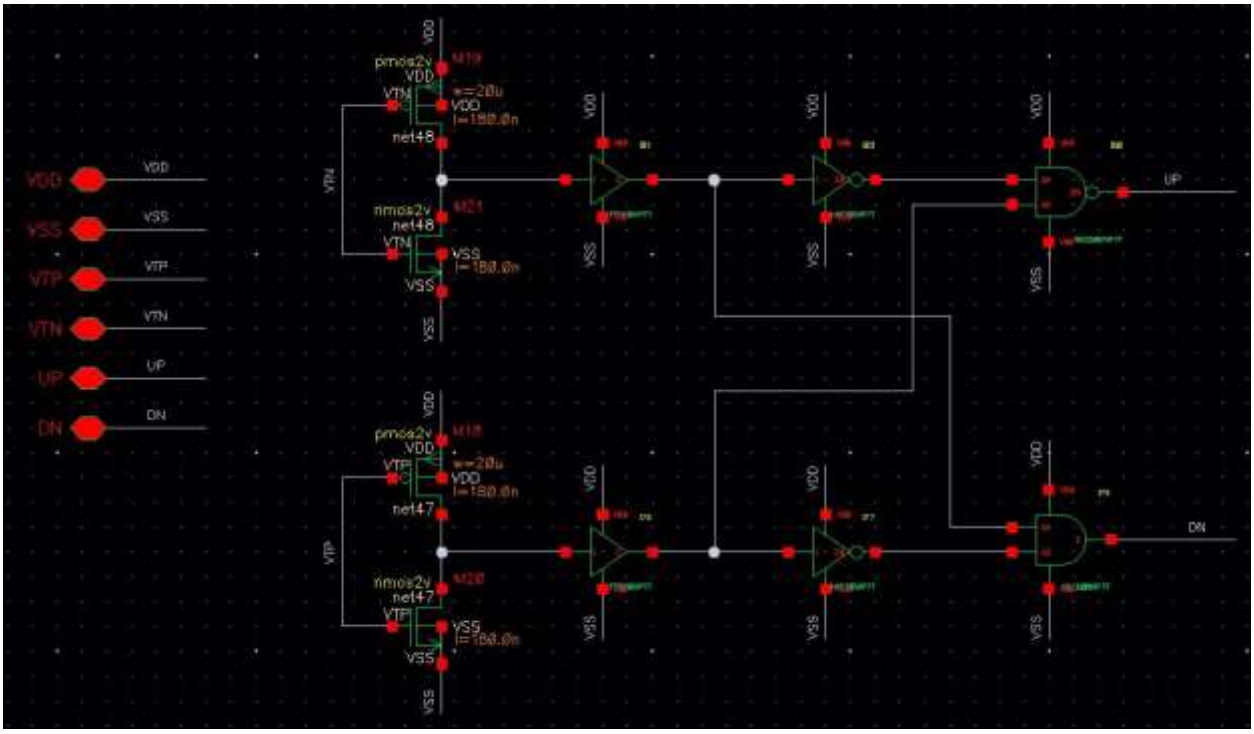


Figure 3.8: Designed schematic of Fine loop VIC.

3.2.5 Analog Assistance Loop

To efficiently reduce voltage undershoots (ΔV_{OUT}) and enhance transient response, the analog-assisted (AA) loop has been constructed with the particular purpose of rapidly implementing corrective steps during load transients. A current-boosting circuit (CBC) is a component of the AA loop, and it is connected to an NMOS power transistor. The implementation of this system allows for the rapid delivery of additional current in response to sudden changes in the load.

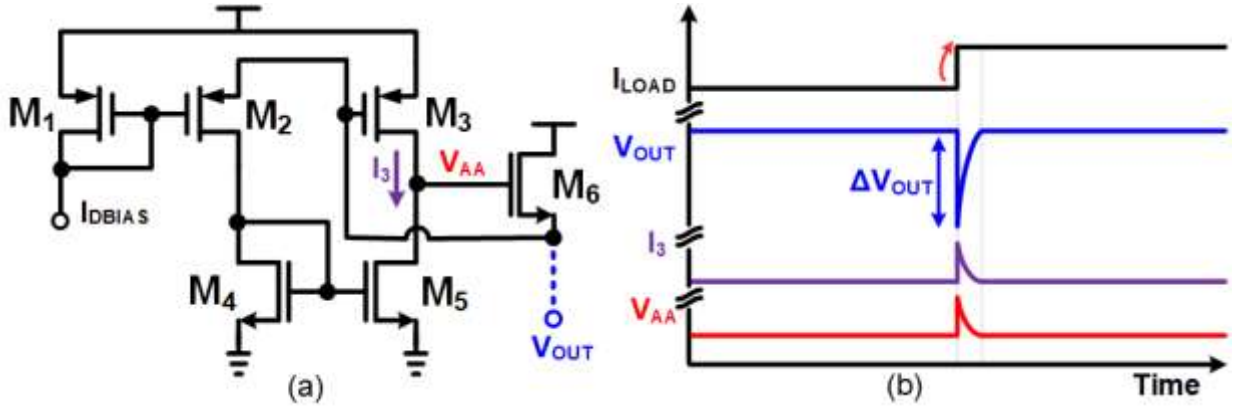


Figure 3.9: The proposed analog-assisted loop: (a) circuit diagram and (b) operational waveforms.

The proposed AA loop consists of a bias circuit, a current boosting circuit (CBC), and a MAA power transistor, as shown in Fig. 3.9(a) and its operational waveforms are shown in Figure 3.9(b). The AA loop can quickly respond to changes in load, hence reducing the voltage variance (ΔV_{OUT}) and ultimately improving stability. It has low power overhead during steady-state operation, which ensures that it has good overall efficiency.

3.2.6 Unary Binary Weighted Power Transistor Array

The unary-binary weighted power transistor array, as shown in Fig. 3.10 provides a mechanism that is both versatile and scalable for managing the voltage output (V_{OUT}). A combination of unary-weighted transistors, which are used for coarse control, and binary-weighted transistors, which are used for precision control, make up the array. With the help of this combination, the DLDO can attain an exceptionally high level of precision across a wide variety of output voltages. The principal traits of this one are:

- **Scalable Design**: The scalable design makes use of both unary and binary-weighted transistors to incorporate a diverse range of output voltages.
- **High Precision**: The enhanced accuracy feature allows for exact modulation of V_{OUT}, hence reducing V_{RIPP} and boosting regulatory precision.

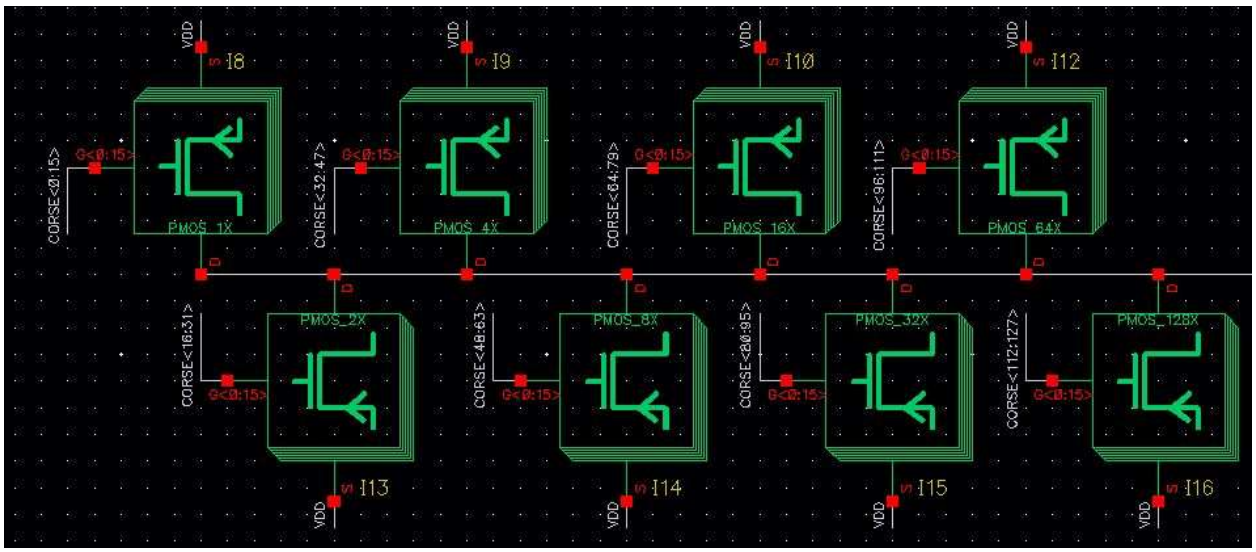


Figure 3.10: Unary Binary PMOS Array.

3.2.7 Built-in Load

The load is a crucial component of the DLDO design that is utilized for the purpose of testing and characterization. Through the simulation of a variety of load conditions, the performance of the DLDO is examined. This evaluation includes its transient response, V_{RIPP}, and PSR functions. With load simulation, it is possible to evaluate the performance of DLDO across a variety of load scenarios, which results in the collection of substantial data that may be used for optimization purposes. Integrated Design ensures that the inherent load does not interfere with the normal operation of the DLDO when it is subjected to conditions that are encountered in the real world.

Conventional systems often employ off-chip loads, which introduce supplementary clock delays due to the switching techniques required to activate and deactivate the load. To alleviate these delays and guarantee precise and fast measurements, we have engineered an on-chip load, as shown in Fig. 3.11. This architecture enables more efficient measurement operations free from such delays. Moreover, the majority of Low Dropout Regulators (LDOs) are specifically built for

on-chip loads, akin to the design of analogue or digital intellectual property (IP) blocks. Consequently, our design seeks to accurately simulate the operational conditions that these components would encounter in realistic applications, guaranteeing that the testing corresponds with real-world usage scenarios.

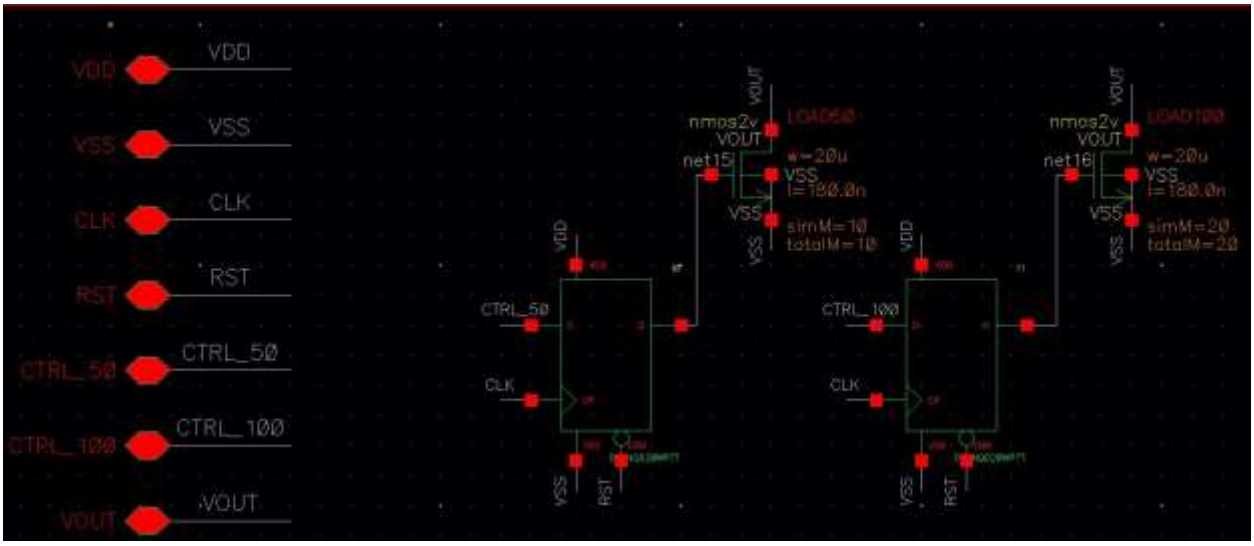


Figure 3.11: Built-in On-Chip Load.

3.2.8 Top level Schematic

All the components that were discussed before are included in a single design that is represented by the principal schematic of the proposed tri-loop DLDO structure as shown in Fig. 3.12 and 3.13. While the figure highlights the unique contributions that each loop makes to the overall performance, it also displays the connections that exist between the digital coarse loop, the charge-pump-based fine loop, and the analog-assisted loop.

- **Integrated Control Loop**: Refers to the utilization of digital, analog, and hybrid control systems to achieve the maximum possible degree of performance.
- **Comprehensive Regulation**: Provides a rapid reaction to abrupt changes, little voltage ripple and noise, better power supply rejection, and low voltage drop-out. As a result of these qualities, it is suitable for a wide range of different applications

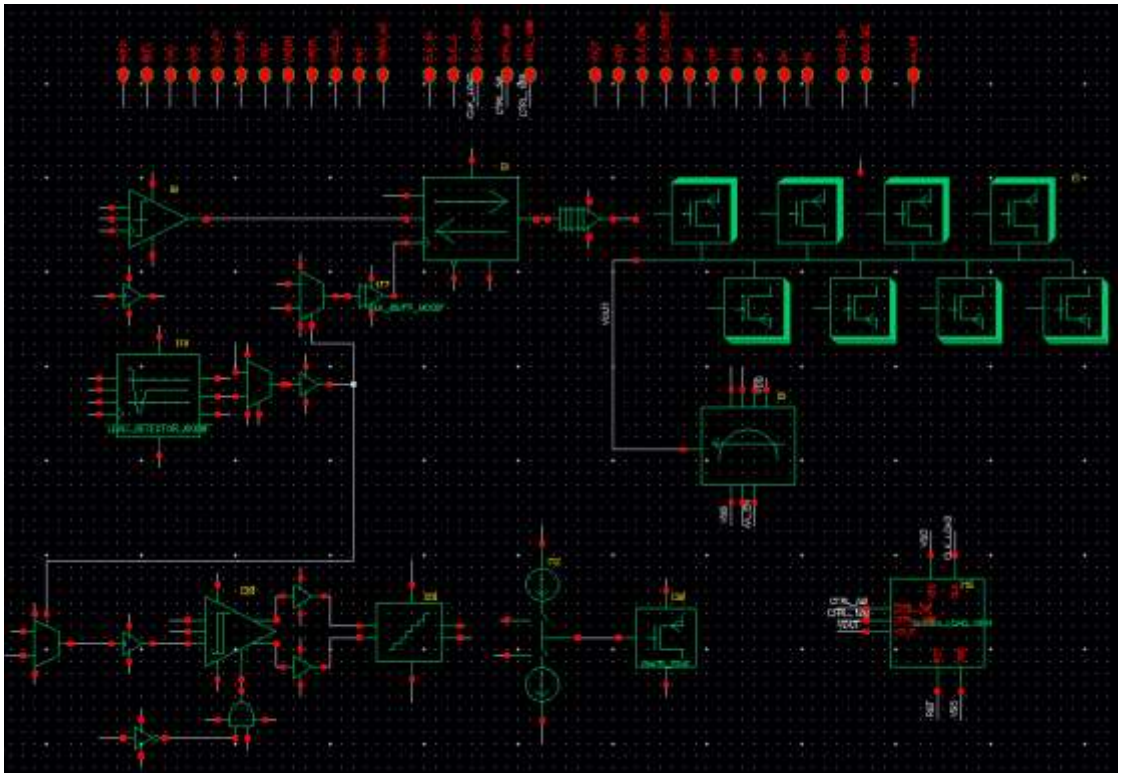


Figure 3.13: Top Level Schematic Design.

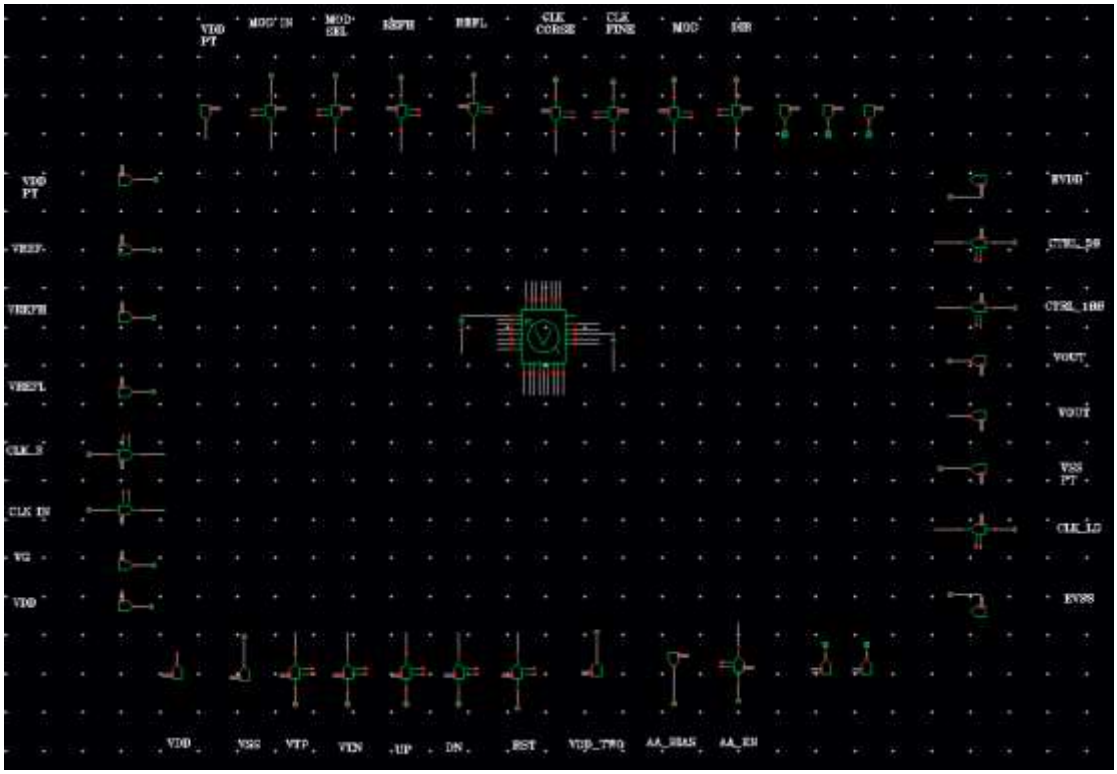


Figure 3.12: Top Level Schematic Design with pads.

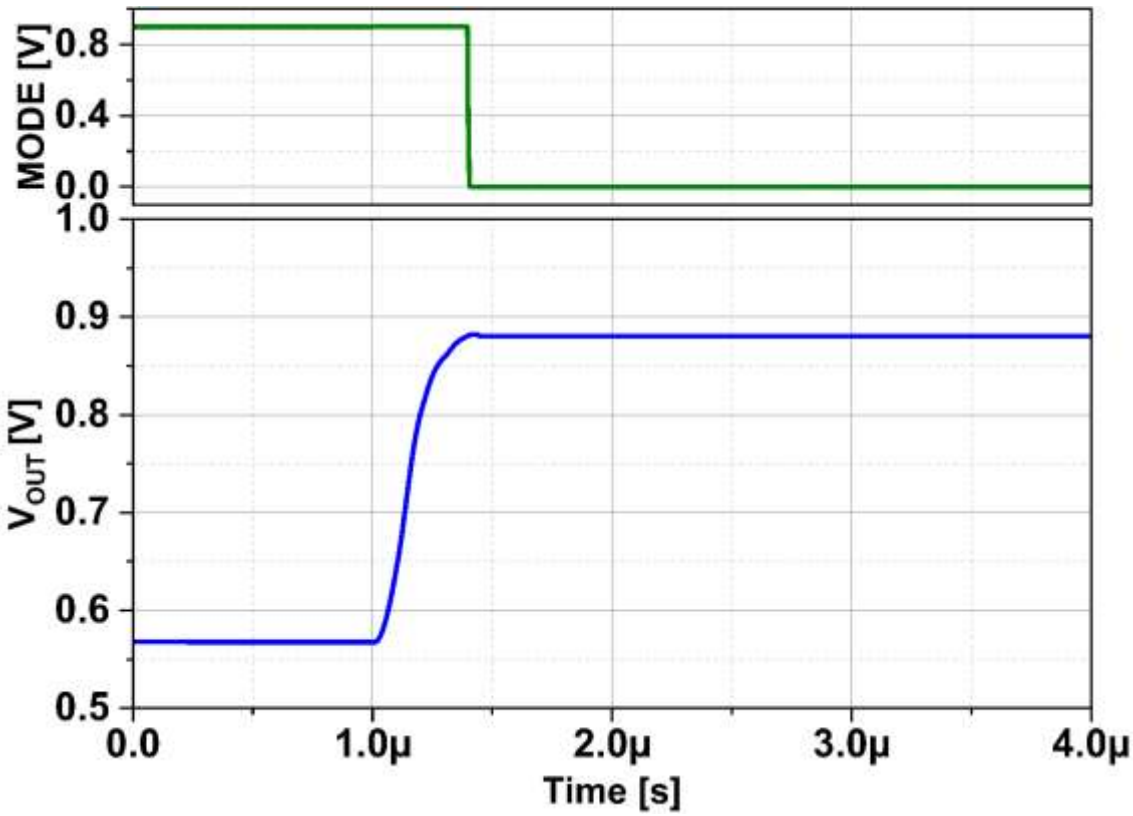


Figure 3.14: Startup response of LDO.

For demonstrating that the tri-loop DLDO design, exhaustive simulations were carried out using TSMC 180-nm CMOS process. The results of the simulation show that traditional DLDO systems are much inferior to the simulated ones in terms of V_{RIPP}, PSR, transient responsiveness, and power efficiency.

3.3 Simulated Results

3.3.1 Startup Response

A simulated startup response of the proposed DLDO was assessed at V_{DD} = 0.9 V, V_{OUT} = 0.88 V, and I_{LOAD} = 1 mA to evaluate the effectiveness of the DLDO in swiftly attaining the target output voltage. Within less than 300 microseconds, the DLDO was able to achieve the target V_{OUT} level, which is evidence of its rapid transient responsiveness as shown in Fig. 3.14. The control made the transition from the rough loop to the exact loop, as indicated by the MODE signal, once

it had reached the desired voltage. This was done to guarantee that the V_{RIPP} would be low in a steady state.

3.3.2 Steady-state Analysis and Output Ripples

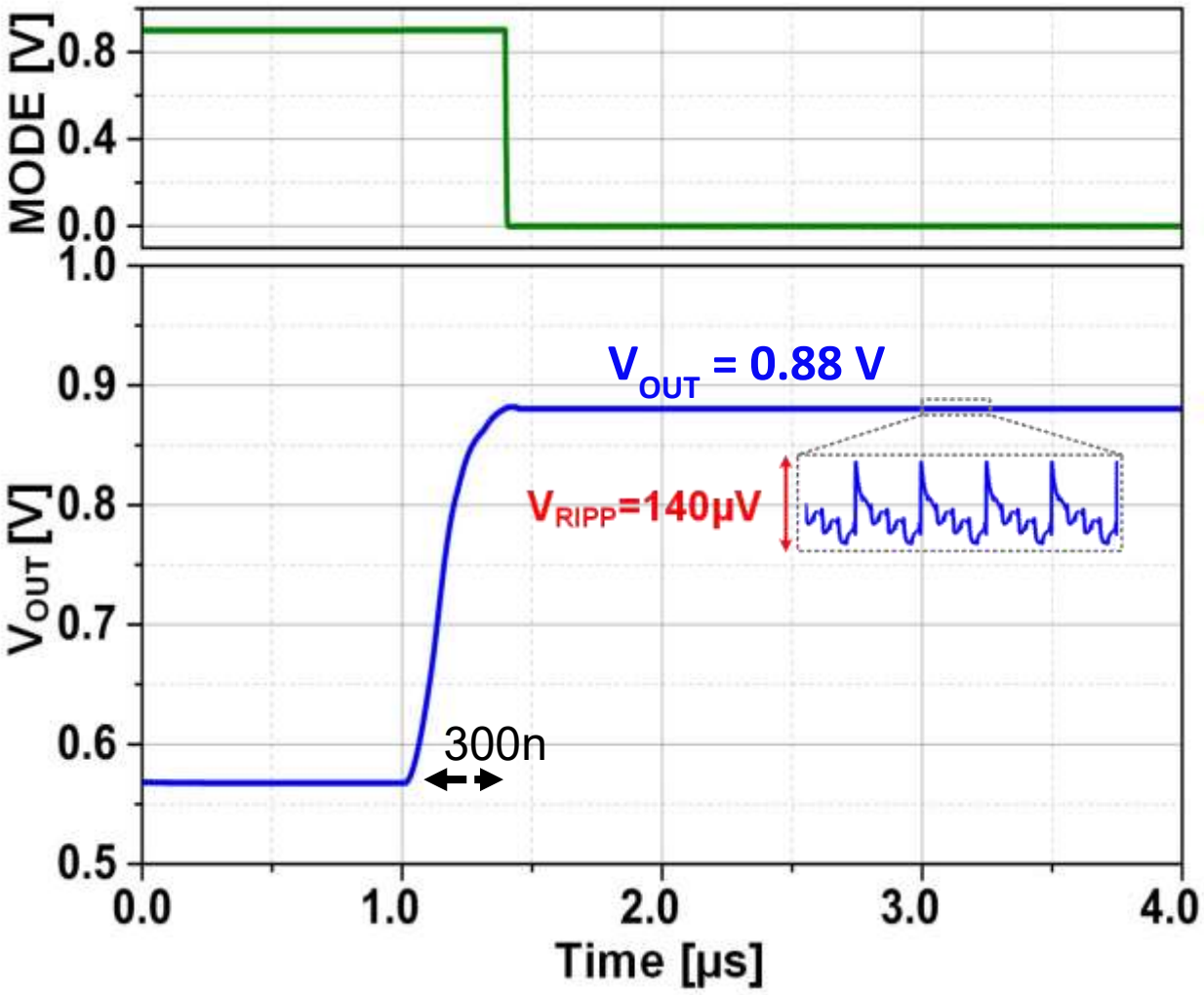


Figure 3.15: Steady-state Analysis and Output Ripples.

In the steady-state investigation, it was established that the recommended DLDO was able to obtain a V_{RIPP} that was less than 140 µV, which indicates that it is suitable for analog loads that are sensitive to noise. The charge-pump-based management of the fine loop, in conjunction with the high-precision voltage-to-time converter, was able to successfully attenuate fluctuations in the output voltage.

To test whether the proposed DLDO is capable of fast achieving the required output voltage (V_{OUT}) from an initial condition, the startup response of the device was evaluated. It is

demonstrated in Fig. 3.15 and 3.16 of the study that the DLDO can attain the target V_{OUT} of 0.88 V during a time frame of 300 ns after the power is supplied (with V_{DD} = 0.9 V and I_{LOAD} = 1 mA). The digital coarse loop is responsible for the rapid beginning time. This loop immediately adjusts the amount of active power transistors to get the output voltage (V_{OUT}) closer to the reference value (V_{REF}).

- Rapid Voltage Regulation: The coarse loop is activated in a short amount of time, which enables the DLDO to stabilize the voltage output (V_{OUT}) in less than 300 nanoseconds. This is a significant improvement over the conventional systems.
- The transition to the fine loop occurs when the voltage output (V_{OUT}) is relatively close to the voltage equal to the output voltage (V_{REF}). The fine loop is based on a charge pump. When the steady state is maintained, this guarantees that the V_{RIPP} is kept to a minimum.

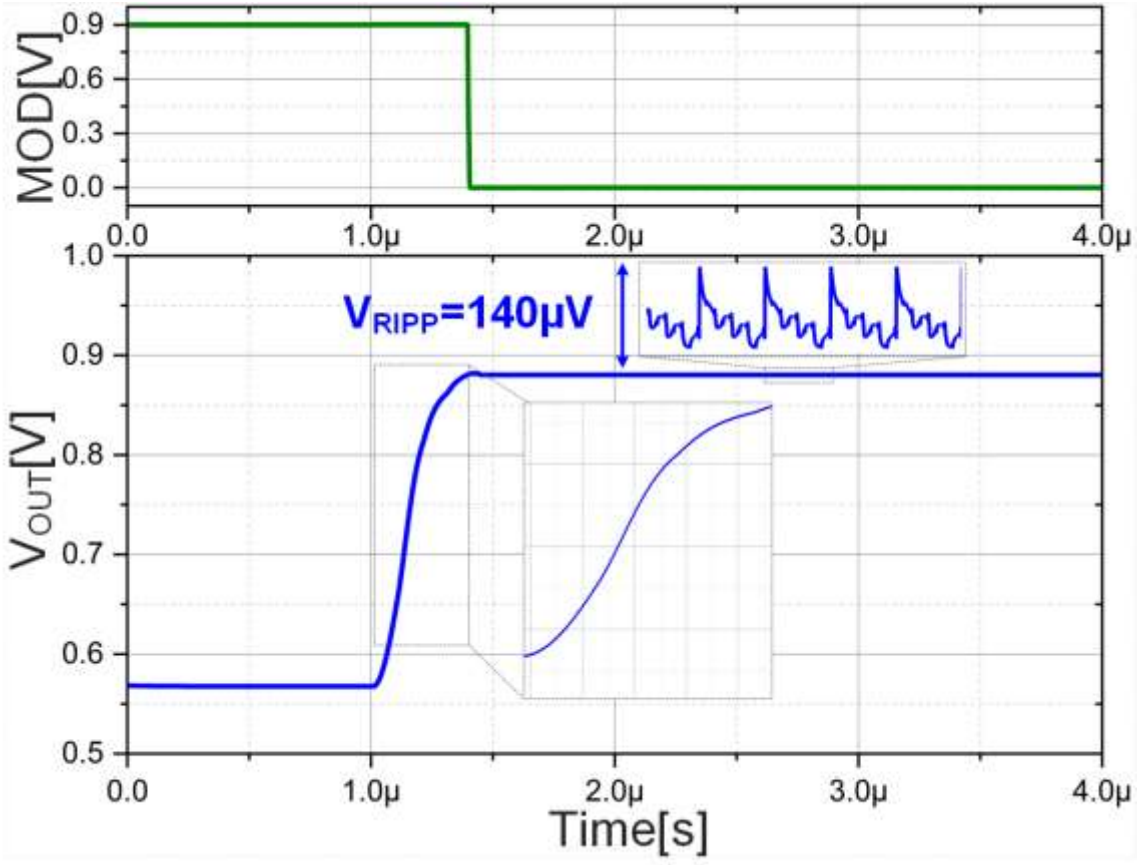


Figure 3.16: Start-up response of the proposed DLDO at V_{DD} = 0.9 V, V_{OUT} = 0.88 V, and I_{LOAD} = 1 mA.

3.3.3 Transient Behavior

To evaluate the proposed DLDO's capability to handle rapid load variations, the transient response of the device was simulated under a variety of load conditions. Due to the synergistic operation of the coarse loop and the analog-assisted loop, the data indicated that the DLDO was able to handle considerable fluctuations in load with minimal voltage deviation. This was accomplished with efficiency. In response to changes in load, the TREC was significantly reduced, and the output voltage quickly returned to its original level.

The transient response of the DLDO was evaluated by putting it through a series of sudden changes in load current (I_{LOAD}) to ascertain whether it can maintain a constant output voltage in the face of dynamic conditions as shown in Fig 3.17.

The findings, which are illustrated in Figure 3.18, provide evidence that the proposed DLDO effectively manages significant load changes while simultaneously decreasing the occurrence of voltage undershoot (ΔV_{OUT}).

1. **Load Transient at V_{OUT} = 0.88 V, I_{LOAD} = 1 mA to 75 mA:** When a considerable load step (from 1 mA to 75 mA) is provided, the DLDO encounters a voltage undershoot of 205 mV. This occurs when the load step is applied during the load transient. Despite this, the undershoot is quickly corrected within 400 nanoseconds because of the combined effect of the coarse loop and the analog-assisted loop coming together.
2. **Load Transient without AA Loop:** In a test that compares the performance with and without the AA loop, the voltage undershoot is significantly increased when the AA loop is absent. This is visible in the results of the test. This exemplifies the significant part that the AA loop plays in improving the performance throughout transients.

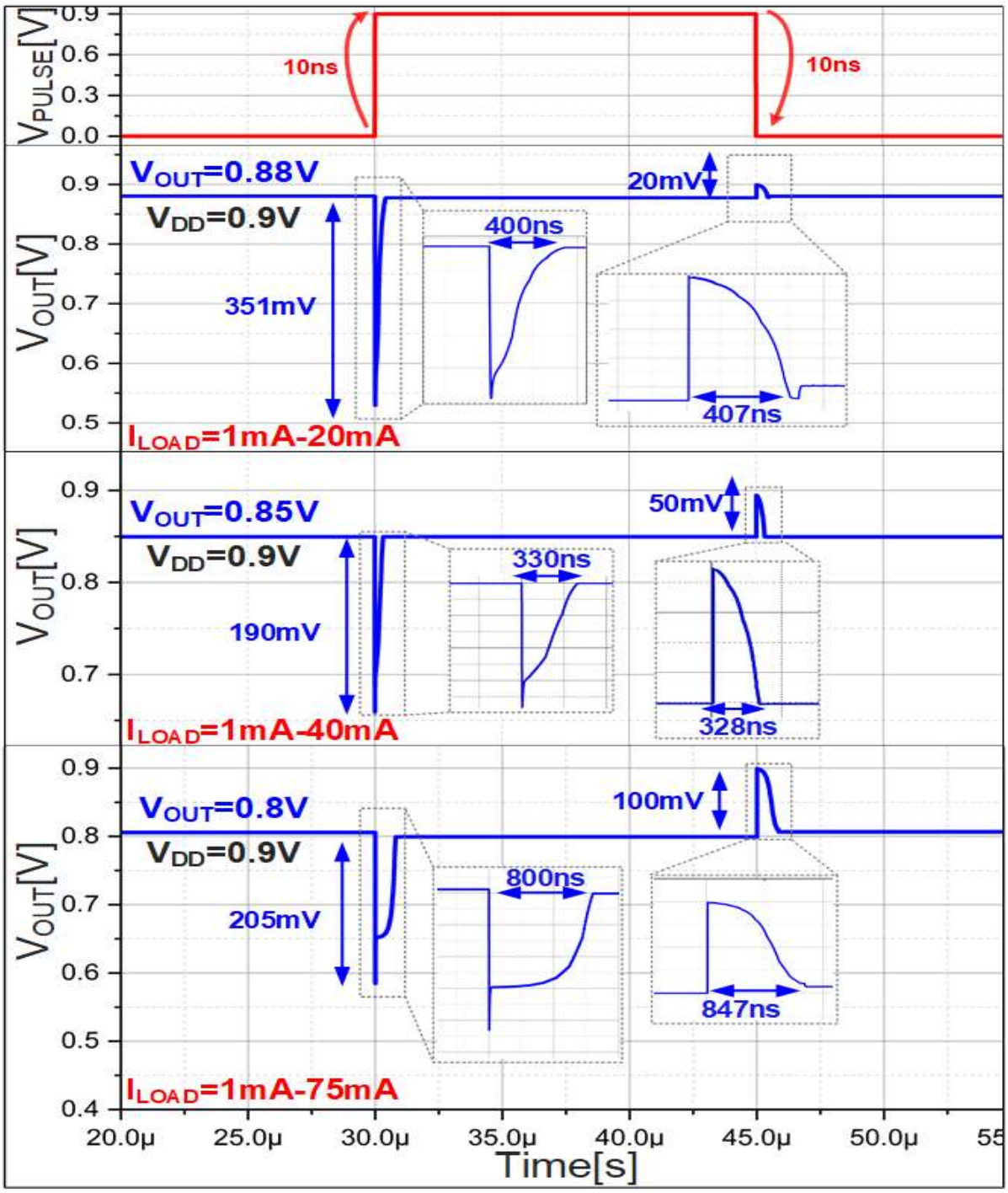


Figure 3.17: Load transient response comparison of the proposed DLDO at different load conditions and V_{REF}.

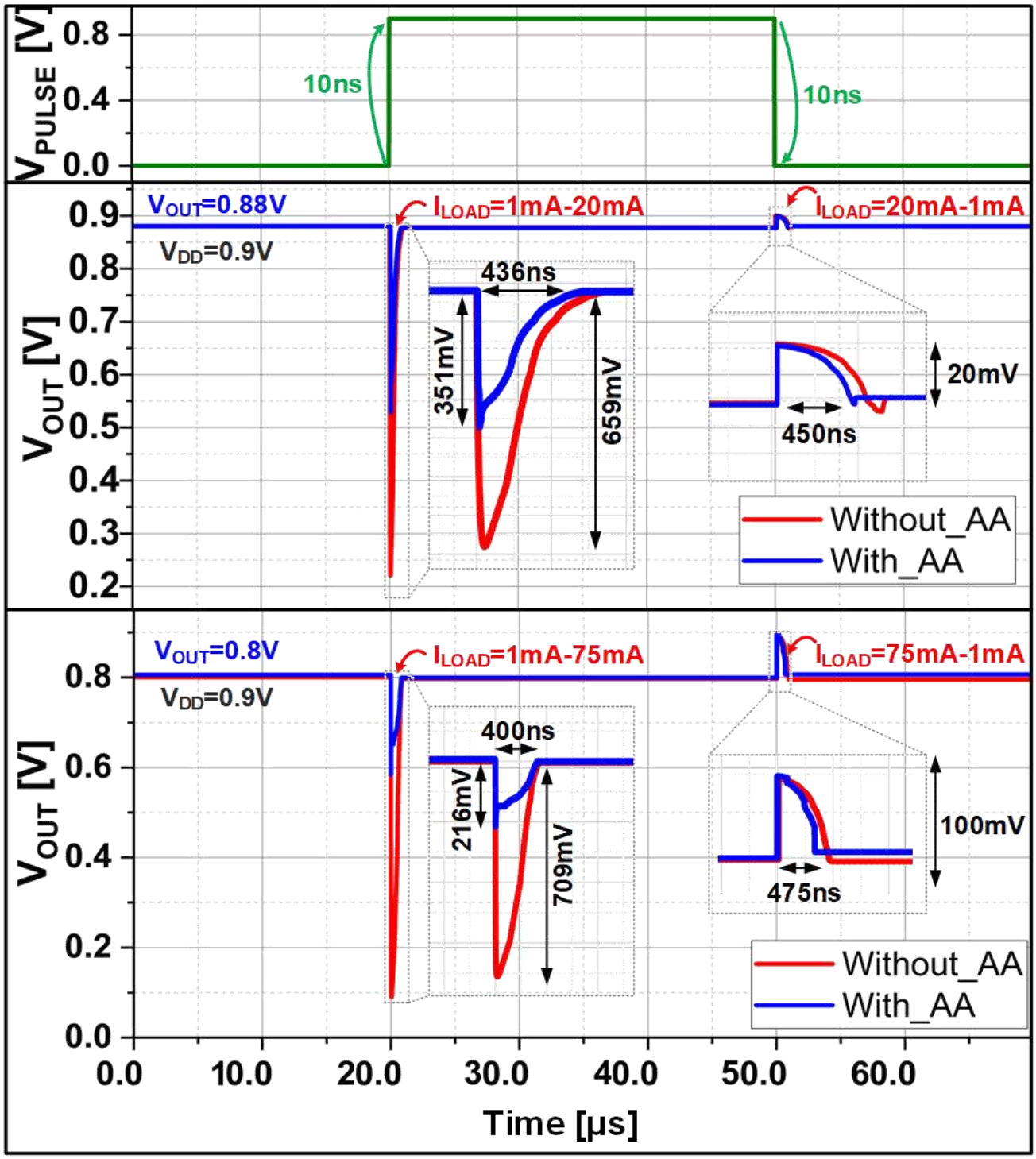


Figure 3.18: Load transient response comparison of the proposed DLDO with and without AA-loop at V_{DD} = 0.9 V for two different I_{LOAD} and V_{OUT} conditions.

3.3.4 Load and Line Regulation of Proposed Design

It was determined how well the suggested DLDO performed by simulating the output voltage while simultaneously modifying the load currents and input voltages. This was done to test the load and line regulation capabilities of the DLDO. Calculated as

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \quad \ldots(1)$$

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \quad \ldots(2)$$

A load regulation of 0.081 mV/mA and a line regulation of 8 mV/V were demonstrated by the DLDO as shown in Fig 3.19, which indicates that it possesses excellent stability and that it is resilient to variations in both the load voltage and the supply voltage.

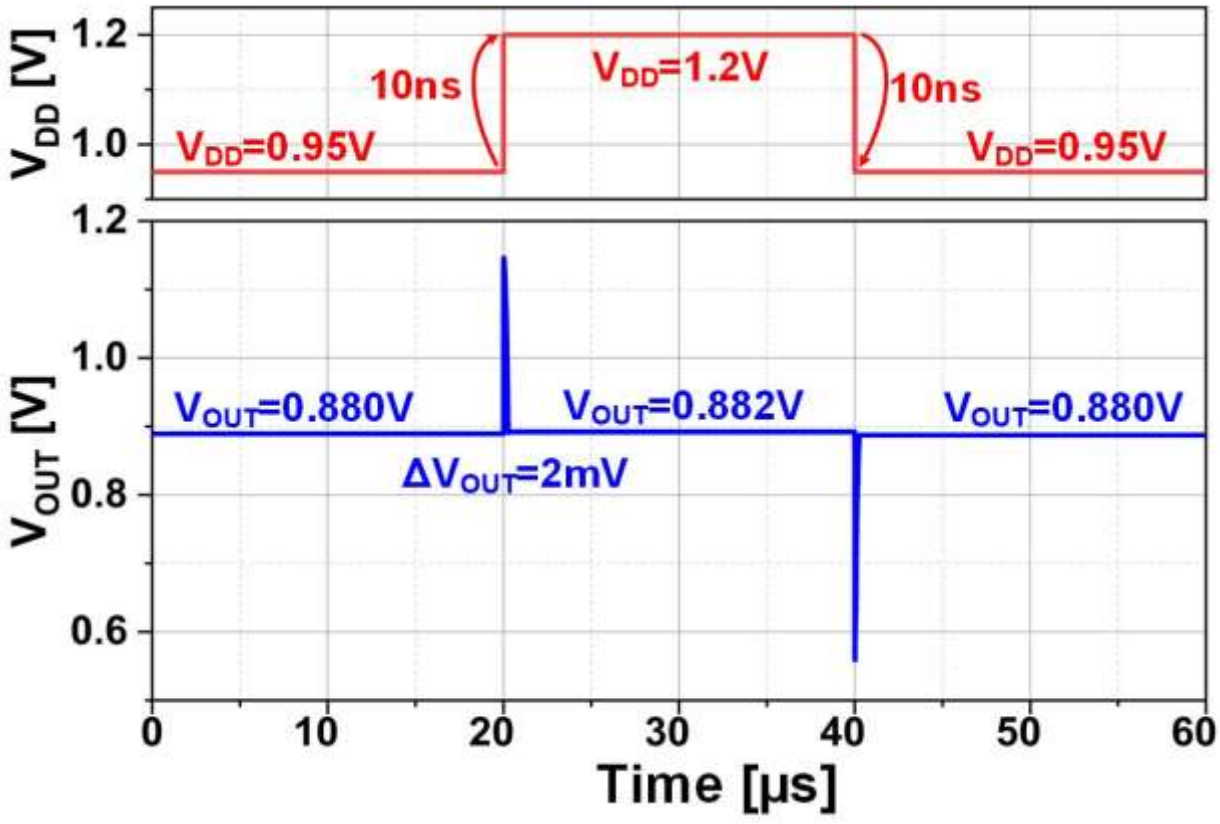


Figure 3.19: Load Regulation of 0.081 mV/mA at V_{DD} = 0.95 to 1.2 V with edge time of 10 ns.

3.3.5 Power Supply Rejection Ratio

To test the proposed DLDO's ability to suppress supply noise, the Power Supply Rejection (PSR) was simulated across a wide range of noise frequencies from different frequencies. A Power Supply Rejection (PSR) of -30 dB was demonstrated by the DLDO at a noise frequency of 1 kHz as shown in Fig 3.20. This demonstrates that the DLDO is capable of successfully reducing noise by coupling from the power supply (V_{DD}) to the output (V_{OUT}).

$$\text{PSRR (dB)} = 20\log\left(\frac{\Delta V_{IN}}{\Delta V_{OUT}}\right) \quad \ldots(3)$$

$$\text{PSR}\left(\frac{V}{V}\right) = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \quad \ldots(4)$$

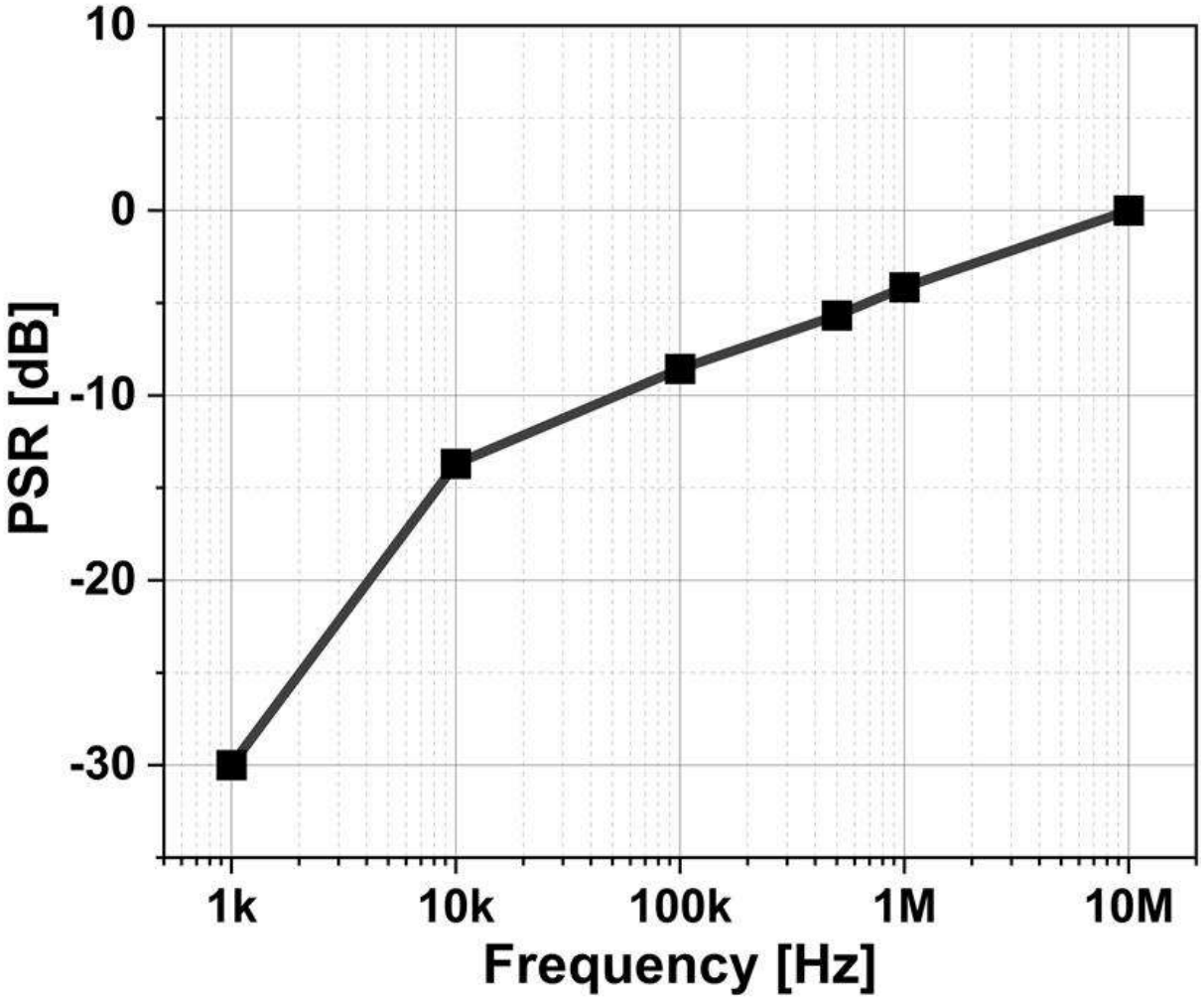


Figure 3.20: PSR performance of the proposed DLDO at V_{DD} = 0.9 V, V_{OUT} = 0.88 V, and I_{LOAD} = 1 mA.

3.3.6 Current and Power Efficiency

The DLDO design achieved a peak current efficiency of 99.93%, while simultaneously using a maximum quiescent current (I_Q) of 47 µA. The power efficiency of this device is improved by its low dropout voltage (V_{DO}) of 20 millivolts, which makes it suitable for applications that require little power.

$$\text{Efficiency} = \frac{I_{OUT}}{(I_{OUT} + I_Q)} \times \frac{V_{OUT}}{V_{IN}} \times 100\% \quad \ldots(5)$$

For determining the power efficiency of the DLDO, the input and output currents were measured under a variety of load conditions. A maximum current efficiency of 99.93% was achieved by the DLDO, which was followed by a peak quiescent current (I_Q) of 47 µA.

The DLDO's dropout voltage (V_{DO}) of 20 mV, which is incredibly low, and its I_Q, which is minimal, considerably enhances power efficiency, making it a good choice for applications that require low power. Efficiency remains consistently high across a large range of load currents, ranging from 1 mA to 75 mA, which demonstrates DLDO's appropriateness for handling dynamic loads. This attribute is referred to as "uniform efficiency across loads".

3.3.7 Figure of Merit Calculations

The figure of merit (FOM) of the recommended DLDO was determined to evaluate its performance in comparison to designs that are state-of-the-art. When compared to conventional designs, the figure of merit (FOM), which is determined by multiplying the product of $\frac{C_{out} \times \Delta V_{out} \times I_Q}{\Delta I_{load}}$ displayed a significantly lower value. It may be deduced from this that the system's performance is superior in terms of its efficiency, its ability to suppress ripples, and its response to temporary fluctuations.

$$\text{FOM (s)} = C_{TOTAL} \times \Delta V_{OUT} \times \frac{I_Q}{I_{Lmax^2}} \quad \ldots(6)$$

The figure of merit (FOM) of the recommended DLDO was determined to evaluate its performance in comparison to designs that are state-of-the-art. The figure of merit (FOM), which is produced by dividing the product of $\frac{C_{out} \times \Delta V_{out} \times I_Q}{\Delta I_{load}}$, was found to be 0.55 ps. This number is significantly lower than the figure of merit (FOM) that is calculated for standard DLDO systems.

Parameters	This Work	[6]	[13]	[14]	[16]
Process [nm]	180	110	65	130	180
Type	Digital	Digital	Digital	Hybrid	Hybrid
V_{DD} [V]	0.9 – 1.8	0.8-1.2	0.5-1	0.6,1.1-1.2	1.43 – 2.0
V_{OUT} [V]	0.88 – 1.78	0.7-1.1	0.45-0.95	0.5-0.55, 0.8-1.1	1.0 – 1.57
V_{DO} [mV]	20	100	50	100	430
I_{LOAD}[mA]	1-75	2.5-50	0.07-5.6	0.03-12	2-100
C_{OUT} [nF]	0.190	40	100	0.5	Cap-free
V_{RIPP} [mV]	0.14	3	N/A	N/A	2
PSR [dB]	-30	N/A	N/A	-12	-50
ΔV_{OUT}[mV]@ΔI_{LOAD}[mA]	205@40	360@47.5	49.5@2.3	240@10.3	421@80
Load Reg. [mV/mA]	0.081	0.422	N/A	<2.67@1V	0.01
I_Q [µA]	47	188-197	18.1	163.2	1000
Current Efficiency [%]	99.93	92.9-99.6	99.7	98.5(R*),98.64(Linear)	99.11
Power Efficiency [%]	93.38	81.38[1]	71.53[1]	12.93[1]	46.62[1]
FOM [ps][1]	0.55	1.26	17	166(R*),244.8(Linear)	N/A
Area [mm^2]	0.253	0.022	0.034	0.0818	0.697

FOM = $(C_{OUT} \times \Delta V_{OUT}) \times (I_Q)/(\Delta I_{LOAD})^2$, *R=Switch mode controller , N/A = Not Addressed

[1]Estimated from the values

Figure 3.21: Performance summary and comparison with state-of-the-art LDOs.

A performance summary of the proposed work and comparison with state-of-the-art DLDOs are shown in Figure 4.6. The low FOM number illustrates that the proposed DLDO has great efficiency, ripple suppression, and transient response, which makes it a good option for modern System-on-Chip (SoC) applications. Because of this, the FOM value is superior.

3.4 Layout Design

The layout of the proposed DLDO design was done using the TSMC 180-nm transistor and other component library, adopting the best layout practices.

3.4.1 Layout Techniques

For minimizing unnecessary capacitance and resistance, reducing interference between signals, and ensuring correct matching of critical components, advanced layout techniques were utilized. To enhance both performance and stability, many techniques were utilized, including the common-centroid arrangement, dummy devices, and guard rings.

3.4.2 Sub-Block Layout

The configuration of each individual sub-block, such as the comparator, VTC, DEBSR, and AA loop as shown in Fig 3.22,3.23,3.24 and 3.25, was carefully created to minimize the amount of space that was occupied while also ensuring that the performance was of the highest possible standard. While the VTC arrangement was specifically designed to ensure high precision in voltage-to-time conversion, the dynamic latch comparator was tuned for speed and low power consumption and these considerations were taken into consideration during the design process.

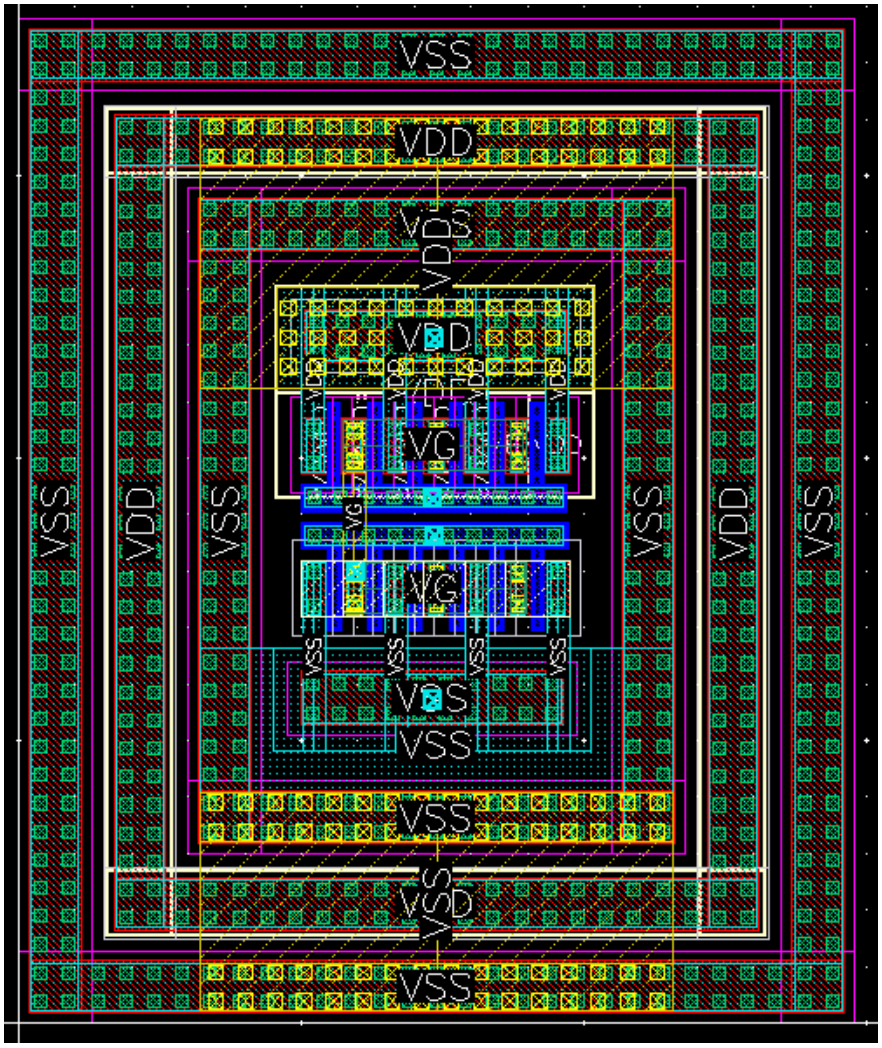


Figure 3.22: Layout of Analog assisted Loop.

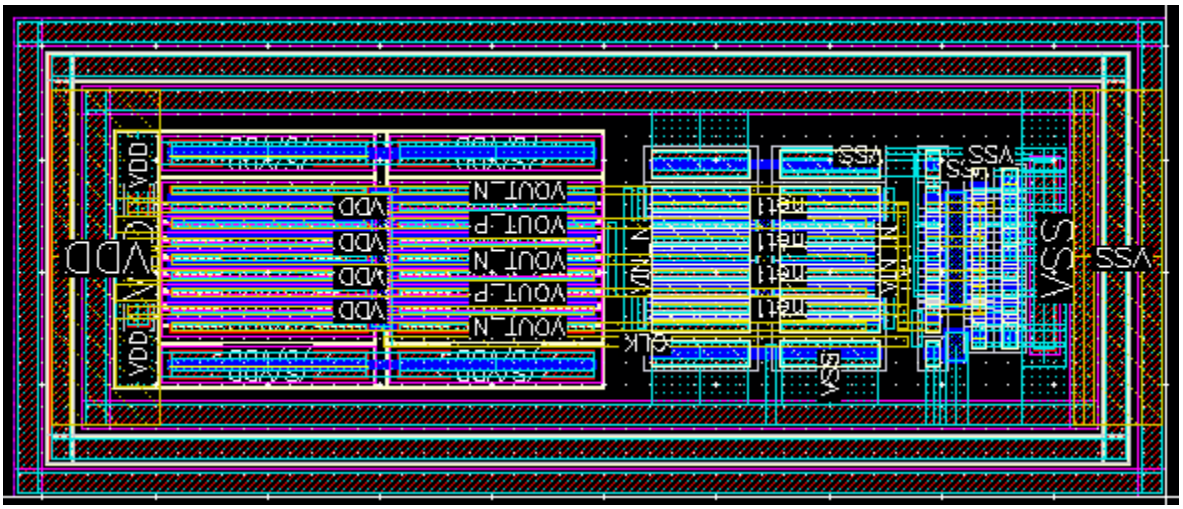


Figure 3.23: Layout of Charge Pump.

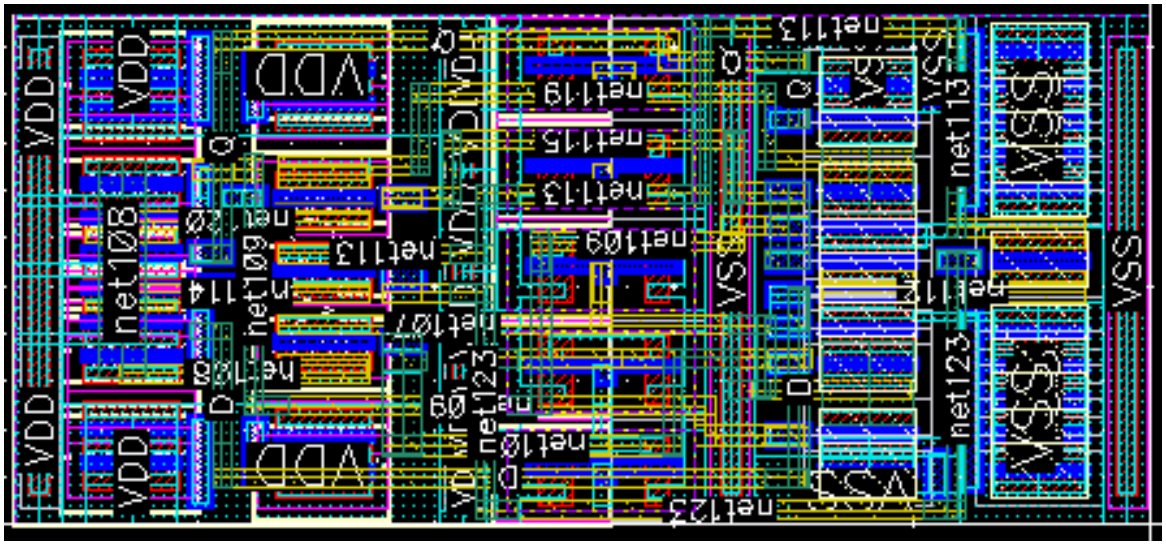


Figure 3.24: Layout of VDTC.

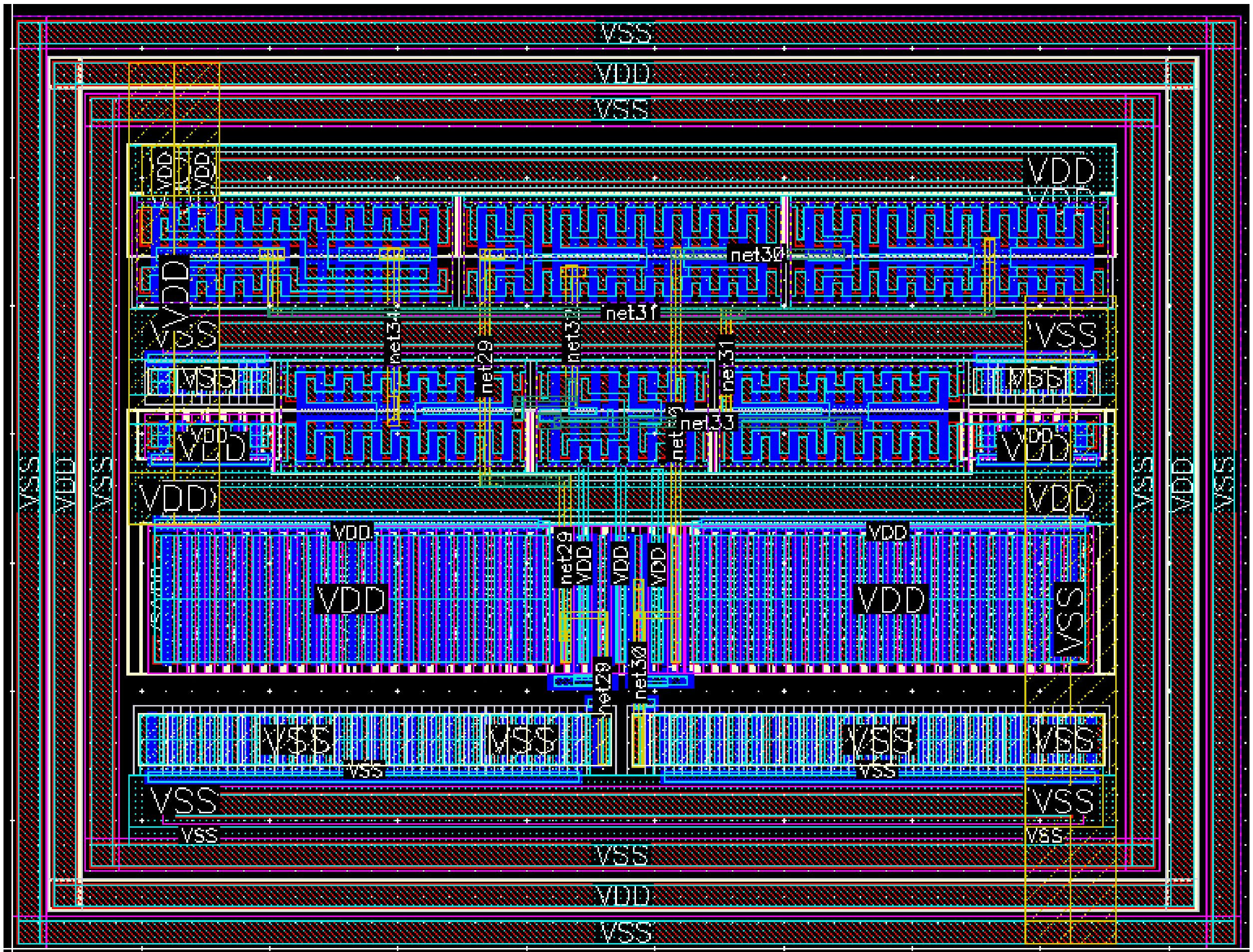


Figure 3.25: Layout of Comparator Block.

3.4.3 Top Level Layout Design

A compact top-level layout having a functional area of 0.253 square millimeters including all the subordinate components under consideration was done. The layout was designed in such a way that it minimized the impact of parasitic elements in the routing and optimized the arrangement of components to reduce interference and increase the overall performance.

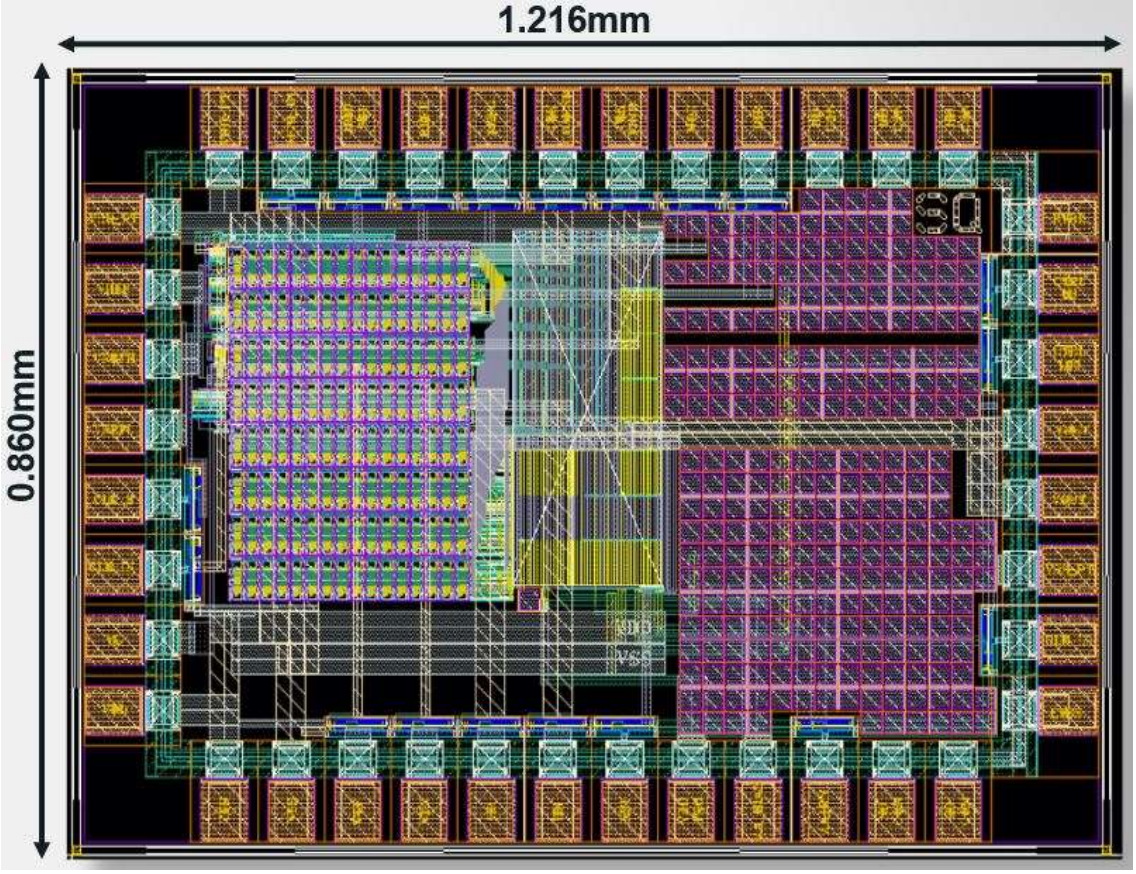


Figure 3.26: Top Level Layout with pads and seal ring.

3.5 Conclusion

The tri-loop DLDO design represents a significant step forward in terms of power management for integrated circuit applications. Through the combination of digital, charge-pump-based, and analog-assisted loops, the system can strike a balance between high power efficiency, rapid transient response, decreased voltage ripples, and higher supply rejection ratio (PSR). The extensive simulation results and optimized layout provide a clear illustration of the effectiveness of the proposed architecture, establishing it as a viable solution for modern mixed-signal system-on-chips (SoCs).

The tri-loop architecture was used to overcome the constraints of traditional DLDO systems. The digital coarse loop quickly responds to significant changes in load, while the charge-pump-based fine loop guarantees minimum steady-state voltage ripple and the analog-assisted loop immediately corrects for undershoots during load transients. The implementation of a dual edge triggered bi-directional shift register (DEBSR) in the digital coarse loop results in a twofold

increase in response speed, without the need to increase the clock frequency. This enhancement greatly improves the transient response. The charge-pump-based fine loop utilizes a voltage-to-time converter to accurately regulate V_{RIPP}, guaranteeing noiseless operation under stable conditions.

The proposed DLDO can be easily combined with other power management units, like buck converters, to create a complete power delivery solution in real-world SoC applications." The design's modular architecture enables scalability to more modern CMOS technologies, hence boosting performance.

Chapter 4

Chip Testing & Measurements

In Chapter 4, a comprehensive examination of the Die, packaging and measurement data for the proposed tri-loop digital low dropout (DLDO) regulator is presented. The DLDO chip that was manufactured was put through a series of tests to ensure that it performed successfully in accordance with the design criteria and to determine whether it was suitable for power management in applications that are sensitive to noise. The purpose of this chapter is to provide extensive information regarding the design of the printed circuit board (PCB) that was utilized for testing and the setup for measurement. Die Micrograph of the Fabricated Chip is shown in Fig 4.2 which can help design a testing board for it.

Fig 4.2 presents the micrograph of the DLDO chip, which was fabricated using the TSMC 180nm CMOS process and it consists of 6 metal layers. The metal configuration for 180nm CMOS is defined as 1p6m_4X1U40KA, which provides the required conductivity and reliability for the chip’s functionality. These metal layers play a critical role in the chip's electrical performance, allowing for effective signal routing and power distribution throughout the chip.

In addition to the metal layer information, the stack-up information of the chip's design is depicted in Fig 4.1. This Figure shows the different layers of the chip's structure, offering insight into the precise material arrangement and layer composition. Understanding the stack-up configuration is important for the chip's overall design performance, as it changes the thermal and electrical characteristics. By analyzing this configuration, one can get a deeper knowledge of how the layers interact with the chip’s overall functionality.

The table provides valuable information regarding the chip’s pinout and packaging. It highlights the pin placement of the pads with its location as x and y dimensions, which is necessary for connecting the chip to external components. Moreover, the table includes the wire bonding information, detailing how the pins are physically connected to the rest of the package. This information is essential to understand the assembly process and ensure that the chip can be integrated effectively into a larger system.

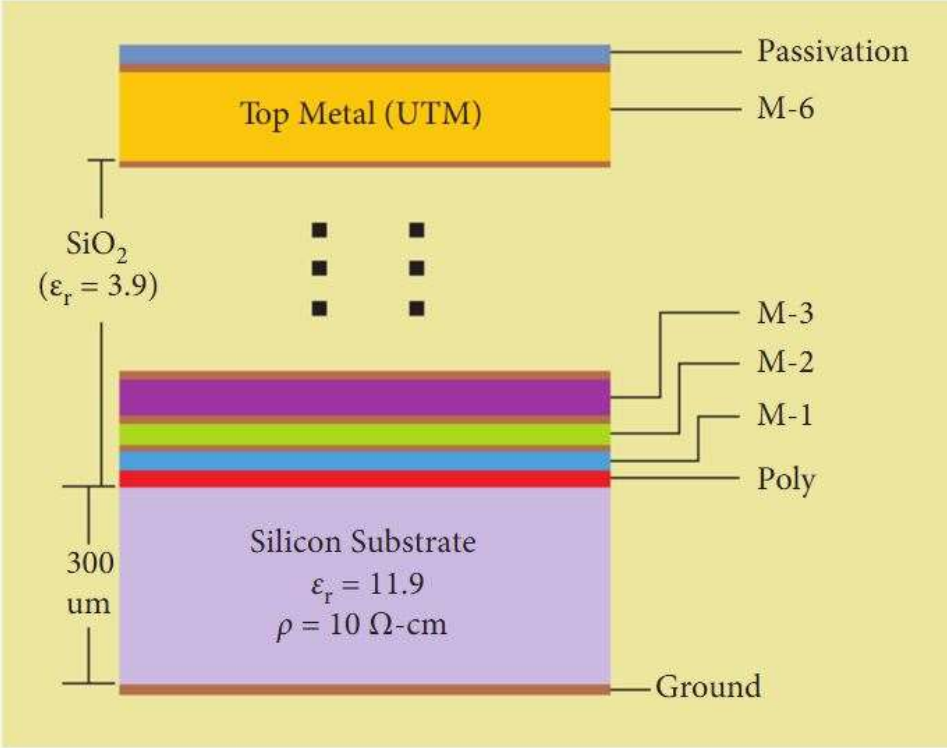


Figure 4.1: Stacked BEOL metal layers of the TSMC 180 nm CMOS process technology. [62]

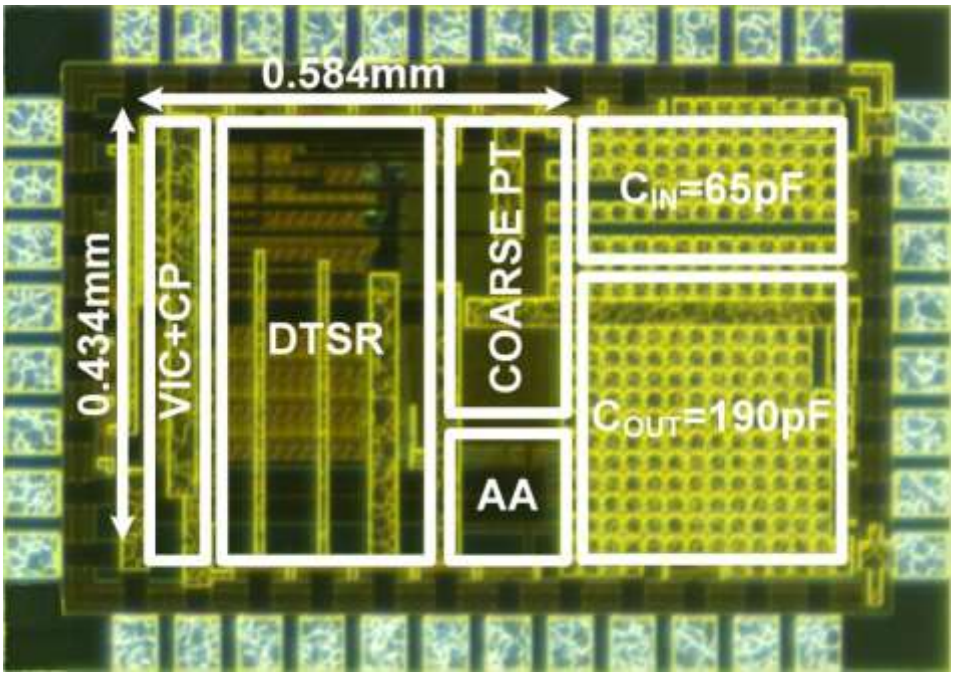


Figure 4.2: Die Micrograph.

	PKG Type: 48L LQFP 7mm x 7mm						Wiring			
	Pin No	Site	Pad No.	Pad Name	X	Y	Pad to pin	Pad to ground	Pin to ground	
1	1	left					No	No	No	
2	2						No	No	No	
3	3		1	VDD-PT	36.25	710	Yes			1
4	4		2	VREF	36.25	630	Yes			2
5	5		3	VREFH	36.25	550	Yes			3
6	6		4	VREFL	36.25	470	Yes			4
7	7		5	CLK_S	36.25	390	Yes			5
8	8		6	CLK_N	36.25	310	Yes			6
9	9		7	VG	36.25	230	Yes			7
10	10		8	VDD	36.25	150	Yes			8
11	11						No	No	No	
12	12						No	No	No	
1	13	bottom	9	VDD	160.08	36.25	Yes			1
2	14		10	VSS	248.08	36.25	Yes			2
3	15		11	VTP	328.08	36.25	Yes			3
4	16		12	VTN	408.08	36.25	Yes			4
5	17		13	UP	488.08	36.25	Yes			5
6	18		14	DN	568.08	36.25	Yes			6
7	19		15	RST	648.08	36.25	Yes			7
8	20		16	VDD_TWO	728.08	36.25	Yes			8
9	21		17	AA_BIAS	808.08	36.25	Yes			9
10	22		18	AA_EN	888.08	36.25	Yes			10
11	23		19	NOT USED	968.08	36.25	Yes			11
12	24		20	NOT USED	1048.08	36.25	Yes			12
1	25	right					No	No	No	
2	26						No	No	No	
3	27		21	EVSS	1179.91	150	No	Yes	Yes	
4	28		22	CLK-LO	1179.91	230	Yes			1
5	29		23	VSS_PT	1179.91	310	Yes			2
6	30		24	VOUT	1179.91	390	Yes			3
7	31		25	VOUT	1179.91	470	Yes			4
8	32		26	CTRL_100	1179.91	550	Yes			5
9	33		27	CTRL_50	1179.91	630	Yes			6
10	34		28	EVDD	1179.91	710	Yes			7
11	35						NO	NO	NO	8
12	36						NO	NO	NO	
1	37	top	29	NOT USED	1048.08	823.75	Yes			1
2	38		30	NOT USED	968.08	823.75	Yes			2
3	39		31	NOT USED	888.08	823.75	Yes			3
4	40		32	DIR	808.08	823.75	Yes			4
5	41		33	MOD	728.08	823.75	Yes			5
6	42		34	CLK_FINE	648.08	823.75	Yes			6
7	43		35	CLK_COARSE	568.08	823.75	Yes			7
8	44		36	REFL	488.08	823.75	Yes			8
9	45		37	REFH	408.08	823.75	Yes			9
10	46		38	MOD_SEL	328.08	823.75	Yes			10
11	47		39	MOD_IN	248.08	823.75	Yes			11
12	48		40	VDD-PT	168.08	823.75	Yes			12

4.1 Printed Circuit Board Design

A printed circuit board (PCB) that is specifically designed for the purpose of simplifying the testing and characterization of the DLDO chip was designed and fabricated. A stable bias for measurements, a reduction in interference from external sources, and a guarantee of precise performance evaluation were the goals of the development of the printed circuit board (PCB).

4.1.1 PCB Schematic

Schematic Design as shown in Fig 4.3 is the first phase of the design process, which is when the overall concept and layout of a project are produced and expressed in a visual diagram. This phase serves as the beginning of the design process. The DLDO chip, input and output capacitors, a load resistor bank, and connectors for power supply and measurement equipment were all incorporated into the schematic design of the printed circuit board (printed circuit board). A programmable power supply was connected to the DLDO chip to supply the input voltage (V_{DD}). Additionally, a digital multimeter and oscilloscope were connected to observe the output voltage (V_{OUT}) and quantify voltage ripples (V_{RIPP}), as well as line and load regulation, power supply rejection ratio (PSR), and transient response.

The DLDO chip, which was manufactured by a CMOS process with a 180-nm layer size, is the primary component that is being analyzed. A capacitor with a capacitance of 65 pF is referred to as the input capacitor (C_{IN}). This capacitor is placed near the V_{DD} pin to reduce high-frequency noise that originates from the power supply. It was necessary to make use of the output capacitor, which is also referred to as C_{OUT}, to stabilize V_{OUT} and reduce variations in output voltage. A capacitance of 190 pF was possessed by it. The term "Load Resistor Bank" refers to a collection of precise resistors that were made available to simulate a wide range of load circumstances, ranging from modest to substantial loads. Test points were purposefully placed on the printed circuit board (PCB) to facilitate accurate measurements of the voltage output (V_{OUT}), the input current (I_{DD}), and the output current (I_{OUT}).

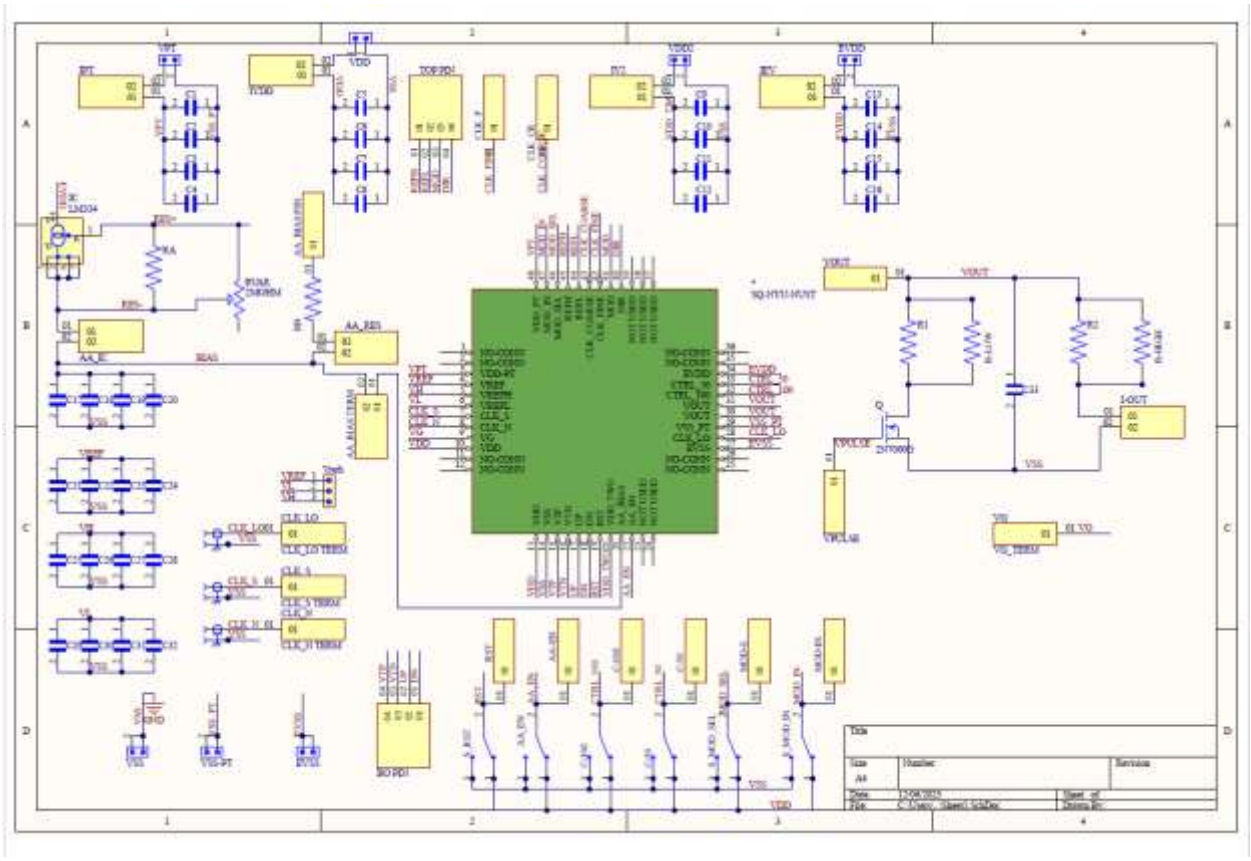


Figure 4.3: Schematic design of test PCB.

4.1.2 PCB Layout

To lessen the effects of parasitic effects and noise coupling, the layout design of the printed circuit board (PCB) was developed. To exclude any possibility of interference during the process of measurement, stringent steps were put into place to ensure that proper grounding and shielding were provided. The following are some important considerations to make while designing a key layout:

1. Reduced Trace Lengths: To lessen the detrimental impacts of parasitic inductance and resistance, the traces that connect the DLDO chip to the capacitors and load resistors were purposefully kept as short as possible. This was done to minimize the negative effects of parasitic inductance and resistance.
2. Ground Planes and Shielding: We installed many ground planes and electromagnetic interference (EMI) shields in order to reduce noise and ensure that the DLDO chip receive clean power.

3. Thermal Management: To effectively dissipate heat during periods of severe workload, sufficient gaps and thermal relief cushions were built into the design.

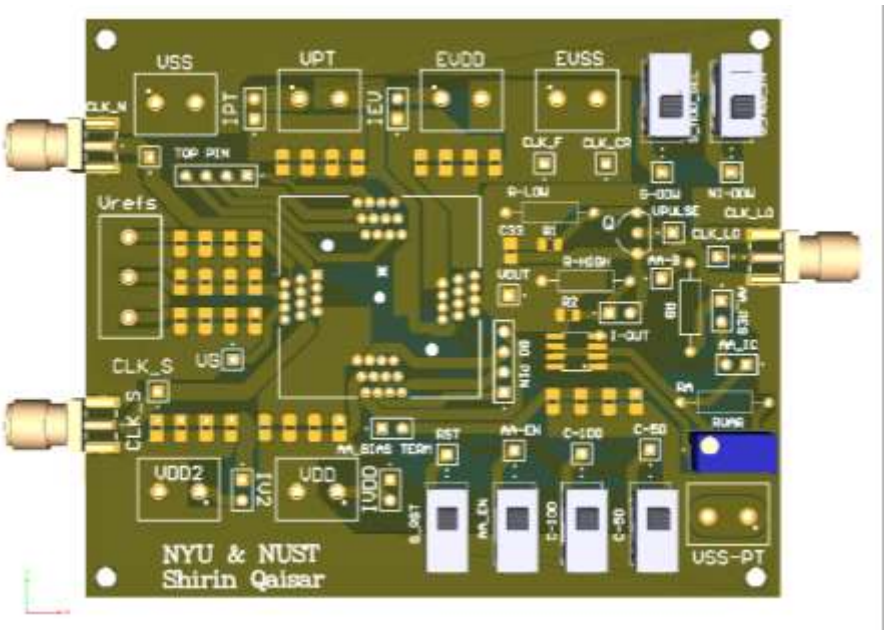


Figure 4.4: Top level layout of PCB.

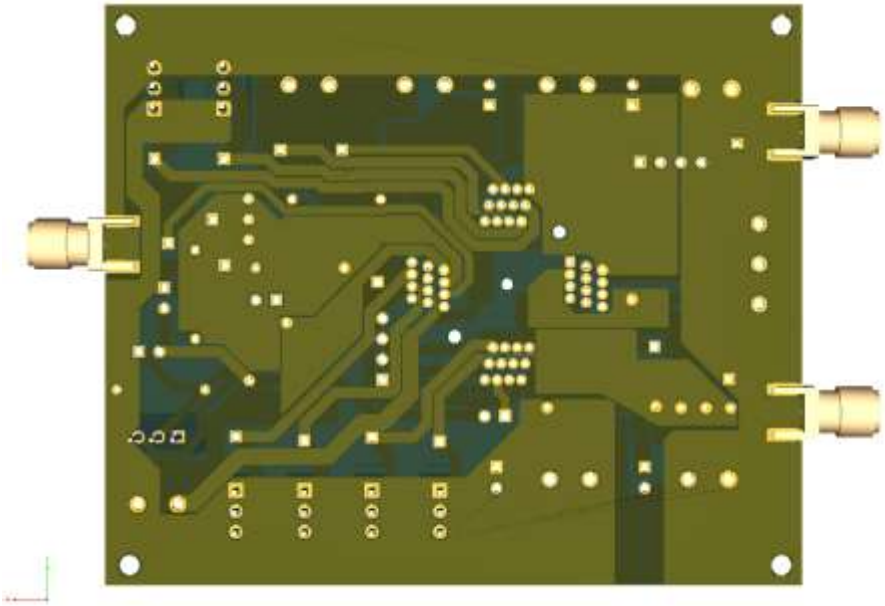


Figure 4.5: Bottom level layout of PCB.

4.1.3 Fabricated PCB

Figure 4.6: Fabricated PCB for Test.

The proposed ripple-less DLDO was designed and fabricated in TSMC 180-nm CMOS process and placed in the chip holder on PCBs shown in Fig 4.4, 4.5 and 4.6 of the study.

4.2 Measurement Setup

A test plan for evaluating the performance parameters of the proposed DLDO was created. These parameters include power efficiency, power supply ratio (PSR), line and load control, steady-state voltage ripple power (V_{RIPP}), and transient response. The setup consisted of cutting-edge measuring equipment and a controlled environment, both of which were designed to provide accurate and repeatable results. For recording the transient response, V_{RIPP}, and PSR data, a sophisticated digital oscilloscope that possessed a wide bandwidth was deployed. To measure the output voltage (V_{OUT}), the input voltage (V_{DD}), and the current (I_{DD} and I_{OUT}), high-precision DMMs were utilized.

For the aim of testing line regulation, a programmable power supply that possessed low noise characteristics was deployed. This supply was utilized to provide a constant input voltage and to

permit regulated fluctuation in V_{DD}. The evaluation of load management and transient response was made possible by utilization of a programmable electronic load that was used to simulate a variety of load scenarios.

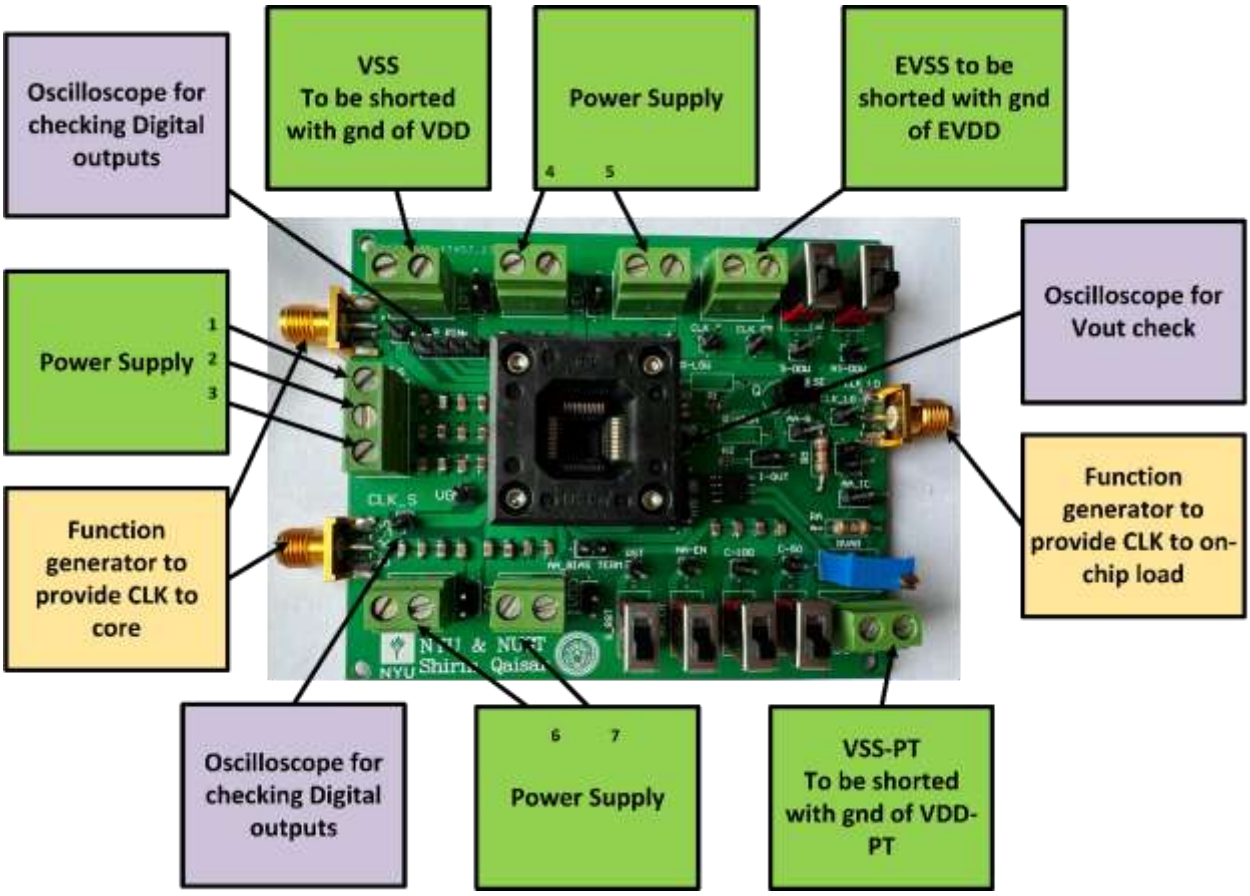


Figure 4.7: Measurement Setup Plan.

a. **Input Voltage Range (V_{DD}):** To analyze the line regulation and transient responsiveness, the input voltage was systematically varied between 0.9 V and 1.8 V. This was done to determine the range of the voltage. For evaluating the steady-state behavior and regulation, the desired output voltage, which is denoted by the symbol V_{OUT}, was set at 0.88 V. For simulating a variety of load scenarios and evaluating load control and efficiency, the current load range (I_{LOAD}) was changed to be between 1 mA and 75 mA.

b. **Temperature Range:** To determine the normal performance of the DLDO, testing was carried out at room temperature, which comes in at 25 degrees Celsius**.**

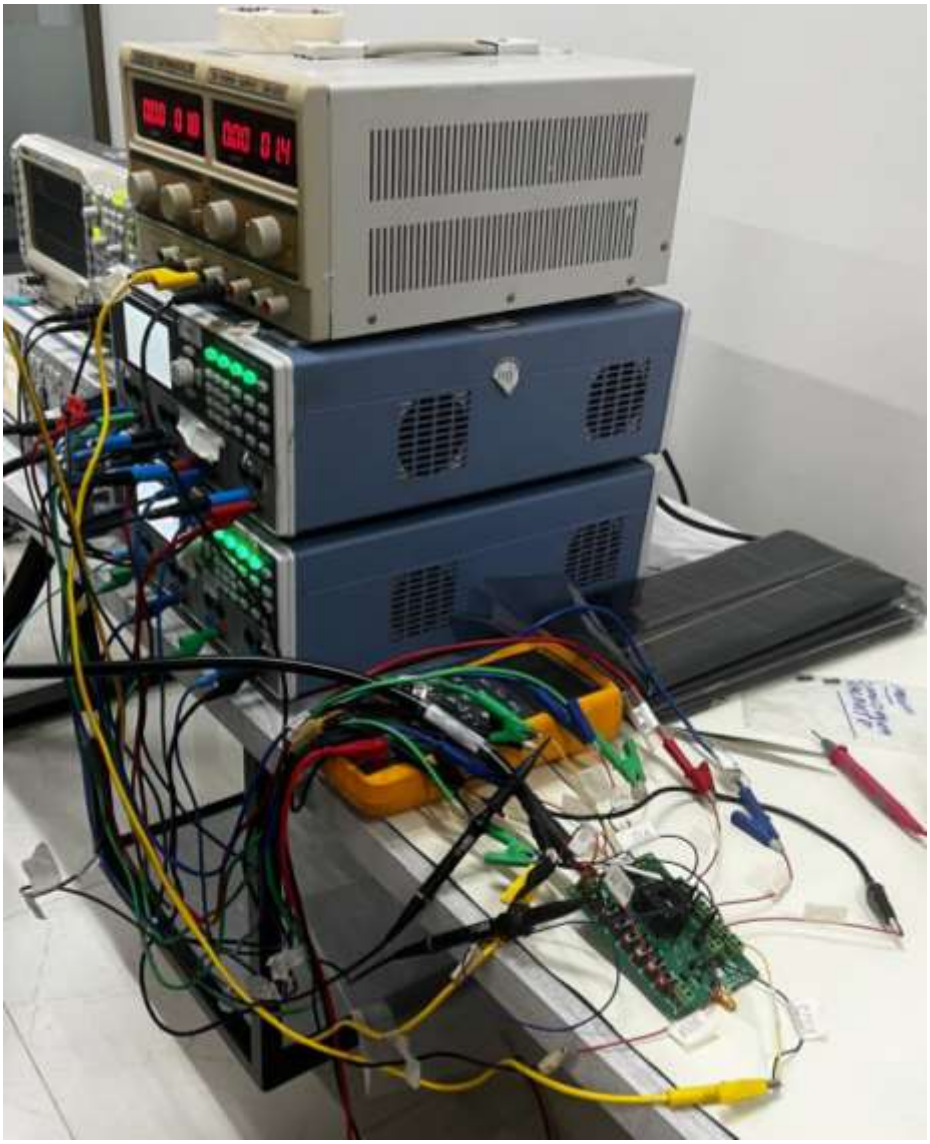


Figure 4.8: Measurement Setup

4.3 Measurement Results

4.3.1 Measurement Setup and Initial Observations

The process of measuring the chip's performance began with setting up the necessary equipment and ensuring that all power supplies and supporting devices were connected and operational as shown in Fig 4.8. This initial setup was crucial to provide stable power to the chip during the measurement process. Once the system was powered on, an issue was immediately detected. A short circuit appeared on several pins, which were critical to the chip’s functioning. Specifically,

the digital supply voltage pins, DVDD and VDD (pin numbers 8 and 9, respectively), showed signs of a short circuit.

To further investigate this anomaly, a thorough examination of the PCB test board was conducted. It was essential to determine if the short circuit originated from the external connections on the board itself. However, after conducting a meticulous inspection, no short circuit was found on the PCB test board. This initial review ruled out the possibility of the short being caused by an error or fault in the board's design or physical connections. With the external test board not showing any issues, attention was then directed towards the packaged chips themselves, where the short circuit was still evident.

4.3.2 In-Depth Investigation and Troubleshooting Measures

Given that the external board and connections appeared to be functioning correctly, a more detailed analysis of the chip's internal structure was warranted. The next logical step involved revisiting the layout of the chip and ensuring that no design-related problems were present. A Design Rule Check (DRC) was conducted to examine the layout for any violations of the predefined design rules, such as incorrect trace widths or spacing issues. In addition, a Layout Versus Schematic (LVS) check was performed to confirm that the physical layout matched the intended schematic design.

These checks were conducted both with and without the pads to ensure that any potential issues related to the pads themselves would also be identified. After completing these thorough checks, the results were clear: no design violations or errors were detected in the layout. This outcome suggested that the problem was not related to a design flaw but possibly due to an internal issue with the chip, which was not evident through standard layout verification processes. However, even though the layout and design checks showed no issues, the short circuit continued to persist. To gain further insight into the potential cause of the issue, additional diagnostic methods were considered, and the next step was to perform X-ray imaging on the chip sets. This technique allowed for a more detailed examination of the internal structures of the chips, which would not be visible through external inspection.

4.3.3 X-ray Imaging and Internal Examination

The X-ray imaging provided valuable insights into the internal structure of the chips. The scans revealed that there wasn't an issue with the wire bonding inside the chip, specifically showing that

two pads were shorted internally as shown in Fig 4.9. This internal short was not visible in the wire bonding, suggesting that the cause of the issue might be related to an internal defect in the chip's wire bonding or packaging, rather than an issue with the external design or PCB connections.

The discovery of the short pads highlighted a potential manufacturing defect that could only be observed through specialized diagnostic techniques such as X-ray imaging. However, this internal issue did not align with the design specifications or the results from previous checks, further complicating the diagnosis. While the X-ray imaging provided new information, it did not offer a definitive solution, and the problem remained unresolved at this stage.

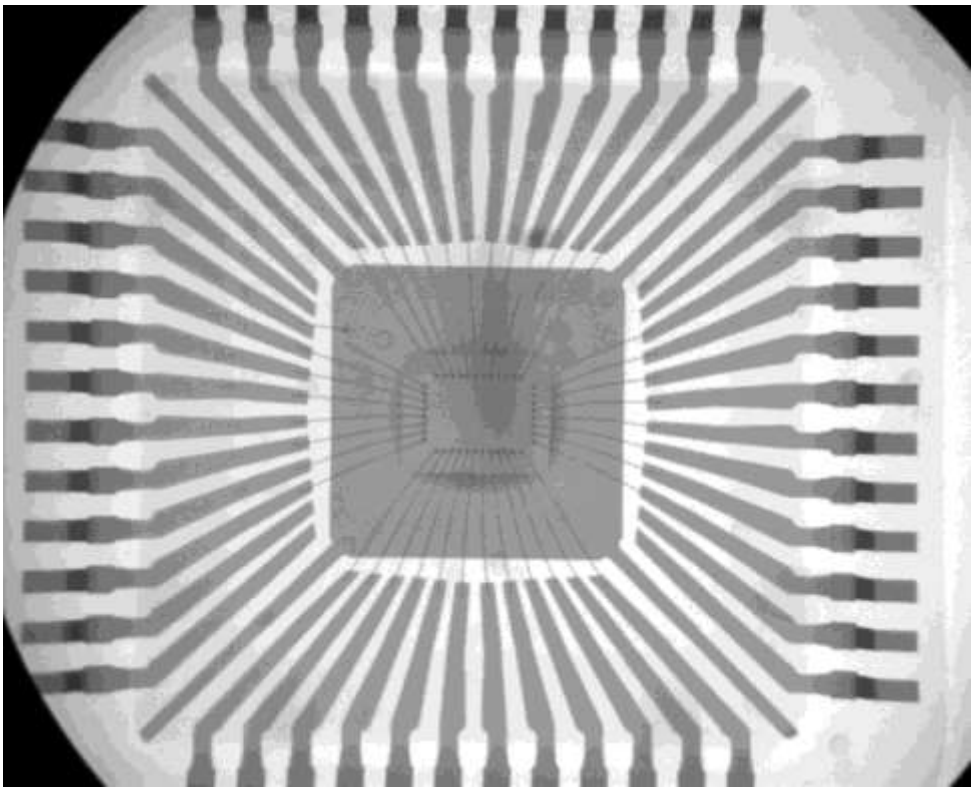


Figure 4.9: Xray image of chip for wire bonding reference

4.3.4 Final Analysis and Post-Layout Extraction

After completing the X-ray analysis, a post-layout extraction (PEX) can be performed as a final step to ensure that the layout matched the expected results after all design checks had been completed. PEX analysis involves extracting a detailed representation of the physical layout, which is then compared to the schematic to verify that there are no shorts or errors present in the

design. The PEX results should confirm that no shorts were detected in the layout after the additional testing. This step is still pending due to the unavailability of the corners file in the TSMC 180nm PDK deck.

Despite the comprehensive testing and analysis conducted, including the DRC, LVS checks, and X-ray imaging, the source of the short circuit remained unidentified. The inability to identify the root cause after such thorough testing has led to the conclusion that further investigation and additional diagnostic techniques are needed to uncover the true origin of the issue.

4.3.5 Conclusion and Current Status

At present, the short circuit issue remains unresolved, and no conclusive measurement results can be provided. The extensive testing and diagnostic methods have not led to a clear solution, leaving the root cause of the problem undetermined. Given the complexity of the issue, additional tools and further analysis will be required in the future to accurately diagnose and resolve the problem. The investigation is ongoing, and future steps will include exploring other potential internal faults or design issues that may not have been previously identified.

4.4 Summary

The measurement process described in this chapter provides a comprehensive overview of the steps taken to assess the performance of the chip under test. The chapter begins with a discussion of the chip micrograph, which offers a detailed view of the internal structure of the chip. Following the chip micrograph, the schematic and layout design of the test PCB were carefully examined. The schematic diagram outlined the essential components and their interconnections, while the layout design visually represented the physical arrangement of these components on the PCB. Once the test PCB was fabricated, the focus shifted to the measurement setup. This involved setting up the necessary equipment, including power supplies and measurement devices, to ensure that the chip received the correct power and signals during testing. However, short circuit appeared on the digital supply voltage pins, DVDD and VDD, specifically on pins 33 and 34. To investigate this issue, an initial examination of the PCB test board was conducted. The goal was to determine whether the short circuit originated from an error in the external connections or the board's physical layout. After a thorough inspection, no short circuit was found on the test board. Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks were performed with and without pads to identify any potential issues related to the pads themselves. The results of these checks

showed no violations or errors in the layout, suggesting that the issue was not caused by a design flaw but was possibly due to an internal problem within the chip. Following the X-ray analysis, a final step in the investigation involved conducting post-layout extraction (PEX). The investigation is ongoing, and further analysis will be required to explore other possible causes of the short circuit that were not detected by the current testing methods.

Chapter 5

Conclusion

A review of the most important contributions, conclusions, and ramifications of the proposed design for a tri-loop digital low dropout (DLDO) regulator is presented in Chapter 5, which serves as the conclusion to the thesis. In addition to this, it suggests potential areas that might be further investigated and developed in the future to further enhance the performance of DLDO in integrated circuit (IC) power management.

5.1 A Brief Synopsis

The purpose of the research that was carried out for this thesis was to build a novel tri-loop architecture with the intention of overcoming the limitations that are associated with conventional digital low dropout (DLDO) regulators. A digital coarse loop, a fine loop based on a charge pump, and an analog-assisted (AA) loop are the three distinct control loops that are incorporated into this architecture. The incorporation of these loops provides a comprehensive solution to the problems of rapid transient response, minimization of voltage fluctuations, improvement of the power-supply rejection ratio, and reduction of dropout voltage. An exceptional transient responsiveness was demonstrated by the DLDO prototype, which was able to achieve the desired output voltage (V_{OUT}) within a span of 300 nanoseconds during the first phase. Furthermore, it was able to recover quickly from severe load fluctuations while experiencing minimal undershoot (ΔV_{OUT}). The Digital Low-Dropout Regulator (DLDO) can successfully handle rapid load changes and maintain stable operation in dynamic conditions. This is made possible by the dual-edge triggered bi-directional shift register (DEBSR) that is a part of the digital coarse loop and the rapid current boosting mechanism that is a part of the analog-assisted loop.

By incorporating a voltage-to-time converter (V_{TC}) and a control mechanism that is based on a charge pump, the fine loop was able to successfully reduce the steady-state voltage-induced potential difference (V_{RIPP}) to a level that is lower than 140 µV. Since the suggested DLDO has a low degree of ripple, it is an excellent choice for analog loads that are sensitive to noise. Existing designs, which suffer from excessive V_{RIPP} because of the discrete nature of digital control, are surpassed by this DLDO concept.

The power supply rejection (PSR) of the DLDO was improved with the implementation of an analog-assisted loop, which led to a PSR of -30 dB at a frequency of 1 kHz. The power supply rejection (PSR) performance of the proposed DLDO has been enhanced, which enables a more efficient rejection of supply noise. This, in turn, results in an output voltage that is consistent and clean. This is of utmost significance when it comes to the provision of power to analog and mixed-signal circuits that are somewhat sensitive. In the context of power regulators, the term "low dropout voltage" (V_{DO}) refers to the minimal voltage difference that exists between the input and output of the regulator. Below this voltage difference, the regulator is unable to maintain a steady output voltage. The ability of a device or system to convert input power into useful output power with low losses is referred to as high power efficiency. On the other hand, high power efficiency refers to both capabilities. A minimal V_{DO} (Voltage Dropout) of 20 mV was achieved by the DLDO, which brings about a significant improvement in the power efficiency of the device. The DLDO exhibits a peak current efficiency of 99.93% and a maximum quiescent current (I_Q) of 47 µA, so demonstrating its exceptional efficiency under a wide range of load conditions. Because of this, it is an excellent choice for applications that require little power. A 180-nm CMOS manufacturing technique was utilized in the creation of the DLDO that is currently under consideration. The active area of the device was 0.253 millimeters squared, and it was designed to have a compact layout. The design's capacity to be simply scaled, its minimal energy usage, and its excellent efficacy make it a highly acceptable option for integration into contemporary system-on-chip (SoC) devices that demand powerful power management solutions.

In System-on-Chips (SoCs), the significance of power management lies in the design of the tri-loop DLDO is a significant advancement in the field of power management for integrated circuits, particularly in environments that are sensitive to noise and mixed signals simultaneously. The DLDO that has been proposed helps to overcome the limitations that are associated with conventional designs, providing a solution that is more all-encompassing for contemporary System-on-Chips (SoCs). The digital and analog domains are both provided with a power supply that is both efficient and low in noise thanks to this.

5.2 Future Work

DLDO architecture that was recommended has demonstrated significant improvements in performance, there are still several areas that require additional research and development. In

subsequent study, integration of the proposed DLDO framework into more advanced CMOS technology nodes, such as 65-nm or 28-nm processes, could be the primary focus of attention. It is possible to accomplish additional reductions in power consumption and space by adopting smaller feature sizes. Furthermore, it is conceivable to get improved PSR and V_{RIPP} performance because of the improved features. A supplementary line of inquiry could concentrate on adaptive control systems, which are able to dynamically adjust the gain and bandwidth of the control loops in response to real-time load conditions. This would make it possible to exercise a greater degree of control over the transient response and V_{RIPP}, which might potentially lead to an improvement in overall performance across a variety of operational scenarios.

There is the potential for more testing to be carried out to evaluate the performance of the DLDO using a wider range of temperatures and process modifications. If this were to be done, a more comprehensive understanding of its durability and dependability in a variety of operational circumstances would be achieved. To establish a full power management solution for System-on-Chips (SoCs), more research could investigate the possibility of incorporating the suggested DLDO with additional power management components. These components could include buck converters or switched-capacitor regulators. The integration of components has the potential to enhance power delivery networks (PDNs) by making them more efficient. This would result in improved performance and reduced power losses because of increased efficiency.

Future study could investigate the application of machine learning techniques to dynamically optimize the control parameters of the DLDO in real-time. This would be because machine learning has recently come into existence. This has the potential to result in power regulation that is more intelligent and adaptable, and that can successfully respond to complex load patterns.

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