Temperature Tuned Simulations of Double HeteroJunction Bipolar Transistors

By

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MASTER'S THESIS Work

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ABSTRACT

Double Heterojunction Bipolar Transistor (DHBT) is one of the promising fields of modern era of semiconductor industry. InAlAs-InGaAs-InAlAs DHBT is simulated in Synopsys TCAD. Device structure is designed in Sentaurus Device Editor (SDE). The emitter device area is taken as 1×5 μm^2. The common emitter current voltage (IV) characterization of device is studied at different temperatures from 300k to 400K with fixed base current ranging from 10 to 200 μA with step size of 10 μA. For this purpose thermionic and thermodynamic transport models were incorporated. The breakdown voltage decreases from 6.5 to 6V, while device gain increases from 40 to 45 with an increase in the temperature from 300 to 400K, respectively.

Proposed structure works well for the high frequency edge of microwave band (100GHz) which can be used for various applications such as push-pull amplifiers. An effect of the SETBACK layer (InGaAs) thickness on the break down voltage was studied. Effects of the SPACER and SETBACK layers on the break down voltages of BE and BC junctions were also reported. Hydro- and thermo-dynamic transport models along with the drift diffusion models were successfully used to understand the Physics of device.

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PUBLICATIONS

- M. F. Bhopal, J. A. Abbasi, T. Khalid, A. S. Bhatti and T. Tauqeer, *"Temperature Tuned simulation of DHBTs"* in Nanotechnology in the Edge of Convergence 24th – 27th November, 2011.
- J.Abbasi, M.F.Bhopal, T.Tauqeer "Effect of Absorption Region Thickness on the Performance of Planner InP/InGaAs/InP PiN Photodiode" inNanotechnology in the edge of Convergence" 24th – 27th November,2011.

CHAPTER ONE: INTRODUCTION

1.1 OVERVIEW AND BACKGROUND

Silicon has been the leading material of the electronics industry for the past five decades and will continue to remain so in the foreseeable future. However, silicon-based devices come under severe limitations like current gain degradation and lack of linearity when they are extended to microwave frequencies. The silicon-based Bipolar Junction Transistor (BJT) can only be used in applications in the frequency range up to a few GHz. Excellent high frequency performance characteristics of III-V compound semiconductors based devices can be harnessed, particularly in satellite, mobile and radar communications. With more of these applications being adopted for consumer uses, the market for III-V compound semiconductors based devices is expected to continue to grow.

1.2 MOTIVATION

The work is based on a motivation to do extensive modeling and simulation of high speed semiconductor devices such as in the field of double heterojunction bipolar transistor (DBHT) [1] . The work presented in [1] has been simulated for good breakdown voltages. There have been efforts to simulate DBHT for higher values of breakdown voltages. The work is based on a motivation to simulate and suggest an epitaxial structure of a DHBT that results in good high frequency characteristics.

Advantages of III-V compound semiconductors based HBTs are defined in the preceding paragraph; it is desirable to study and quantify the performance capabilities of the InAlAs/InGaAs/InAlAs DHBT and to optimize its design. Computer based simulation tools have become an integral part of the modern design process, helping speed up the time to market of integrated circuit products. Computer aided designs (CAD) are useful tools for resolving design issues like doping and layer thickness. Moreover, it can help us to understand the transistor performance and offer deep insight into the physics behind their operation. By far, the most important advantage is that simulation tools can drastically reduce fabrication costs by providing the manufacturer with the optimum structured device. Ultimately, device fabrication and characterization are required to finalize the device design.

1.3 AIMS AND OBJECTIVES

InAlAs/InGaAs/InAlAs based DHBTs were simulated and results showed complete elimination of current blocking by adding PN dipole layers in DHBTs structure. This device was simulated on different temperatures to check its performance and frequency response. InAlAs-InGaAs-InAlAs DHBT is simulated to check the gain and break down voltage. The emitter device area is taken as $(1 \times 5)\ \mu m^2$. Proposed structure works well for high frequency edge of microwave band (100GHz).

1.4 THESIS ORGANIZATION

Chapter One: A brief introduction of III-V based HBTs, also discussed what are the motivation and aims behind it.

Chapter Two: In Chapter two an overview of Band theory, PN junction, BJTs and DHBTs are discussed. The limitation and advantages of both Homojuntion bipolar transistors and Heterojunction bipolar transistors are explained.

Chapter Three: In chapter three Physical models and parameters are discussed in detail. The simulation tools used are also introduced and discussed in this chapter.

Chapter Four: Detailed descriptions of the designed DHBTs results are given which includes the Current-Voltage Characteristics (IV curves) of DHBTs, and its Frequency response.

CHAPTER TWO: HETEROJUNCTION BIPOLAR TRANSISTORS

2.1 INTRODUCTION

Excellent performances in microwave freuquency operating range and current gains have been seen of III-V based NPN bipolar transistors, due to their better material properties; mainly higher electron mobility, and distinctive bandgap alignment in the formation of two different materials in achieving a Heterojunction. NPN heterojunction bipolar transistors (HBTs) are different from the conventional BJTs in the perspective that their Emitter is replaced by a larger band gap material than that of the Base region. This has led to the decline of the electron injection barrier into the base, but adds a hole to prevent the back injected into the emission, resulting in a higher current gain of the barrier. Therefore, the base can be made thinner than the emitter region with the same doping, in order to reduce the base resistance and further improve its higher-frequency performance

2.2 BAND THEORY

When atoms come together to form a compound; their atomic orbital mixing of energies leads to the formation of molecular orbital energies. As more and more atoms start mixing, the formation of more molecular orbitals takes place, which brings in an expectation that these energy levels will begin almost or completely degenerate energy. These energy levels are then said to form bands of energy, as demonstrated in Figure 2.1.

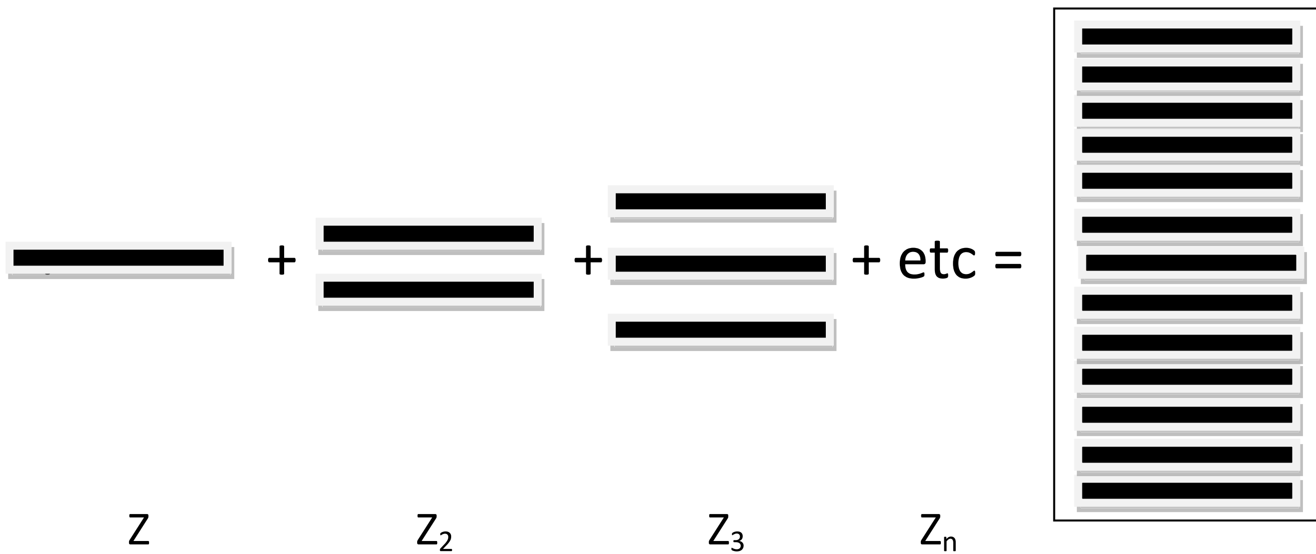

Figure2.1 An extremely over simplified diagram of band energy. Z represents one atom with an arbitrary energy level. When more and more Z atoms interact to form a crystal lattice, they all have energy levels that are practically degenerate in energy. Thus, all of these energy levels become a band, which is represented by the energy levels encased by the box [2]

On the basis of band theory, semiconductors in fact will work as an insulator at absolute zero. Above this temperature, but still lower than the melting point of solids, the metals will work as semiconductors. Semiconductors are categorized as completely occupants of valence band and conduction band left fully vacant. It requires only a certain amount of energy for the electrons to be excited to the conduction band from the valence band due to the small band gap between these two bands. Therefore, the conductivity of the solids will be based on the temperature; it would be more conductive at higher temperatures. [10, 11]

2.2.1 BAND ENERGY

As mentioned earlier, the continuous band of energy formation is a consequence of molecular orbital energy portfolio. Hence, due to the different molecular orbital mixing,

different energy bands will be formed. The difference between the energy of these bands is called the band gap, indicating that in Figure 2.2.

Band theory, focuses on electron jumps within the entire band gap. In particular, their Fermi level energies associated with jumps of electrons into the conduction band from their valence band. This "jump" is to determine the solids optical and magnetic properties. [10, 11]

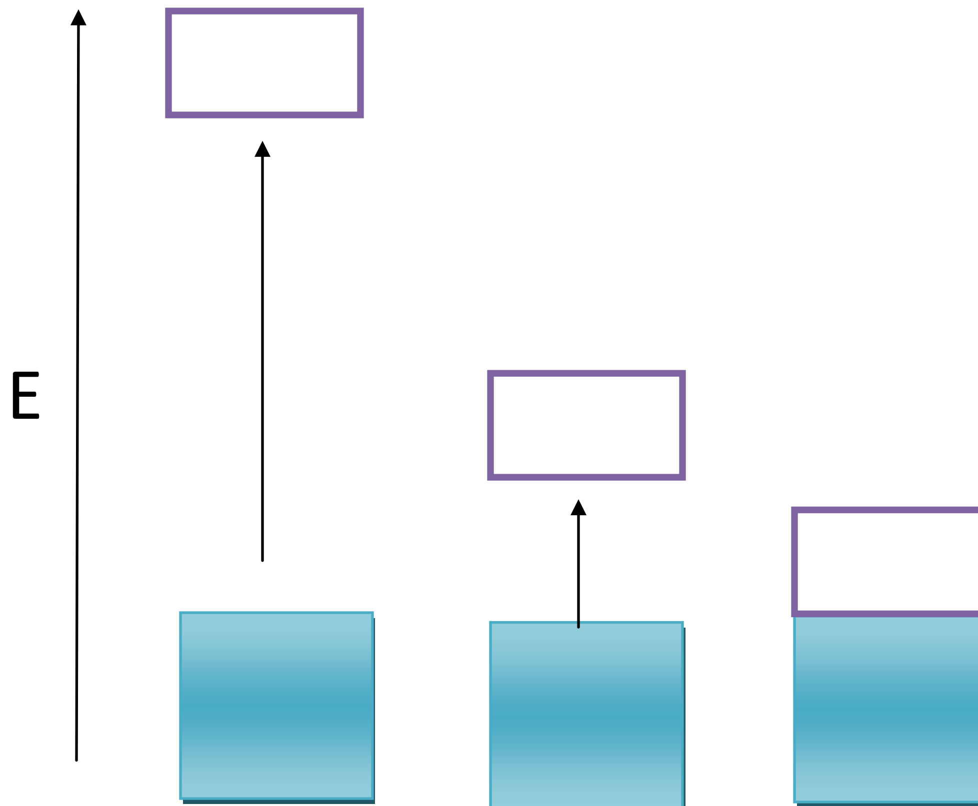

Figure 2.2 The blue boxes represent the conduction bands while the purple boxes represent valence bands. The shading of the boxes is indicative of electron density within the band. (a) band energies of an insulator (b) band energy of a semiconductor (c) band energy of a metal[2]

2.2.1.1 VALANCE BAND

All valence electrons are residual of the molecular orbitals with the highest energy and their involvement in this particular band constitutes a band of energy known as valence band.

2.2.1.2 CONDUCTION BAND

The existence of positive or negative mobile charge carriers in a band of energy constitutes a conduction band. Mobile negative charge carrier is a simple electron that possessed enough energy to leave the valence band and jump in to the conduction band. Here, they are free to move throughout the lattice, and to participate directly in the conductivity of the semiconductor. The positive mobile charge carrier is known as Hole; it refers to the non-existent of an electron in the conduction band. In other words, a hole in the band refers to the fact that an electron can exist (i.e. negative mobile charge carriers), but no longer exist in that specific location. However, electron has the potential to exist, but it does not exist, it is referred to as the mobile positive charge carrier.

2.2.1.3 FERMI LEVEL

This level at absolute zero when it's the highest occupied molecular orbital is known as the Fermi level; it's usually located in the center between the valence band and conduction band. A particle in this state has its own quantum state and generally does not interact with the other particles. When the temperature begins to

rise above absolute zero, the particles will begin occupation of states above the Fermi level while the Fermi level's lower states become vacant.

2.2.2 SEMICONDUCTORS

Semiconductors are defined to have conductivity in between an insulator and a conductor. Due to this property, semiconductors are very common in every day electronics since they likely will not always short circuit like a conductor. They get their characteristic conductivity from their small band gap. Having a band gap prevents short circuits since the electrons aren't continuously in the conduction band. A small band gap allows for the solid to have a strong enough flow of electrons from the valence to conduction bands in order to have some conductivity.

Electrons in the conduction band become free from the nuclear charge of the atom and thus can move freely around the band. These free-moving electrons are known as a negative charge carriers and results in the electrical conductivity of the solid. When the electron leaves the valence band, the state then becomes a positive charge carrier, or a hole. [10, 11]

2.2.2.1 INTRINSIC SEMICONDUCTORS

An intrinsic semiconductor is one which is based on the properties of the material itself, and is a pure semiconductor, they are also known as i-types. Here, the number of electrons in the conduction band is equal to the number of holes in the valence band.

2.2.2.2 EXTRINSIC SEMICONDUCTORS

Impurity has been added as a dopant in order to improve the conductivity of the semiconductor. There are two types: p-type and n-type extrinsic semiconductors. Add a "dopant" to the atomic lattice in order to attract the electrons from the valence band, and the atom is called as the acceptor. With more and more of the acceptors being added to the lattice, the number of holes begins to exceed the amount of negative charge carriers, eventually leading to the p-type semiconductor (positive type). N-type semiconductor with a large number of donors, atomic doping is through dopants donating electrons to the conduction band. [10, 11]

2.3 METAL SEMICONDUCTOR CONTACTS

Metal-semiconductor contacts are an evident component of any semiconductor device. At the same time, such contacts cannot be assumed to have a resistance as low as that of two connected metals.

2.3.1 OHMIC CONTACT

An Ohmic contact, ideally, is capable of delivering the required current with no voltage drop at metal and semiconductor interface and its current-voltage (I-V) curve is linear and symmetric. In real life, therefore, an Ohmic contact must have resistance as small as possible to make it negligible in comparison to the bulk or series resistance of semiconductor. A metal-Si contact

appears Ohmic when Si is heavily doped, It makes Schottky barrier thin enough for tunneling. It is used to make the contact of device with outside world. [10]

2.3.2 SCHOTTKY CONTACT

Schottky barrier refers to a metal-semiconductor contact having a large barrier height and low doping concentration that is less than the density of the states in the conduction band or valence band. Also it is a majority carrier device, where electron-hole recombination is usually not important thus it works like a rectifying diode but with a very fast switching time/frequency response, low forward voltage drop and also has large reverse-saturation current density than pn junction diode. I-V curve of Schottky contact is non-linear and asymmetric. Therefore, Schottky diodes are used in applications where the speed of response is important e.g, in microwave detectors, mixers and varactors. Also schottky diodes are now becoming viable tools for various sensing applications such as liquid, biochemical, chemical and gas sensors. [10]

2.4 PN JUNCTION

PN junction can be seen as a close contact between isolated n-type and p-type materials Figure 2.3(a). Rich in n-type material, the electron diffusion to the p-type material takes place. The same process occurs in the p-type material for the holes. The flow of such charges set an electric field, which hinders the further diffusion process until the balance is achieved, and the equilibrium energy band diagram is shown in the figure 2.3 (b). (Note that when $N_A \neq N_D$, the E_i crossing E_F does not meet the metallurgical junction). However, the overall conversation of the charges to take place, it follows for a sudden (step) at the junction[3]

$$W_{dp} N_A = W_{dn} N_D$$

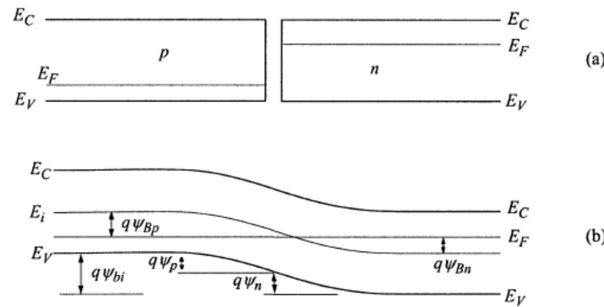

Figure 2.3 (a) P-N type (b) Energy Band Diagram [3]

2.3 BIPOLAR TRANSISTOR THEORY

A review on homojunction BJT's basic operations and its understanding is essentially desirable in order to discuss the InAlAs /InGaAs /InAlAs heterojunction bipolar transistors HBTs performances. The BJT consists of three main layers, namely the emitter, base and collector and all are of the same material.

The emitter and collector doping is of the same type, while the layer in between them known as the base is of a different doping. The basic principle of the BJT is the base controlled flow of current from the emitter to the collector, based on an assumption as the NPN transistor, the emitter and collector is the n-type and the base is p-type.

PN junction's main feature is the minority carrier's injection across the barrier when it is forward biased forms a BJT operational basis. Under normal operating conditions of the NPN

transistor, the base-emitter junction is forward biased at V_{BE} ($V_{BE} > 0$), and the base-collector junction reverse biased at V_{BC} ($V_{BC} < 0$). Under forward bias, the minority carrier concentration in base emitter junction is to enlarge the junction by a factor of $exp^{(qV_{BE}/kt)}$ according to the law of junction, where the V_{BE} is the base emitter junction applied voltage. For normal operation of the transistor, the width of the base W_B should be less than the electrons diffusion length L_n [13, 14]. This is because the electrons injected in to the base must not be recombining too much with the holes in the base, and this is ensured when maximum electrons reach collector through base after being injected from the emitter. When these minority carriers arrive at the base- collector junction, the high electric field in the base-collector reversed bias junction rapidly sweeps them to collector; the field also constitutes the collector current as shown in Figure 2.4

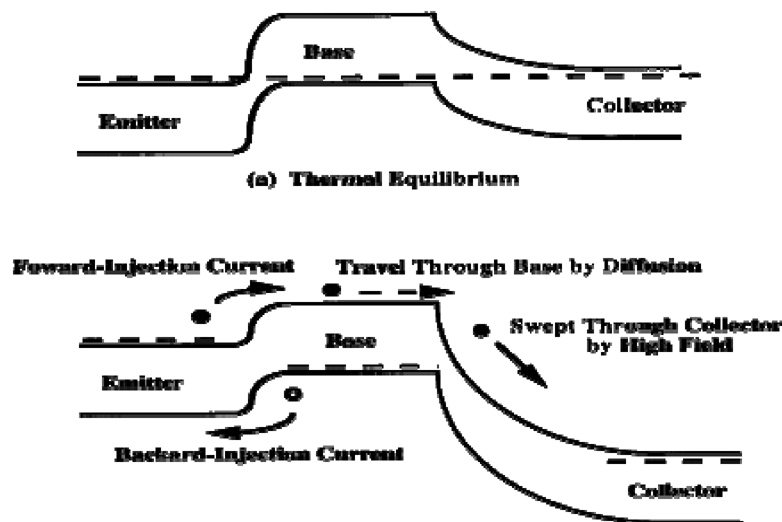

Figure 2.4 Band diagrams of an npn homojunction bipolar transistor under (a) thermal equilibrium (b) and in the normal, forward-active mode [13]

BJT's heat balance and the the band diagram under normal operation is shown in Figure 2.4. The dashed line in Figure shows the Fermi levels in each region of the transistor. We can see lightly doped collector region and heavily doped emitter region for a normal BJT. Under normal operating conditions, the two currents constitute the operation of the transistor, the current from the emitter to the collector (i.e. the collector current I_C) and the base current (I_B). The base current is usually due to back injection of holes from the base to emitter. Solving the carrier continuity equations; the base current and collector current are as follows [13, 14]

$$I_B = \frac{qA_E D_{pE}}{X_E} \frac{n_{iE}^2}{N_E} \exp\left(\frac{qV_{BE}}{kT}\right) \qquad 2.1$$

$$I_C = \frac{qA_E D_{nB}}{X_B} \frac{n_{iB}^2}{N_B} \exp\left(\frac{qV_{BE}}{kT}\right) \qquad 2.2$$

where A_E is the emitter junction area, N_E is the emitter doping level, X_E is the emitter thickness, D_{pE} is the minority hole diffusion coefficient in the emitter, n_{iE} is the intrinsic carrier concentration in the emitter, N_B is the base doping level, X_B is the base thickness, D_{nB} is the minority electron diffusion coefficient in the base and n_{iB} is the intrinsic carrier concentration in the base.

A simple analysis of these two equations lead to the findings that in order for the collector current to be greater than the base current, it is necessary that the emitter doping level exceeds the base doping level. To do so, we have to deal with an important

transistor design parameters. In order to maintain the base doping level at a lower value means that the base has to have a value of high resistance. However, this is achieved by expanding the base, which will in turn contribute significantly to the electron's base transit time, thus reducing the device's maximum operating frequency (f_{max}) and current gain. Therefore, for a fixed base doping level, the BJT current gain can be increased, initially, by increasing the emitter doping.

However, a major emitter band-gap narrowing can be achieved with an emitter doping around $N_E \sim 1x10^{18}/cm^3$, resulting in lower current gain. BJT's Homojunction nature therefore, provides us with a set of conflicting requirements; where without sacrificing the current gain an increase the base doping can't be incorporated. This limits the BJT operation to low-frequency amplifiers, filters and oscillators applications.
HBT's performance can be significantly better than that of BJT, if a highly doped base is achieved while keeping relatively lower emitter doping, it is feasible because of the wide band gap emitter of HBTs. This is where heterojunction bipolar transistor has made tremendous progress; the operation frequency is in of 100's of gigahertz range.

2.5 HETEROSTRUCTURES

A heterostructure is the interface that occurs between two layers or regions of dissimilar crystalline semiconductors. These semiconducting materials have unequal band gaps as opposed to a homojunction. The "bringing together" of these different semiconductors is not a simple procedure, but involves complicated fabrication processes. Heterojunction in which the type of dopant changes at the junction are called anisotype, and heterojunction

in which the type of dopant is the same on both sides are called isotype. Since different semiconductor materials generally do not have the same energy bandgap, there will be a discontinuity in the energy bands at the interface.

2.5.1 TYPES OF HETEROSTRUCTURES

As these heterostructures have different band gaps and electron affinities, these results into different combinations of E_c and E_v arrangement at the interface.

This band arrangement is classified into three categories as shown in Figure 2.5.

a) Type I or straddling heterojunction
b) Type II or staggered heterjunction
c) Type III or broken-gap heterojunction

One of the two materials having lower E_c and higher E_v than the other two types with less E_g in type-I. In a type II (staggered) heterojunction, the locations of lower E_c and higher E_v are moved for collection of electrons at lower E_c and holes at higher E_v for the confinement in various regions. A type-III (broken-gap) heterojunction is a particular case of Type-II, With E_c lower than the E_v of the other. Overlapping of conduction and valence band at the interface is termed as broken gap.

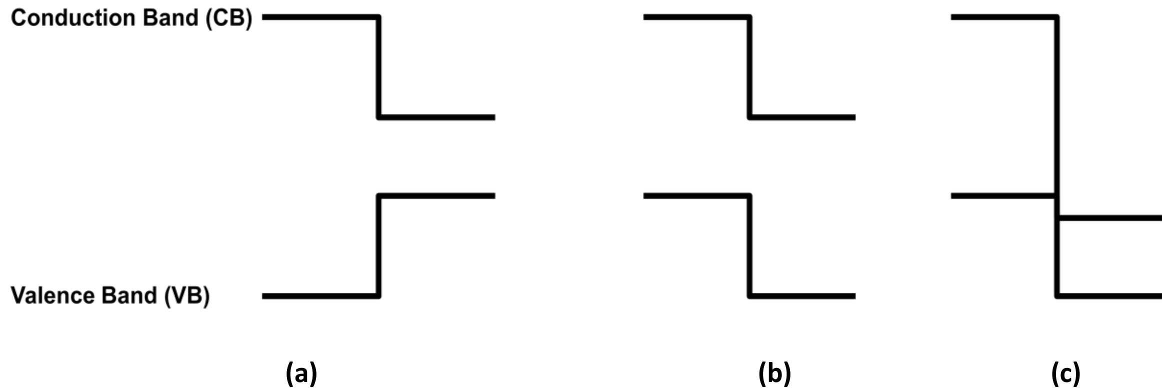

Figure 2.5 Classification of heterojunction (a) Type-I (b) Type-II (c) Type-III [14, 4]

2.6 HETEROJUNCTION BIPOLAR TRANSISTOR

Various doping of Impurities resulting in giving control on the type of conductivity of a semiconductor material and the idea of injecting non-equilibrium carriers can be said to be the basis of the development of Semiconductor electronics. With the development of heterostructures on the same basis of semiconductor electronics, it solved the general problem of the basic parameters of semiconductor crystals and devices, and provided internal control over: the band gap, effective masses of charge carriers and mobility, refractive index, electron spectroscopy, etc. [13, 14]

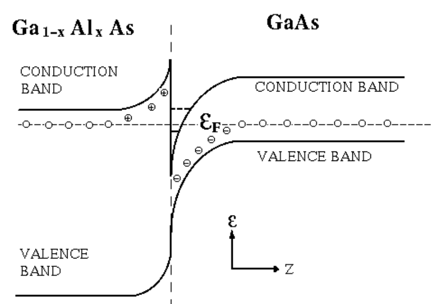

Figure 2.6 HETEROJUNCTION [16]

Excellent performances in microwave frequency operating range and current gains have been seen of III-V based NPN bipolar transistors, due to their better material properties; mainly higher electron mobility, and distinctive bandgap alignment in the formation of two different materials in achieving a Heterojunction. NPN heterojunction bipolar transistor (HBTs) is different from the BJTs in the perspective that their emitter is replaced by a larger band gap than that of the base material as shown in Figure 2.7. This has led to the decline of the electron injection barrier into the base, but adds a hole to prevent the back injected into the emission, resulting in a higher current gain of the barrier. Therefore, the base can be made thinner than the transmitter in the same doping, in order to reduce the base resistance and further improve its higher-frequency performance.

Shockley's heterojunction bipolar transistors initial description terminated with describing them as possessing wide band gap emitter, whereas now it's a fact the the collecter of a wide band gap material can have a great advantage as well. Using the same materials for the emitter and the collector forms a double heterojunction bipolar transistor (DHBT), with single junctions both at the emitter-base and the base-collector. Setting up the heterojunction bipolar transistor IC can result in to numerous advantages with interchangeable collector and emitter.

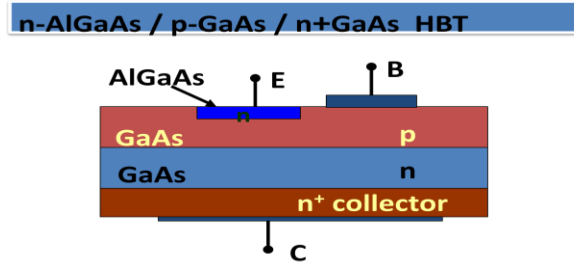

FIGURE 2.7 Schematic Diagram of Single Heterojunction Bipolar Transistor [13]

Heterojunctions are of two types, both graded and abrupt. Abrupt heterojunction, two different bandgap possessed semiconductors aggregate and the interface is abrupt with sudden changes in the composition. Graded heterojunction, is one with gradually changing composition across the heterojunction, with energy band peak seen in the abrupt heterojunction interface band edge discontinuity is inhibition. However, we will only discuss the abrupt junctions, because it is directly related to this work. Npn HBTs is such that by limiting hole back injection into the emitter, the emitter injection efficiency is close to the ideal value of unity, regardless of the doping levels of the emitter and the base [14]. In most cases, the conduction band of the emitter lies above that of the base and the current gain of the device is given by equation2.3. [13] In the heterojunction valence band discontinuity is also very important, because it controls the back injected into the emitter. The ratio of the electron to hole currents across the emitter-base heterojunction is given approximately by [13]

$$\frac{I_n}{I_P} = \beta_{max} = \frac{N_E}{N_B}\frac{v_{nb}}{N_E}\exp\left(\frac{\Delta E_g}{kT}\right) \qquad 2.3$$

where ΔE_g is the difference in bandgap between the emitter and base, where N_E is the emitter doping, N_B is the base doping and V_{nb} and V_{pe} are the thermal velocities of electrons and holes in the base and emitter, respectively. This result assumes negligible recombination in the base and $\Delta E_v = \Delta E_g$, so it gives the maximum possible current gain. When $\Delta E_v \neq \Delta E_g$ then the emitter base energy bandgap difference increases the I_n/I_p ratio by a factor of $\exp(\Delta E_v/kT)$ relative to that for BJTs and the valence band ΔEv discontinuity at the heterojunction replaces ΔEg in (2.3) and is directly related to the current gain as follows [13]

$$\frac{I_n}{I_P} \sim \exp\left(\frac{\Delta E_V}{kT}\right) \qquad 2.4$$

So if the valence band discontinuity is sufficiently large, as it is for the InAlAs/InGaAs HBT, a significant current gain can be expected even if $N_E=N_B$. For an abrupt heterojunction bipolar transistor, an advantage of the potential barrier (spike) in the conduction band at the emitter-base interface is that the barrier facilitates the injection of the electrons into the base region with a high velocity ($\sim 1x10^8$ cm/s) that exceeds the saturation velocity. The result is a highly efficient and very fast, near-ballistic electron transport through the base. Thus, an HBT can be designed for high frequency operation using a highly doped base without compromising injection efficiency or current gain.

Figure 2.8 shows the schematic diagram of SHBTs and DHBTs, it shows the difference between the SHBTs and DHBTs. Both structure starts from InP substrate, in DHBTs same material is

used in emitter and collector, on the other hand in SHBTs Base and Collector have same material.

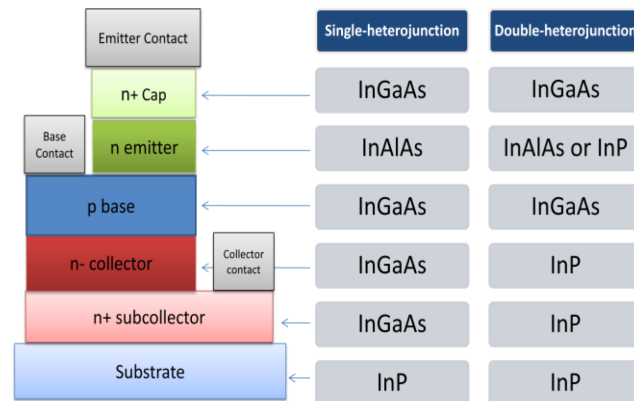

FIGURE 2.8 Single- and double-heterojunction bipolar transistors (SHBTs and DHBTs, respectively) are made using a combination of materials, but start with an indium phosphide substrate.

2.7 ADVANTAGES OF HETROJUNCTION BIPOLAR TRANSISTOR

One of the main advantages of the DHBTs, including InAlAs/InGaAs/InAlAs DHBT, is that they have a low turn-on voltage of ~0.4V translating into higher power gain and power added efficiency, which is extremely important for portable devices like mobile phones running on limited power sources like batteries.

The hole injection from the base to the collector is suppressed because of the wide bandgap collector. This is particularly important if the transistors are being used for digital switching operations. Use of a wide gap collector facilitates the use of higher base doping and at the same time keeping the collector doping low. In addition, there is a complete suppression of parasitic

charge storage, combined with greatly reduced RC-time constant due to lower base resistance as a result of higher base doping.

Using the same material for the emitter and the collector produces a double heterojunction transistor (DHBT), one at the emitter and the other at the collector junction. This translates into a huge advantage when HBTs are incorporated into ICs since the collector and emitter can be interchanged.[5]

Specific material systems like the InAlAs-based materials offer superior transport and thermal properties than InGaAs based materials. In fact, InAlAs-based HBTs have demonstrated some of the highest microwave performances and InAlAs-based DHBTs have additional benefits like enhanced breakdown voltages.[6]

2.8 IV Curve of DHBTs

To understand the behavior of DHBTs, I-V characteristic curve of DHBTs is shown in Figure 2.9 and Figure 2.10. In Figure 2.9 along horizontal axis V_{CE} is applied to DHBTs while left vertical axis represent the Collector current at various fixed Base current values. In Figure 2.9 along horizontal axis V_{CB} is applied to DHBTs and vertical axis represents Collector current at different temperature and fixed value of Collector current applied.

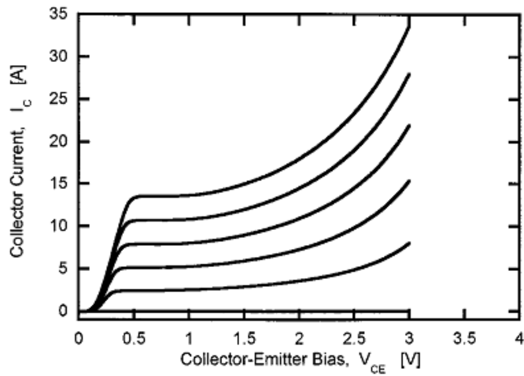

Figure 2.9 Collector-Emitter Characteristics [8]

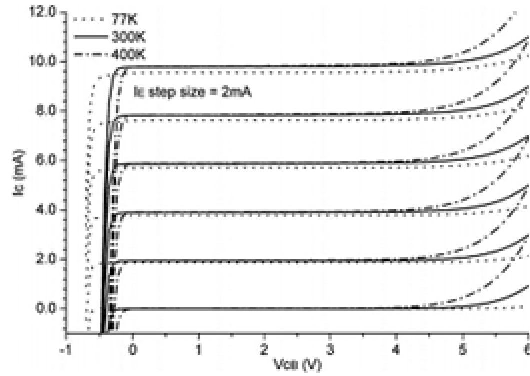

Figure 2.10 IV curves in Common Base configuration [1]

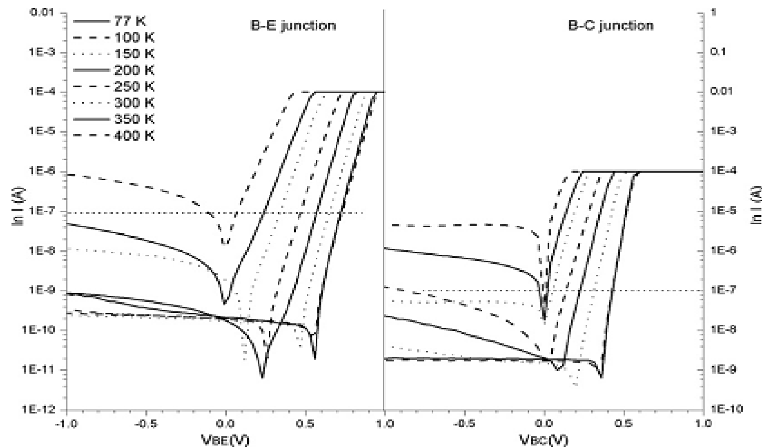

Figure 2.11 B-C and B-E junction Characteristics at different temperatures [1]

Figure 2.11 shows the B-E and B-C junction characteristics of DHBTs at different temperatures. Figure 2.10 shows the IV curves of Common base configuration shows that at higher temperature break down voltage decreasing because with increasing in temperature recombination pairs bonds break and depletion region becomes thin**.** Curves are measured at I_E 2mA step size.

CHAPTER THREE: HBT PHYSICAL MODELLING AND SIMULATION

3.1 Overview

In this chapter methodology of the research is discussed carried out in the state of the art software Technology CAD (TCAD). The TCAD tool incorporates the physical models of the semiconductor devices to predict the behavior of the device. Then design of the device, functionality and parameters are discussed.

3.2 Technology CAD

Modern day semiconductor processing techniques and softwares like Technology Computer Aided Design (TCAD), Silvaco, etc. has made possible to improve the performance of devices. Upgrading of conventional devices for better performance is also an ongoing process which becomes possible with the availability of such technology. To design, develop and optimize the semiconductor processing technology and devices, TCAD simulation provides the facility to solve fundamental and physical partial differential equation for processes and complex device structures. Now a day's semiconductor industry is extensively rely upon these tools as it save time and cost and improves quality and performance of the devices [12]. The main modules of the software used in this work are as follows:

- Sentaurus workbench
- Sentaurus process
- Sentaurus structure editor

- Sentaurus device
- Tecplot
- Inspect

The brief descriptions of these TCAD modules are given below

3.2.1 Sentaurus Workbench

To simulate a device several modules are required at a time e.g sentaurus process simulate processes and virtually fabricate the device, sentaurus device can be used for structure of the device and meshing strategy, Techplot and Inspect are used for analysis of characterization. All these modules are integrated in sentaurus workbench to work in a chain fashion and this module is capable of sharing data from one module to another.Sentaurus Workbench allows users to define parameters and variables in order to run comprehensive parametric analyses. The resulting data can be used with statistical and spreadsheet software. The GUI window with one of the project can be seen in Figure 3.1.

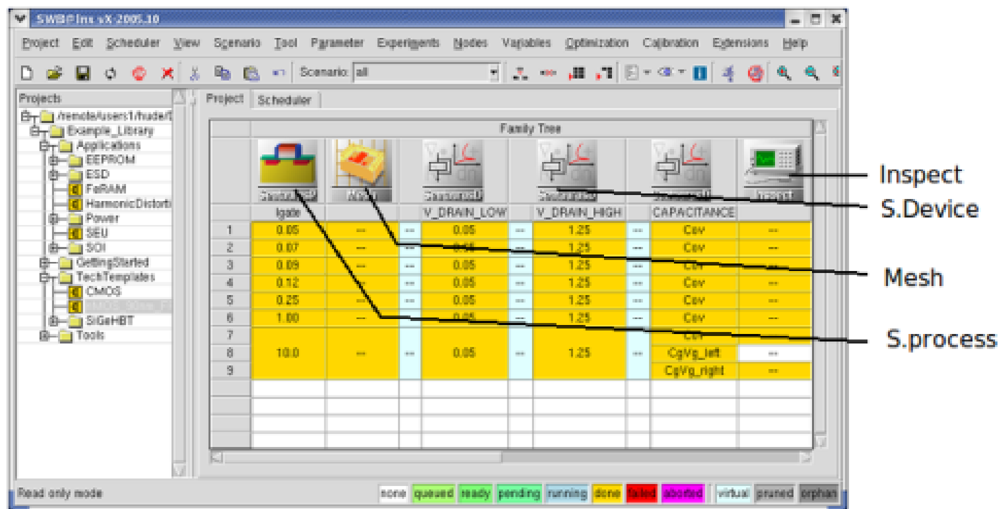

Figure3.1: Graphical user interface of sentaurus workbench with loaded project. Different modules are indicated.

3.2.2 Sentaurus process

Sentaurus Process is a complete and highly flexible, multidimensional, process modeling environment. With its modern software architecture, it constitutes a new tool generation and a solid base for process simulation like etching, deposition, epitaxial growth implantation etc. Calibrated to a wide range of the latest experimental data using proven calibration methodology, Sentaurus Process offers unique predictive capabilities for modern silicon and non silicon technologies. [12]

3.2.3 Sentaurus structure editor

Sentaurus Structure Editor is used to create structures of semiconductor devices in 2D and 3D. Geometrical structures such as rectangles, cuboids, cylinders and spheres are used in graphical user interface to create designs of devices. Rounded edges are generated by filleting, 3D edge blending, and chamfering. Complex shapes are generated by simply intersecting primitive elements. Meshing of the device can also be constructed in this module.

3.2.4 Sentaurus device

Sentaurus Device is capable of simulating the electrical, thermal, and optical characteristics of silicon-based and compound semiconductors. This module provides the facility to simulate the device by defining different physical models defined in Chapter 3 under different environmental and operational conditions. For characterization different parameters like current, voltage, bandgap, doping levels, electric field etc. can be defined. These parameters are plotted in inspect and techplot modules.

3.2.5 Techplot

Tecplot Sentaurus Viewer (SV) is an advanced visualization tool for viewing 2D and 3D devices. In addition, it can extract slices of data along the coordinate axes or user-defined lines of a 2D device, obtain 2D cross sections of 3D devices, and perform mathematical operations on the extracted data. In this module different parameters of the device can be seen in multicolored snapshot format inside the device geometry that can be converted to xy plots.

3.2.6 Inspect

Inspect is a TCAD plotting and analysis tool for XY data, such as 1D doping profiles and terminal characteristics of semiconductor devices. Its script language and library of mathematical functions allow users to compute using curve data, and to manipulate and extract data from simulations. Inspect is a versatile tool for efficient viewing of XY plots and I-V curves. Inspect extracts parameters, such as junction depth, threshold voltage, and saturation currents, from the respective XY plot. Users can manipulate curves interactively by using scripts. Inspect features a large set of mathematical functions for curve manipulation, such as differentiation, integration, and find min/max.

3.3 Device Physics and Models

The simulation technique is a numerical one, which arrives at the terminal characteristics of the device by solving the partial differential equations describing the physics of the materials and the effects of potentials and heterojunctions on carrier transport. These equations include Poisson's equation, the carrier continuity equations and the transport equations for each carrier (electrons and holes). These equations must be solved simultaneously and self consistently in each region

of the device. Here, a brief description of the basic semiconductor equations involved is provided.

3.3.1 Poisson's Equation

Mathematical form of Poisson equation is given in equation 3.1 [12]. Space charge distribution and the electrostatic potential are given by Poisson's equation,

$$\nabla.\varepsilon\nabla\varphi = -q(p - n + N_D - N_A) - \rho_{trap} \tag{3.1}$$

where

ε is electrical permittivity

q is elementary charge

n and p are electron and hole densities

N_D and N_D are concentrations of donor and accepter ions

ρ trap is charge density contribution by trap and fixed charges

3.3.2 Continuity Equations

Continuity equation for both types of charge carriers (n and p) are given in following equations 3.2 and 3.3 [12]. Overall effect when drift diffusion, and recombination occur simultaneously in a semiconductor material, the governing equation is called the continuity equation.

$$\nabla.\vec{J}_n = qR_{net} + q\frac{\partial n}{\partial t} \qquad 3.2$$

$$-\nabla.\overrightarrow{J_p} = qR_{net} + q\frac{\partial p}{\partial t} \quad 3.3$$

where

q is elementary charge

Rnet is the net electron and hole recombination rate and

J_n and J_p are the electron and hole current densities

3.3.3 Transport Eqaution

The hole and electron current densities J_p and J_n are important terms in (3.4) and (3.5) and therefore they justify further elaboration. These two terms are derived from the drift-diffusion model relating the carrier concentrations to the current density and are given as follows [12]

$$J_P = q\mu_p pE(x) - q\, D_P\, \frac{\partial P(x)}{\partial x} \quad 3.4$$

$$J_n = q\mu_n pE(x) - q\, D_n\, \frac{\partial n(x)}{\partial x} \quad 3.5$$

Where μ_n and μ_p are electron and hole mobilities, and D_p and D_n are hole and electron diffusion constants. The first term involving the E(x) is called the drift current while the second term refers to the diffusion current. By default, TCAD SYNOPSYS solves both equations.

However, for some specific circumstances, it is sufficient to solve for only one carrier. Device modeling consists of the solution to the above defined Equations' (Poisson, continuity and current density equations) subject to boundary conditions imposed by the device geometry and biasing. The previously discussed set of five equations provides a basic framework for device simulation once a device structure and its biasing have been specified. These current density

equations are based on transport models that are obtained by applying approximations and simplifications to the Boltzman transport equation. However, to completely and accurately define the device model, it is essential that each of the parameters in equation 3.1 to 3.5 be further defined by secondary equations. For example, the electron mobility maybe a function of position x if the doping is not uniform, since the mobility varies with the doping level. In the simplest cases the material parameters are just constants, but they must be specified for each material incorporated in the device.

Other models incorporated in the simulation include ones for the carrier generation recombination mechanism, band gap narrowing model at high doping density, density of states for different materials and velocity saturation effects at high electric fields.

3.3.4 Heterointerface

Sentaurus Device supports both abrupt and graded heterojunctions, with an arbitrary mole fraction distribution. In the case of abrupt heterojunctions, Sentaurus Device treats discontinuous datasets properly by introducing double points at the heterointerfaces

Conventional transport equations cease to be valid at a heterojunction interface, and currents and energy fluxes at the abrupt interface between two materials are better defined by the interface condition at the heterojunction. In defining thermionic current and thermionic energy flux Sentaurus Device follows the literature.

3.3.5 Thermionic Emission Model

Heterointerface between materials 1 (InAlAs) and 2 (InGaAs), the conduction edge jump is positive, that is $\Delta E_C > 0$, where $\Delta E_C = E_{C,2} - E_{C,1}$ (that is, $X_1 > X_2$). If $J_{n,2}$ and $S_{n,2}$ are the electron

current density and electron energy flux density entering material 2, $J_{n,1}$ and $S_{n,1}$ are the electron current density and electron energy flux density leaving material 1, the interface condition can be written as: [12]

$$J_{n2} = J_{n1} \quad 3.6$$

$$J_{n2} = a_n q[\, v_{n,2}\, n_2 - \frac{m_{n,2}}{m_{n,1}} v_{n,1} n_1 \exp\left(\frac{\Delta E_c}{kT_{n,1}}\right)] \quad 3.7$$

$$S_{n2} = S_{n,1} + \frac{C_n}{q} J_{n,2} \Delta E_c \quad 3.8$$

$$S_{n2} = -b_n \left[v_{n,2}\, n_2 kT_{n,2} - \frac{m_{n,2}}{m_{n,1}} v_{n,1} n_1 kT_{n,1} \exp\left(\frac{\Delta E_c}{kT_{n,1}}\right)\right] \quad 3.9$$

Where the 'emission velocities' are defined as:

$$v_{n,i} = \sqrt{\frac{kT_{n,i}}{2\pi m_{n,i}}} \quad 3.10$$

Similar equations for the hole thermionic current and hole thermionic energy flux are presented below:

$$J_{p2} = J_{p1} \quad 3.11$$

$$J_{p2} = a_p q[\, v_{p,2}\, p_2 - \frac{m_{p,2}}{m_{p,1}} v_{p,1} p_1 \exp\left(\frac{\Delta E_c}{kT_{p,1}}\right)] \quad 3.12$$

$$S_{p2} = S_{p,1} + \frac{C_p}{q} J_{p,2} \Delta E_c \quad 3.13$$

$$S_{p,2} = -b_p \left[v_{p,2}\, p_2 k T_{p,2} - \frac{m_{p,2}}{m_{p,1}} v_{p,1} p_1 k T_{p,1} \exp\left(\frac{\Delta E_c}{k T_{p,1}}\right)\right] \quad 3.14$$

Where the ‘emission velocities’ are defined as:

$$v_{p,i} = \sqrt{\frac{kT_{p,i}}{2\pi m_{p,i}}} \quad 3.15$$

3.4 Material Parameter Models

Many properties of the materials are important for device modeling such as energy bandgap, the effective mass, mobility, saturation velocity, and recombination lifetimes. These parameters are typically dependent on the local concentration of the dopants and the temperature as well as the composition. Material models are needed for device modeling that incorporate these effects and are briefly discussed here. [12]

3.4.1 MOBILITY MODEL

The carrier mobility is a parameter that characterizes the drift motion of the carriers in the presence of an electric field. The electrons and holes are accelerated by electric fields, but lose momentum because of various scattering process involving lattice vibrations, impurity ions,

material interfaces and other imperfections. The effects of these microscopic phenomena are averaged and lumped together into the macroscopic parameter called the mobility, which is a function of the local electric field, doping concentration, and temperature. Though a variety of models are available for characterizing the mobility's behavior in low and high electric fields, we use two empirical models that are widely used. These models arefurther discussed as under: [12]

1) Constant Mobility Model and doping dependent Model

2) Electric field dependent mobility model

3.4.1.1 Constant Mobility Model

This model is used for intrinsic semiconductors and is dependent upon lattice temperature only. The affect of phonon scattering in semiconductor on mobility is described in equation 3.7.

$$\mu_{const} = \mu_L \left(\frac{T}{300\text{K}} \right)^{-\zeta} \qquad 3.16$$

where

μ_L is the mobility due to bulk phonon scattering

ζ is constant

And for Doping Dependent model following relations are used,

$$\mu_{dop} = \mu_{min} + \frac{\mu_d}{1 + \left(N_{tot} / N_0 \right)^A} \qquad 3.17$$

with

$$\mu_{min} = A_{min} \cdot \left(\frac{T}{300\text{K}} \right)^{\alpha_m}, \quad \mu_d = A_d \cdot \left(\frac{T}{300\text{K}} \right)^{\alpha_d}$$

and

$$N_0 = A_N \cdot \left(\frac{T}{300\text{K}} \right)^{\alpha_N}, \quad A = A_a \cdot \left(\frac{T}{300\text{K}} \right)^{\alpha_a}$$

T is the temperature in degrees Kelvin

N_{tot} is the total number of carrier concentration

A_{min} , A_d , A_N and A_a are the Constant

μ_d and μ_{min} are the mobilites

3.4.1.2 Electric Field dependent Mobility Model

As the electrons and holes are accelerated by the electric field, their drift velocities initially increase linearly. However, these velocities begin to saturate at higher electric fields ~10^5 V/cm. So the mobility becomes a function of the electric field strength. The following expression is an empirical one widely used to describe the mobility's variation between low and high electric fields.

$$v_{sat} = \left[A_{vsat} - B_{vsat} \left(\frac{T}{300K} \right) \quad v_{vsat} > v_{sat,min} \right] \qquad 3.18$$

$$v_{sat} = \left[v_{sat,min} \; otherwise \right]$$

Here Vsat are the saturation velocities.

A_{vsat} and B_{vsat} are the saturation velocities for electrons and holes.

3.4.2 Generation Recombination

In generation and recombination process, electrons and holes either appear or vanish. In generation process charge carriers are transferred from valance to conduction, trap level to conduction and vice versa in the recombination process. To explain the physical behavior of generation and recombination process, different models are described below.

3.4.2.1 Shockley-Read-Hall (SRH) recombination

Generation–recombination processes are processes that exchange carriers between the conduction band and the valence band. They are very important in device physics, in particular, for bipolar devices. [12]

The process as a two-step transition of an electron from the conduction band to the valence band or as the annihilation of the electron and hole, which meet each other in the trap. We will refer to this process as Shockley-Read-Hall (SRH) recombination as shown in Figure 3.2

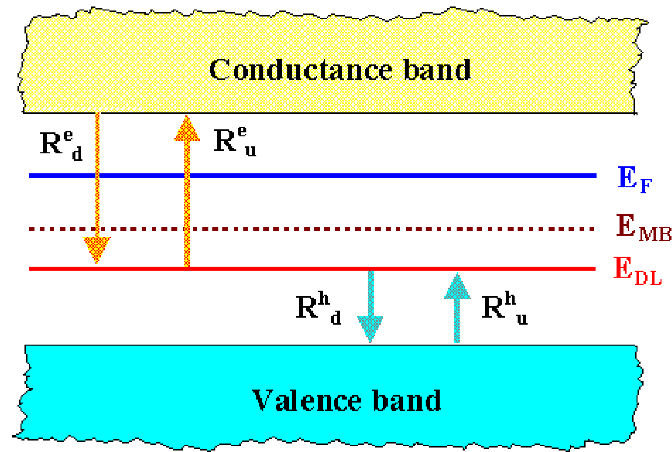

Figure 3.2 SRH Recombination Process [28]

The duration the electron hole pairs remain without recombining determines their lifetime in the material. It is an important parameter because it can influence the current gain in an HBT. TCAD synopsys implements carrier lifetime modeling by using the Shockley- Read-Hall (SRH) recombination model where the lifetime is dependent on the impurity concentration

In Sentaurus Device the following form is implemented

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \quad 3.19$$

$$n_1 = n_{i,eff} \exp(\frac{E_{trap}}{kT}) \quad 3.20$$

$$P_1 = n_{i,eff} \exp(\frac{-E_{trap}}{kT}) \quad 3.21$$

Here Etrap is the difference between the defect level and intrinsic level.

$n_{i,eff}^2$ is intrinsic carrier density

τ_p ,τ_n are the trap time for electron and holes

kT is the thermal Energy

3.4.3 MATERIAL PROPERTIES OF InAlAs/InGaAs/InP

Summarized in Table 3.1 are the energy bandgaps and band discontinuities for the InP/InGaAs and InAlAs/InGaAs heterojunctions compared with those for the AlGaAs/GaAs system (Refrence). While the ratio of valence to conduction band discontinuities is nearly the same for the InAlAs/InGaAs and AlGaAs/GaAs material systems, the magnitude of the conduction band discontinuity for the former is larger so that electron back injection into the emitter is further suppressed thereby enhancing the maximum emitter injection efficiency and possibly the current gain for the InAlAs/InGaAs npn HBT. For the InP/InGaAs system, the conduction band discontinuity is nearly the same as that for AlGaAs/GaAs. In practice, the current gain is frequently limited by recombination in the quasi-neutral base for npn InP-based HBTs. InAlAs/InGaAs and InP/InGaAs heterojunctions, the valence band discontinuities are larger (0.24 and 0.34 eV, respectively) than for the AlGaAs/GaAs case (0.15 eV). This contributes to a larger spike in the valence band, which can block the injection of holes from the emitter into the base and require a larger turn-on voltage. As a result, grading of the emitter-base junction may be important to ensure sufficient hole injection into the base and an adequate emitter injection efficiency. As is the case for the npn InP-based HBT’s [7, 1]. The smaller energy bandgap for the

Energy BandGaps and Band Discontinuities				
HETEROJUNCTION	**E_G (eV)**	**ΔE_c (eV)**	**ΔE_v (eV)**	**ΔE_v (eV)/ΔE_c (eV)**
InP/InGaAs	1.35/0.76	0.25	0.34	58/42
InAlAs/InGaAs	1.48/0.76	0.48	0.24	33/67
AlGaAs/GaAs	1.86/1.42	0.28	0.15	35/65

Table 3.1 Energy Band Gaps and Band Discontinuities [7, 1]

InGaAs gives a lower turn-on voltage than for the GaAs-based npn HBT, but also a smaller breakdown voltage.

Table 3.2 shows a summary of important parameters for the InP, InAlAs, and InGaAs materials assembled from the literature [7, 1] and used in the simulations. As can be seen, the hole effective masses are a factor of six to ten larger than those for the electrons so that the hole mobilities are correspondingly reduced. More specifically, the larger hole effective mass will decrease the hole minority carrier diffusion length in the base thereby reducing the base transport

Parameter	Symbol	InP	InGaAs	InAlAs
Permittivity	$\varepsilon_r / \varepsilon_o$	12.35	13.88	12.30
Energy Gap	E_g (eV)	1.35	0.75	1.47
Electron affinity	χ (eV)	4.37	4.58	4.1
Electron effective mass	m_n^*/m_o	0.077	0.041	0.075
Hole effective mass	m_p^*/m_o	0.50	0.47	0.47
Light hole	m_{lh}^*/m_o	0.12	0.05	0.09
Heavy hole	m_{hh}^*/m_o	0.56	0.46	0.58

Table 3.2 Summary of materials parameters [8]

factor and current gain. It will also increase the base transit time and degrade the transistor's cutoff frequency. In addition, the lower majority carrier hole mobility in the emitter and collector will increase the corresponding series resistances. However, the small electron effective mass gives rise to large majority carrier electron mobility in the base that reduces the base resistance which contributes to a higher power gain and maximum frequency of oscillation.

The carrier mobilities are known to be strong functions of the doping level. To enable the study of tradeoffs in device design of the doping level in each region, the doping dependence of the carrier mobilities was included in each of the material libraries. Summarized in Table 3.3 and Table 3.4 are empirical fits of the electron and hole mobilities dependence on doping to experimental reports in the three materials. The electron mobilities for InP and InAlAs are included in the table for completeness and comparison of the pnp transistor with the npn device. Where Nc describes the doping density above which ionized impurity scattering becomes dominant. As expected, due to the larger hole than electron effective masses in these InP-based materials, the hole mobilities at low doping are more than an order of magnitude less than the corresponding electron mobility. No distinction was made here between majority and minority carrier mobilities for these InP-based materials due to lack of sufficient data, though a significant difference has been reported for the GaAs material system. Recently, Betser and Ritter have reported a measurement of the minority carrier electron mobility in InGaAs of 3400 cm^2/V s at a doping level of 3.4×10^{19} /cm^3, which is in good agreement with the fit in Table 3.3 and Table 3.4.

ELECTRON				
PARAMETER	**UNIT**	**Inp**	**InGaAs**	**InAlAs**
μ_{max}	cm^2/V sec	4917	11,599	4,226
μ_{min}	cm^2/V sec	0	3,372	220
N_c	1/cm^3	$6.4x10^{17}$	$8.9x10^{16}$	$1.5x10^{14}$
α		0.46	0.76	0.27
V_s	cm/sec	$9.2x10^6$	$6.0x10^6$	$8.0x10^6$

Table 3.3 SUMMARY OF MOBILITY MODEL PARAMETERS [8]

Hole				
PARAMETER	**UNIT**	**Inp**	**InGaAs**	**InAlAs**
μ_{max}	cm^2/V sec	151	331	75
μ_{min}	cm^2/V sec	20	75	40
N_c	1/cm^3	$7.4x10^{17}$	$1.0x10^{18}$	$3.8x10^{17}$
α		0.96	1.37	0.79
V_s	cm/sec	$6.6x10^6$	$4.5x10^6$	$3.0x10^6$

Table 3.4 SUMMARY OF MOBILITY MODEL PARAMETERS [8]

3.5 BAND DAIGRAM AND EPITEXIAL STRUCUTRE

Table 3.5 shows the epitaxial structure of Double heterojunction bipolar transistor along with its doping profile and also the layer thicknesses. Base is highly doped which is 4e+19 cm^{-3} which helps for high frequency devices. Between base and emitter junction spacers layer which is unintentionally doped.

To reduce the complete elimination of current blocking, PN dipole doping is introduced which helps to electrons injection from base to collector and helps to increase in current gain.

LAYER	MATERIAL	THICKNESS (A)	DOPING cm^{-3}
Cap 1	InGaAs	800	2e+19(n)
Cap2	InAlAs	800	2e+19(n)
Emitter	**InAlAs**	**500**	**5e+17(n)**
Spacer	InGaAs	100	
Base	**InGaAs**	**450**	**4e+19 (p)**
SetBack	InGaAs	750	1e+16(n)
Diopole-Ptype	InGaAs	100	4e+18(p)
Dipole-Ntype	InAlAs	100	4e+18 (n)
Collector	**InAlAs**	**1000**	**1e+16(n)**
Collector2	InAlAs	500	1e+19(n)
Subcollector	InGaAs	3500	1e+19(n)
Buffer	InGaAs	300	
Substrate	InP	500	

Table 3.5 Epitaxial Structure of Double Heterojunction bipolar Transistor [1], [7]

The equilibrium band diagram shown in figure 3.2 is simulated with a SYNOPAYS TCAD 2D physical simulator. Abrupt Change in BE junction is help to accelerate electron and also help to reduction in current blocking. Spacer layer should be considering being doped 10% of the base doping i.e. 4×10^{18} cm^{-3}. You can see in band diagram band banding even on the base side of BE junction.

In order to ensure complete elimination of current blocking even at large values of collector current, an InGaAs setback of thickness 750 Å between base and collector and a dipole doping of 4×10^{18} cm^{-3} across the BC junction are used. These represent optimum values as lower or higher values leading to either incomplete elimination of current blocking or premature

breakdown voltage of the devices as evidenced by an extensive study of wafer growth and 2D physical simulations undertaken by the authors.

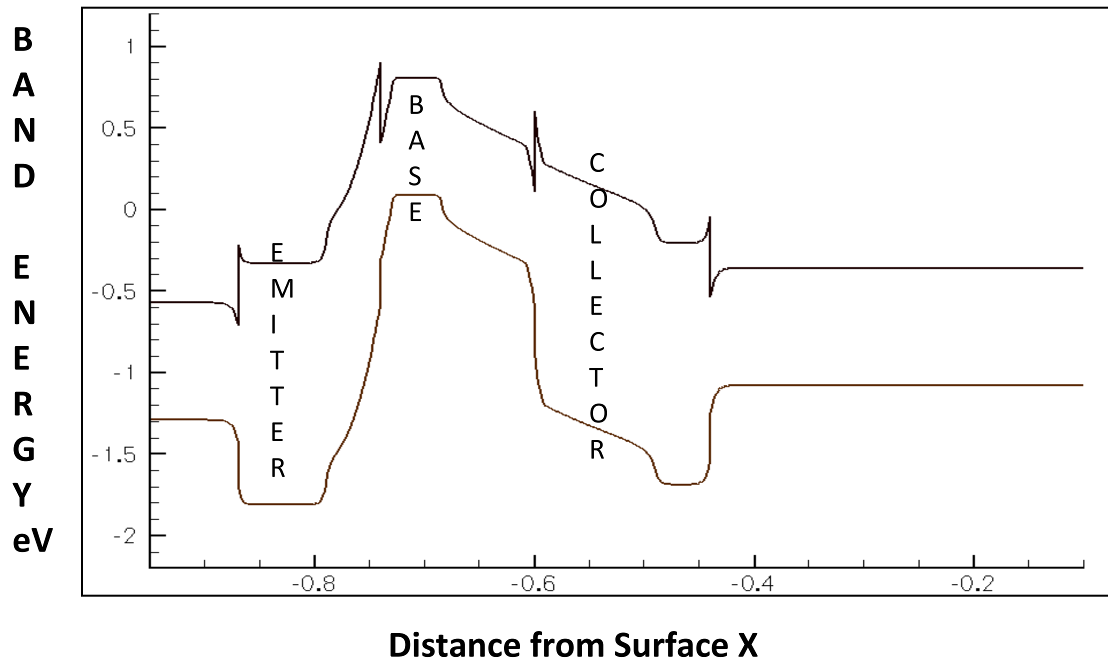

FIGURE 3.3 Simulated conduction band and valence band profiles for InAlAs/InGaAs/InAlAs with 450Å base width and no applied biases

CHAPTER FOUR: RESULTS AND DISCUSSION

4.1 Introduction

In this chapter, the structure of InAlAs/InGaAs/InAlAs double heterojunction bipolar transistor was modeled, simulated and analyzed using the commercial simulator Synopsys TCAD. We have modeled its structure using TCAD tool called Structure Editor and finalize its meshing using TechPlot. Physical model and its biasing were done in Sentaurus Device. In previous section we have discussed physical model briefly and in this chapter we shall discuss results and will compare these results with measured results. In this chapter we shall discuss DC and AC analysis of double heterojunction bipolar transistor, also examine transistors performance. We have compared our simulated results with measured results, which help in establishing the reliability of simulation. After that we also modify our device structure for better performance of DHBTs.

4.2 Software Description

The Synopsys tcad is very flexible software for simulating any semiconductor devices. We can check electronic performance of two dimensional device structure which is composed not only of semiconductors but also insulators, conductors and terminals. Using Synopsys Tcad, not only we can check electronic behavior including AC and DC behavior of a device but we can also analysis internal device parameter distribution, which includes band energies, Recombination process, electrostatic charges, capacitance, and electron and hole concentration. Synopsys Tcad also flexible at interface physics which helps us to study heterostructures metal semiconductors

contacts. This helps to simulate virtually accurate semiconductor device, this helps us to study briefly leakage current, trapped charges and device parasitic capacitance. [12]

TCAD Synopsys includes sub framework SENTAURUS Work Bench having different types of modules including Device structure editor. Device structure editor is a 2-D device simulator for III-V material Devices. It has also Graphical User Interface (GUI) called TECHPLOT and INSPECT VIEW from which we can see IV characteristics of a device also can see electronic properties of a device. Device simulation and to find out its characteristics, the following methodology is followed, Firstly the 2-D device structure is model in Device editor, in the same tool the doping concentration is defined, also the thickness of the device and its correct dimensions and electrical contacts. Meshing of a device is also defined in structure editor. After modeling the Device structure, Physical models are incorporated this depends on each and other parameters. i.e Carrier mobility on doping level. Suitable physical models are then selected for simulation including Recombination (Auger, SRH), Mobility (Doping Dependent, Temperature dependent). After that bias conditions are applied performing AC, DC simulation. Numerical technique for solving the differential equation at mesh grid points is also specified. Process of simulation can be summarized as follows, [12]

1. Run Sentaurus WorkBench
2. Physical structure of DHBT is described
3. Physical models are specified
4. Input bias conditions are specified
5. Output characteristics of a device

Figure below are the flow chart of process of simulation.

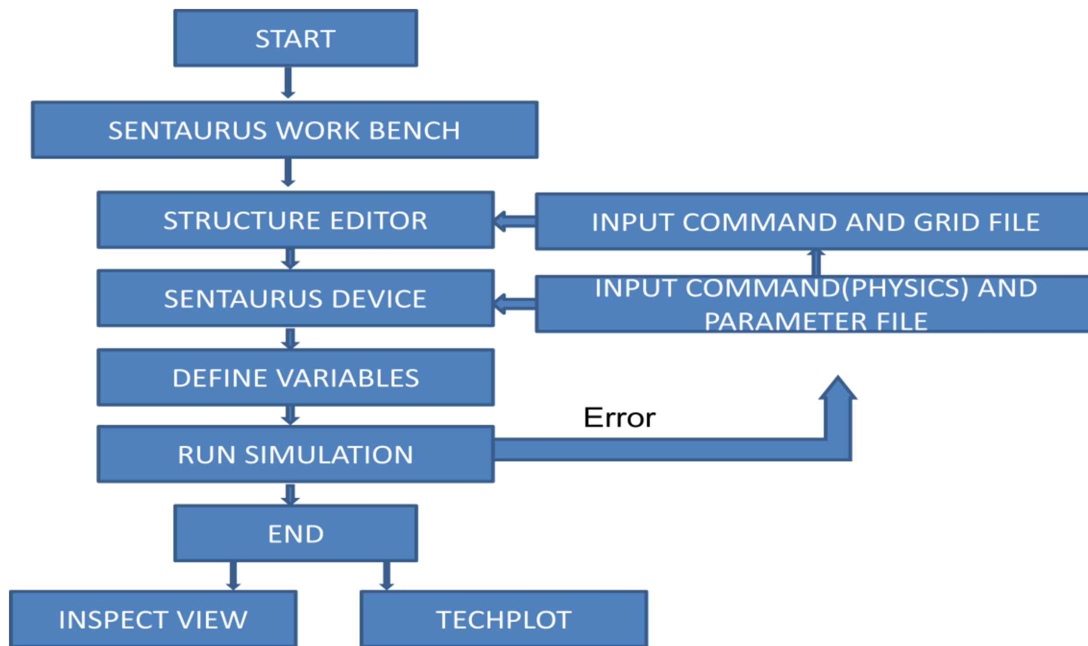

Figure 4.1 Device Simulation Flow Chart

4.2.1 DHBT Structure and Mesh specification

Physical structure of a device which is simulated initially and also specified it along with its material regions and properties; this includes specifying the composition, doping and thickness of each region and the size and location of each of the device contacts. After building up the device structure MESH of the device is specified over the device structure, 2-D meshing of the device is specifying in x and y direction, it is done by TECHPLOT. MESHING of the device is very important, MESH are the nodes specified at which the simulator calculates and solve the device equation and device parameters such as electric potential and carrier concentration. Mostly the device characteristics is determined across the junction and interface, so it is very important mesh of the device across these regions should be accurate, so across the regions

including Base-Emitter and Base-Collector where there is rapid change in potentials and carrier concentration, MESHING of the device is really denser. Figure 4.2 shows the MESH of the device. If there is excessive number of grid points over the device structure, so simulator will take too much time for simulation, so balance should be placed in it. Mesh should not be too much dense because it may cause convergence problem for the equation during simulation. The optimum way to defining the mesh is, it should provide the accurate or reasonable results and also simulator solves the equation without any convergence problem.

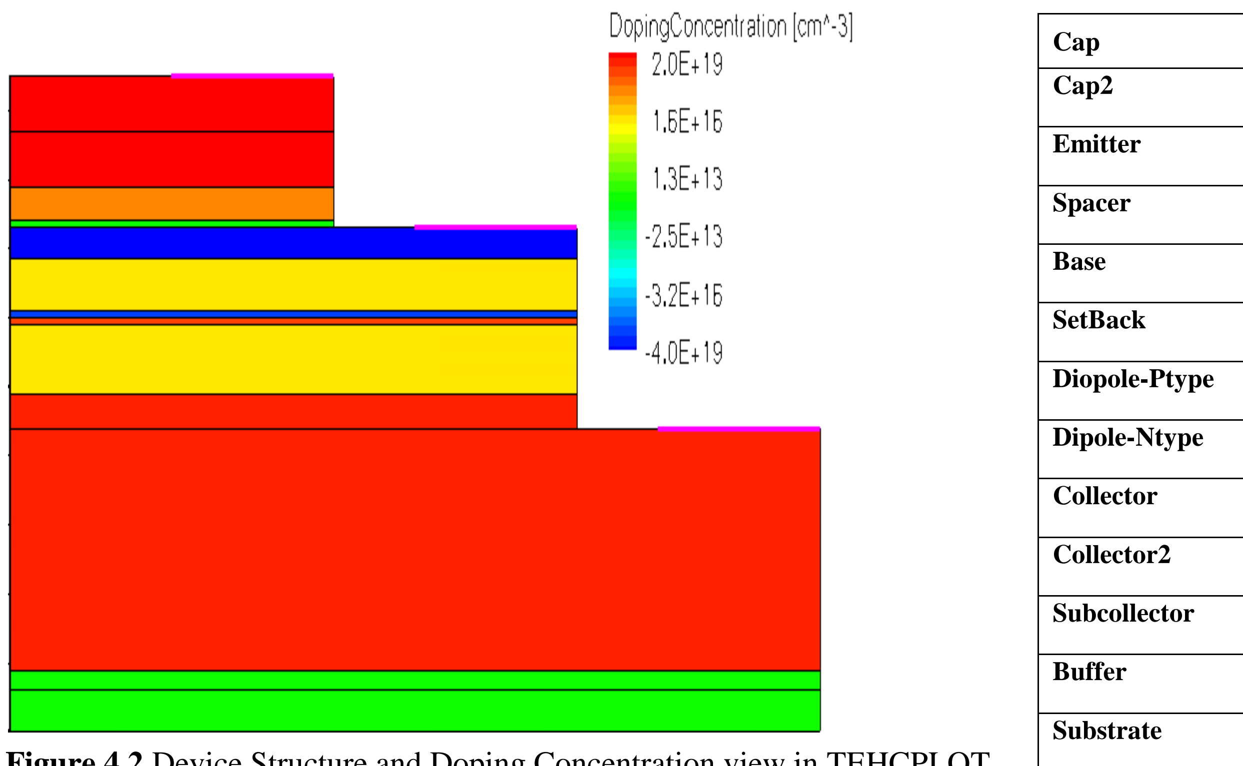

Figure 4.2 Device Structure and Doping Concentration view in TEHCPLOT

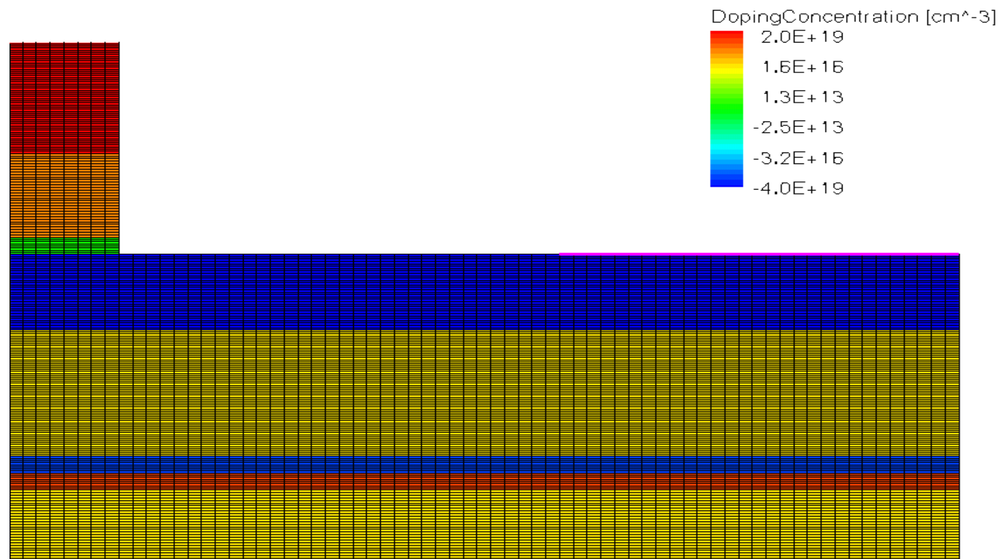

Figure 4.3 Meshing view in TechPlot of DHBTs

4.2.2 Physical Models

In chapter 3 we have discussed physical models in detail. Device characteristics are calculated with the help of these physical models. Type of the model depends on the type of the device such as for optical devices, optical models are defined in physics section in Sentaurus Device. In our case in DHBTs the most important physical models are mobility temperature and doping dependent. These models are activated Sentaurus Device model in physics section with the name of Mobility (DopingDependence TempDep). For the study of carrier recombination and the life time of the carriers across the junction, SRH model is activated for carrier recombination in physics section with the parameter name SRH (DopingDep TempDep). In order to calculate the breakdown of the device, Avalanche model is used, this models is activated also in Physics

section in Sentaurus Device. The parameter for the avalanche model which is mentioned in the physics section is eAvalanche for the electrons and for hole hAvalanche statements are used.

4.3 Band Diagram

High frequency performance of a device is due to the high field effects in base region. High velocity of the electron which causes the electron ballistic ally injected from base region to collector region. The ballistic effect is due to the small dimension of the device, internal high field and the conduction band alignment of base and collector region as shown in band diagram Figure 4.4. Because of these properties electron injected form base to collector have kinetic energy more than kT and its effective temperature is larger than the lattice temperature T. Emitter have wider band gap than base region, there are less collisions in the base region. When the electron moves in to base region from the conduction band spike, they enter with excessive energy and velocity. Ballistic effects found more effectively when base region is reduced. Base region is much smaller in all devices because electron collisions are less, and it get large transport velocity. In our case the base thickness is 450 Å.

Due to the wide band gap between base and emitter region the hole injection is reduced from base to emitter region, it also reduced the capacitance across the base emitter junction. Similarly there is also wide band gap between base and the collector region, which also helps to reduce the hole injection for base region to collector region. So it helps the electron move from base to collector region and also helps in large current. Due to this reason base is highly doped which helps to achieve high frequency performance. From the Figure 4.4 there is a single heterojunction between the emitter and base region and there is also another heterojunction

between the base and the collector region. PN dipole region helps in complete elimination of current blocking. Each PN dipole layers have thickness is 100 Å.

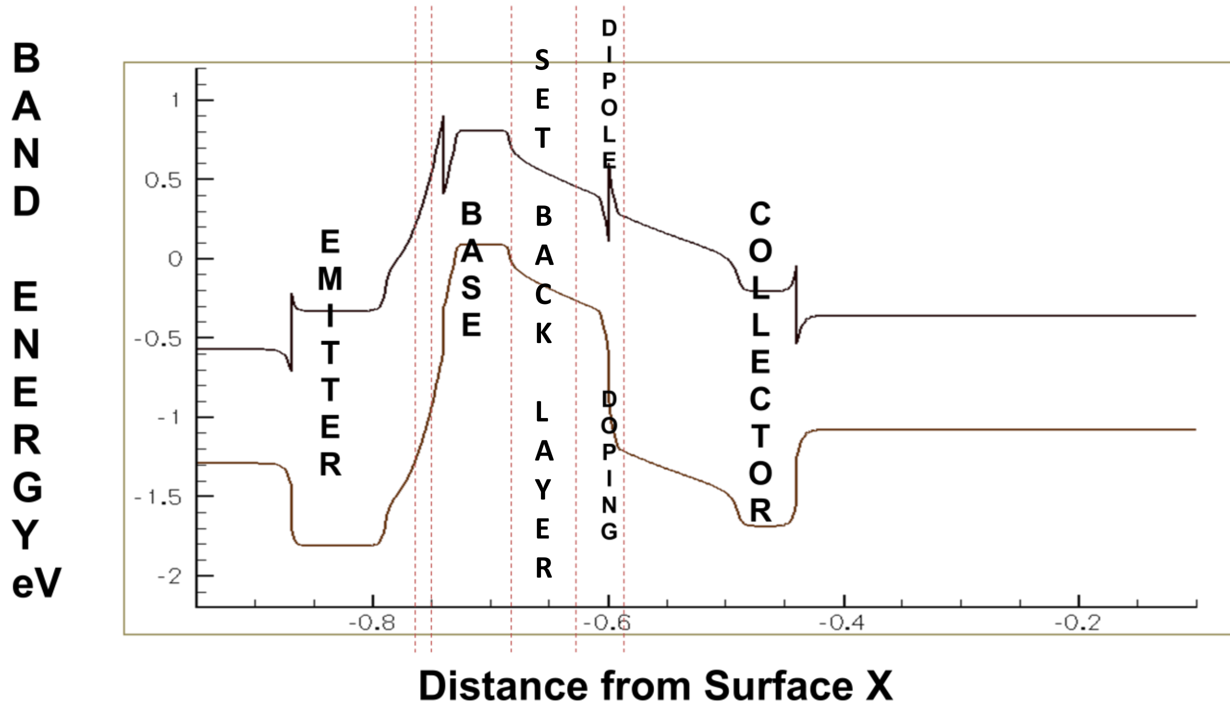

Figure 4.4 Band Diagram of InAlAs/InGaAs/InAlAs

In our device InAlAs/InGaAs/InAlAs DHBTs, from Figure 4.4 we can see that the conduction band of base region is higher than the conduction band of collector. We can conclude that the dominant transport mechanism through the base of InGaAs/InAlAs DHBT and the reason for impressive f_t and f_{max} performance is due the hot-electron effect in the base- collector space charge region.

4.3.1 Input bias and Output Extraction

Biased conditions and temperature parameters must be specified on each terminal of the device. Initially for biased conditions, DC supply is increased in small steps so that simulation proceeds without any convergence problem. After that the collector terminal and the base terminal swept with DC biasing so that Gummel plot can be plotted. Gummel plot is obtained as I_b and I_c versus Vbe. For AC analysis after initial solution of DC biasing is obtaining, frequency is then increased. Finally frequency is swept for calculating the cut of frequency of the device which will help in determination of device performance by calculating maximum frequency of the device.

4.4 Structure and modeling of InAlAs/InGaAs/InAlAs DHBT

The structure of the transistor which we are simulated is studied in Mohiuddin et al [1] , in which transistor is studied at different temperatures Mohiuddin et al [1]. Different transistor configuration is examined. The main reason for choosing their work as a bench mark is that they have reported a series of fabricated devices with increasing performance and different emitter area. In simulation we varied different base thicknesses and also spacer thickness of the device structure. We compared our simulation results with measured results of the transistor structure which is reported by Mohiuddin et al [1].

The epitaxial structure of npn DHBTs InAlAs/InGaAs/InAlAs is shown in Table 4.1. The device consists of heavily doped Base region with $4e10^{19}$ with thickness of 450 Å. Emitter region is less doped as compare to Base region and Emitter area is 1x5 μm^2 with thickness of 500 Å. In between Emitter region and Base region there is spacer layer which unintentionally dope region.

There is heterojunction between Emitter (InAlAs) and Base (InGaAs) regions, Emitter region is n doped region with $5e10^{+17}$ cm^{-3} concentrations. Collector region having 1000 Å layer thickness, and having doping concentration is $1e10^{+16}$, which is doped with n type species.

LAYER	MATERIAL	THICKNESS (A)	DOPING cm^{-3}
Cap 1	InGaAs	800	2e+19(n)
Cap2	InAlAs	800	2e+19(n)
Emitter	**InAlAs**	**500**	**5e+17(n)**
Spacer	InGaAs	100	
Base	**InGaAs**	**450**	**4e+19 (p)**
SetBack	InGaAs	750	1e+16(n)
Diopole-Ptype	InGaAs	100	4e+18(p)
Dipole-Ntype	InAlAs	100	4e+18 (n)
Collector	**InAlAs**	**1000**	**1e+16(n)**
Collector2	InAlAs	500	1e+19(n)
Subcollector	InGaAs	3500	1e+19(n)
Buffer	InGaAs	300	
Substrate	InP	500	

Table 4.1 Epitaxial Structure of Double heterojunction bipolar Transistor [1], [7]

In between the collector region and base region setback, PN dipole layers, this helps to reduce the current blocking. Thickness of Setback layer, which is also undoped region is 750 Å and P and N dipole region have thickness of 100 Å. Cap1 and Cap2 are heavily doped region which will behave like contact and similarly collector2 and subcollector are also heavily doped for Collector contact. The simulated structure is double mesa structure.

The Gummel plot for InAlAs/InGaAs/InAlAs is shown in Figure 4.5. In Gummel plot, we plot base and collector current as a function of V_{be} with V_{ce}=0. The simulated gummel plot in Figure 4.5. The maximum collector current of I_C is about 100mA and the maximum I_b current is about 10mA.

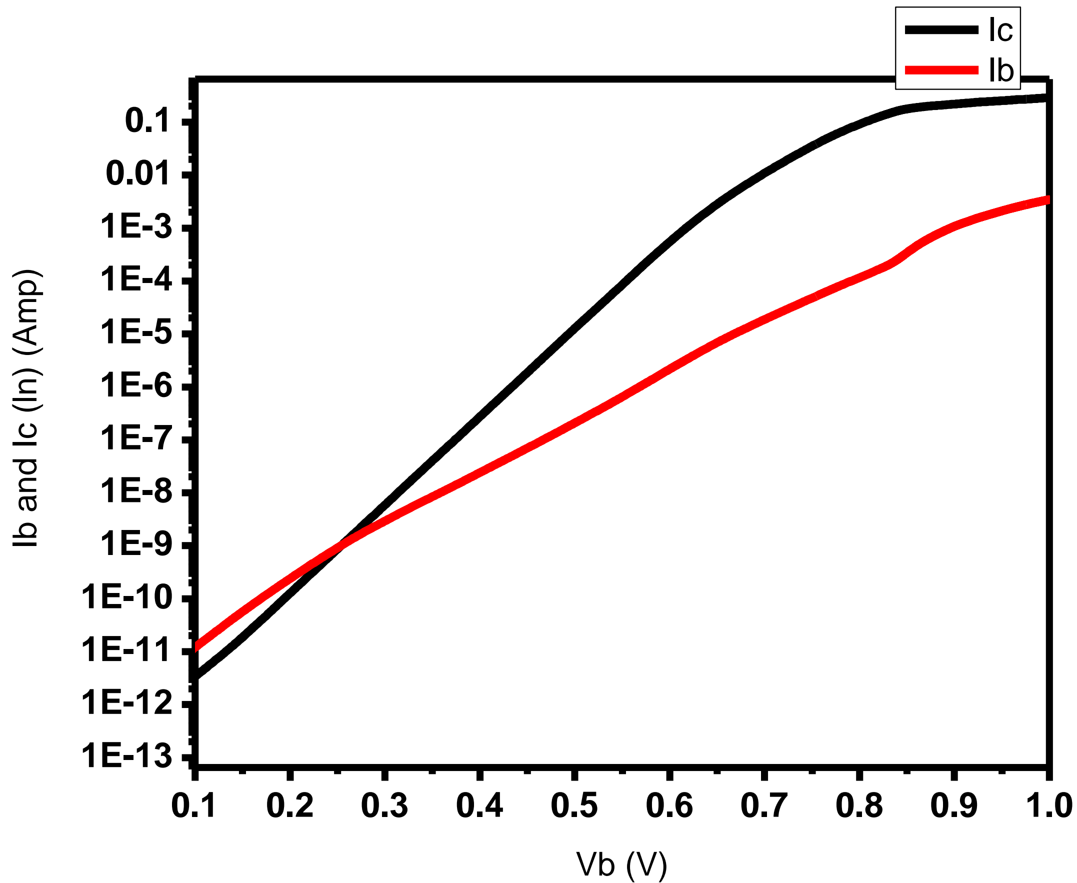

Figure 4.5 Simulated Gummel plot characteristics of InAlAs/InGaAs/InAlAs structure the device structure described in Figures 3.4 and 3.3 for Vcb=2.0 V

4.5 IV Characteristics

The common emitter characteristics of InAlAs/InGaAs/InAlAs double heterojunction bipolar transistor are show in Figure 4.6. Common emitter characteristics of DHBTs have gain ß=41

with break down voltage is 5V at 300K and its turn on voltage is 0.4V. This transistor is fabricated at base width 450 Å, and collector layer thickness is 1000 Å. In Figure 4.6 the green lines are measured results of double heterojunction bipolar transistor. The IV curves are taken in steps of 10µA base current. Similarly the red curves are simulated having current gain is ß=39, and the break down voltage is about 6V. Simulation is also done with same base thickness of 450 Å, collector layer thickness is 1000 Å and the emitter is is 1x5µm^2. As you can see the simulated results and the measured results are well incorporated with each other and simulated device have turn on voltage is 0.35V

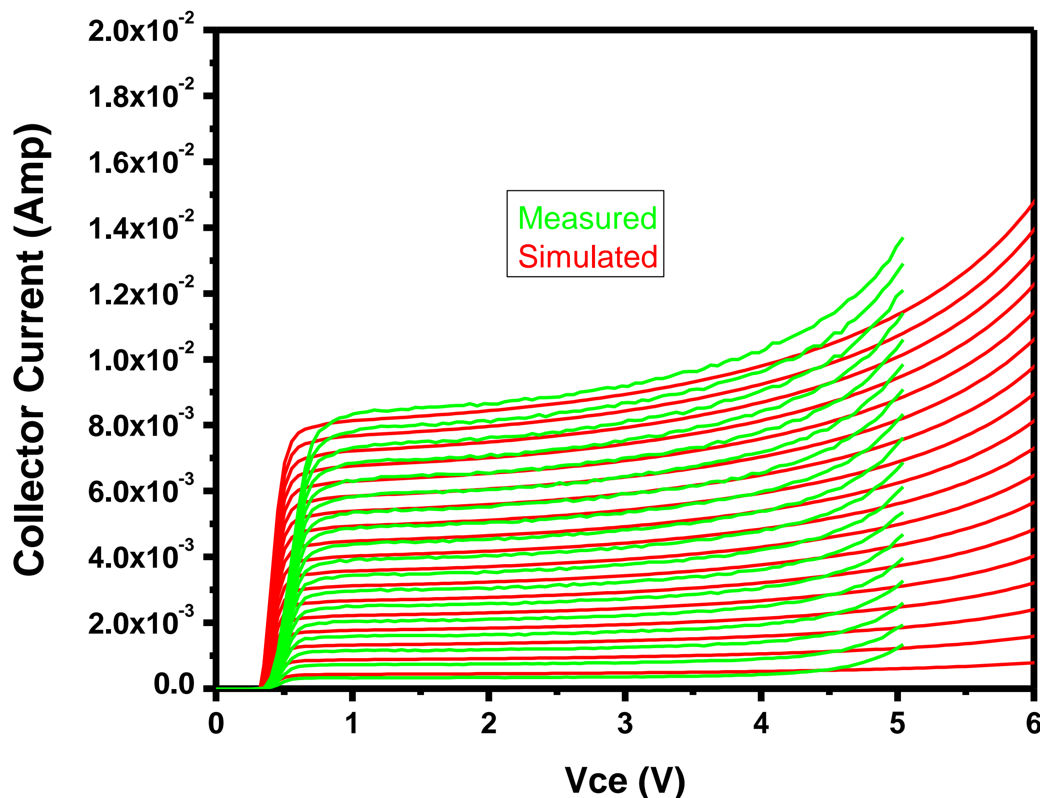

Figure 4.6 Common Emitter characteristics of DHBTs at 300K, with Ib step size 10µAmp

Similarly common emitter characteristics of InAlAs/InGaAs/InAlAs double heterojunction bipolar transistor at temperature 400K are show in Figure 4.7. Common emitter characteristics of

DHBTs have gain ß=44 with break down voltage are 4.5V at 400K, and its turn on voltage is 0.4V. This transistor is fabricated at base width 450Å, and collector layer thickness is 1000Å. In Figure 4.7. The green lines are measured results of double heterojunction bipolar transistor. The IV curves are taken in steps of 10μA base current. Similarly the red curves are simulated having current gain is ß=43, with break down voltage is about 5.5V. Simulation is also done with same base thickness of 450Å, collector layer thickness is 1000Å and the emitter is is 1x5μm^2. As you can see the simulated results and the measured results are well incorporated with each other. At temperature 400K break down comes early than 300K because at higher temperature electron gain thermal energy and current increasing rapidly. Simulated device have turn on voltage of device is 0.35V

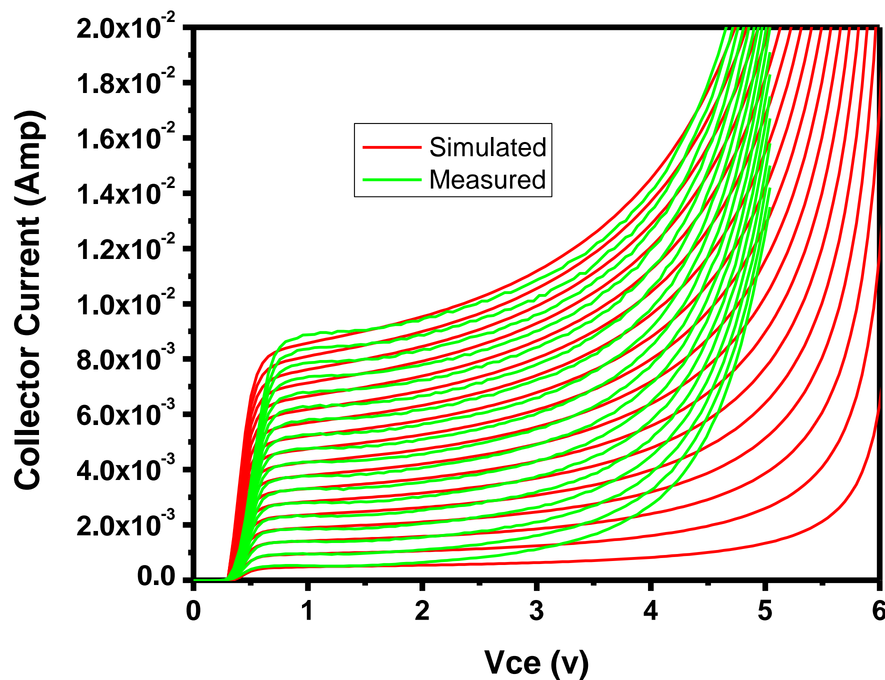

Figure 4.7 IV characteristics of DHBTs at 400k, with Ib current step size 10μAmp

Previously we have discussed IV characteristics of DHBTs and also studied individually BE and BC junction at different temperatures. Figure 4.6 shows the BC region, in simulation we swept

voltage at base contact from 0V to 1V, and collector region is grounded, and the emitter contact is disabled. The simulation is done at different temperatures varying from 250K to 400K; both simulated and measured results are shown in Figure 4.8. The Red lines show the measured or experimental results and the black lines shows the simulated results. From Figure 4.8, we can see that at temperature 250K the conduction of BC region starts from 0.3V in both measured and simulated, whereas when we increased its temperature the potential barrier decreasing and the conduction starts before 0.3V, at 400K the BC conduction starts at 0.1V. At higher temperature, electron gain more thermal energy and more electron hole pairs generated which cause the increasing in current and the potential barrier in between BC junction decreases. The temperature parameters are defined in Thermode Section in Sentaurus Device tool.

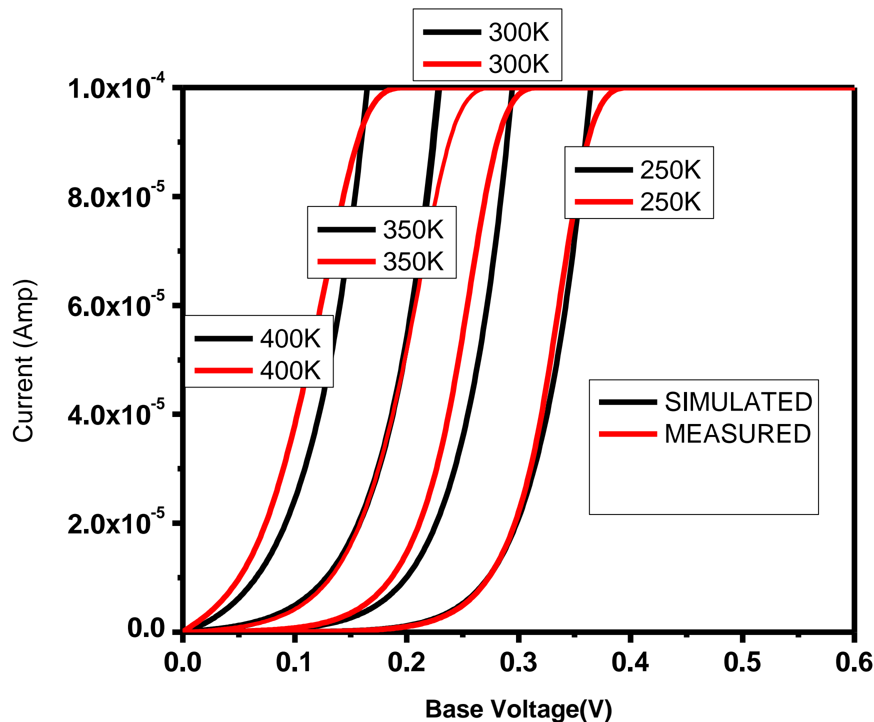

Figure 4.8 Base Collector Characteristics at different temperatures

Figure 4.9 shows the BE region, in simulation we swept voltage at base contact from 0V to 1V, and the emitter region is grounded, and the collector contact is disabled. This simulation is also done at different temperatures varying from 250K to 400K; both simulated and measured results are shown in Figure 4.9. The Red lines show the measured or experimental results and the black lines shows the simulated results. From Figure 4.9 we can see that at temperature 250K the conduction of BE region starts from 0.65V in both measured and simulated, similarly as we increased its temperature the potential barrier decreasing and the conduction starts before 0.65V, at 400K with BE conduction starts at 0.3V. At higher temperature electron gain more thermal energy and more electron hole pairs generated which cause the increasing in current and the potential barrier in between BE junction decreases. As we know that transistor have back to back two diodes but it behaves differently, these results show that forward biased region of both BE and BC region have different characteristics at different temperatures.

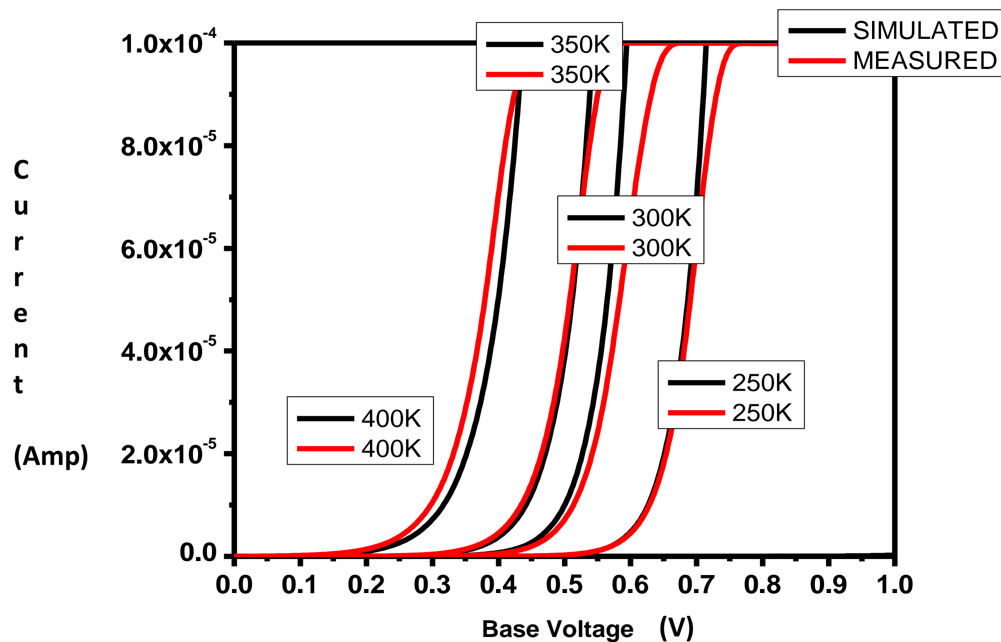

Figure 4.9 Base Emitter Characteristics at different temperatures

The frequency response of the current and power gain of the simulated structures are shown in Figure 4 for a device with a 450 Å thick base and 1x5 μm^2 emitter. The transistor shows a f_t=100GHz obtained by extrapolating the current gain and Mason's unilateral power gain, AC current gain being 40 dB. The simulated performance of the structure is shown in Figure 4. The simulated structure was biased at V_{BE}=0.8V and V_{CE}=2V, and frequency is swept from $1e10^{+5}$ to $1e10^{+12}$.

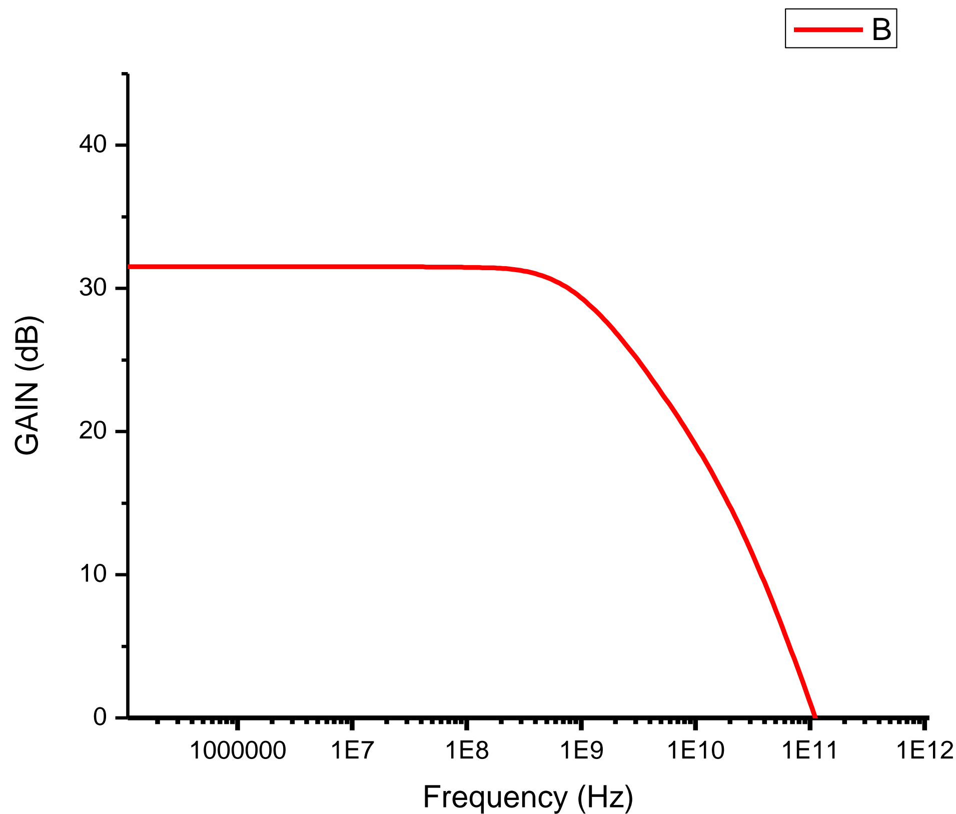

Figure 4.10 Cut off frequency of DHBT

4.7 Optimizing of InAlAs/InGaAs/InAlAs DHBTs

Some of the simulation results of the InAlA/InGaAs/InAlAs DHBTs were discussed in the previous section. In this section, we shall optimize the InAlAs/InGaAs/InAlAs DHBT structure, which was build in previous section, in terms of epitaxial layer thickness for better current gain. The optimization of parameters i.e., layer thickness, is a challenging one, since obtaining a better performance on one set of parameters, i.e. f_t doesn't necessarily mean optimum performance in terms of the other. We arrive at the best epitaxial design for maximizing f_t, power gain, and current gain by optimizing the conflicting effects of varying the epitaxial layer widths.

The semiconductor industry has been able to make impressive advances in technology, because it has been able to continuously improve the performance of its devices. Faster and more efficient devices owe their existence to improve in process technology that has facilitated the fabrication of devices with ever-smaller dimensions. For a III-V device to be more useful, maximizing its high frequency performance is a key factor. With this perspective in mind, we proceed to optimize the device structure, scaling the device's dimension in the vertical and horizontal directions to maximize f_t. The device's performance in terms of the current and power gain are also very important. This is particularly true for the kind of applications for which InAlAs/InGaAs/InAlAs DHBTs will be used, i.e. power amplifiers.

4.7.2 Optimizing Base Layer

The base region of the transistor is the most important layer for the DHBT, in the context that significant improvements in high frequency performance can be made by efficient design of the

base region. The f_T of a transistor is affected by the transistor base layer design mainly through the base transit time. If we reduce the base thickness, it will affect the current gain, for zero base thickness, there is no base region and contact, and so no bipolar transistor can be formed. As a result, from the f_t consideration alone, the goal is to make the base as thin as possible, keeping within the epitaxial processing capabilities. If we increase the current gain, it will affect the breakdown voltage of the device as well, so we should keep in mind a balanced trade-off needs to be made between the two parameters when deciding on the value of the base width.

From the table and the Figure4.11 below, the original base thickness is 45nm having current gain at 300K is 41 and 39 for measurements and simulations, respectively. As we reduce the base thickness from 45nm to 30nm the current gain increases from 39 to 74, but the break down voltage decreases. At 30nm base thickness having breakdown voltage is reduced from 6V to 4.5V. So we should increase our device gain without reducing our breakdown voltage of the device. Graph also shows the linear behavior of the current gain as we decrease the base thickness of the device from 45nm to 30nm.

BASE	GAIN
45nm	39
35nm	63
30nm	74

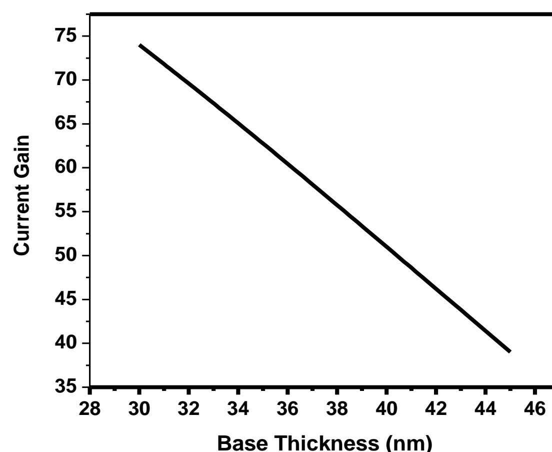

Figure 4.11 Plot of Base thickness versus Current Gain

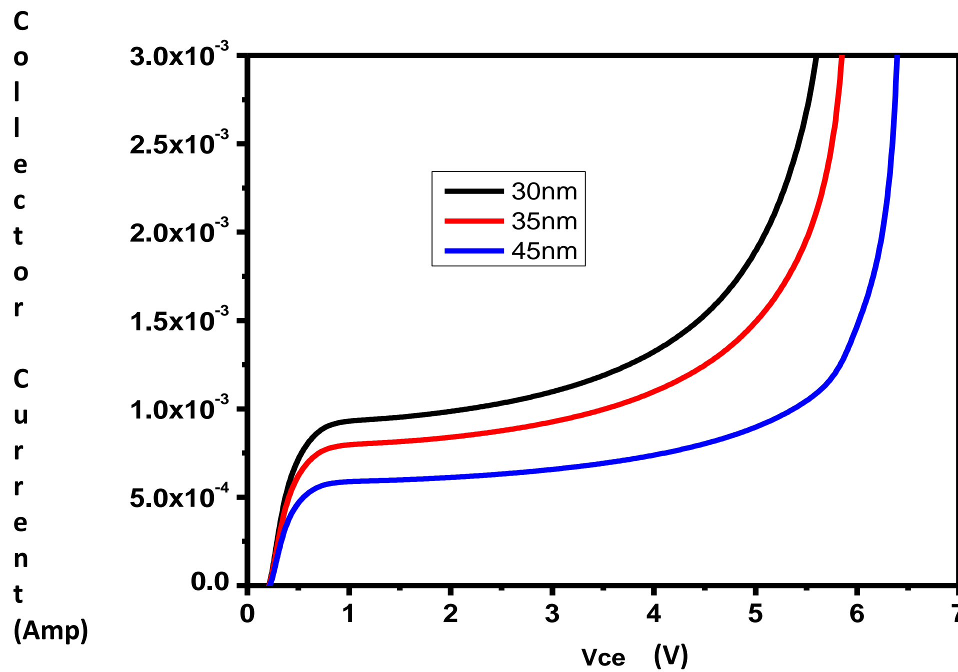

Figure 4.11 IV characteristic of Common Emitter having Different Base Thicknesses

4.7.2 Optimizing SETBACK Layer

After optimizing the gain of the device by changing the thickness of the base layer, Break down Voltage of the device is improved by varying the thickness of the SETBACK layer in the epitaxial structure of DHBTs. Figure 4.12 shows the different SETBACK layer thicknesses results, as we increase the thickness of the SETBACK layer the break down voltage increases, this shows that the electric field becomes weaker as increase in SETBACK region and more potential is required for break down. At 75nm thickness the break down voltage is 6V, as we increase the thickness of the SETBACK layer with the factor of 10nm the break down voltage

increases with factor of 0.4V. The maximum layer thickness which we can optimize is 100nm, above the thickness of 100nm the current of the device start decreasing, so 100nm is optimized thickness of the setback layer. Graph also shows the linear behavior between the variation in thicknesses and the break down voltage

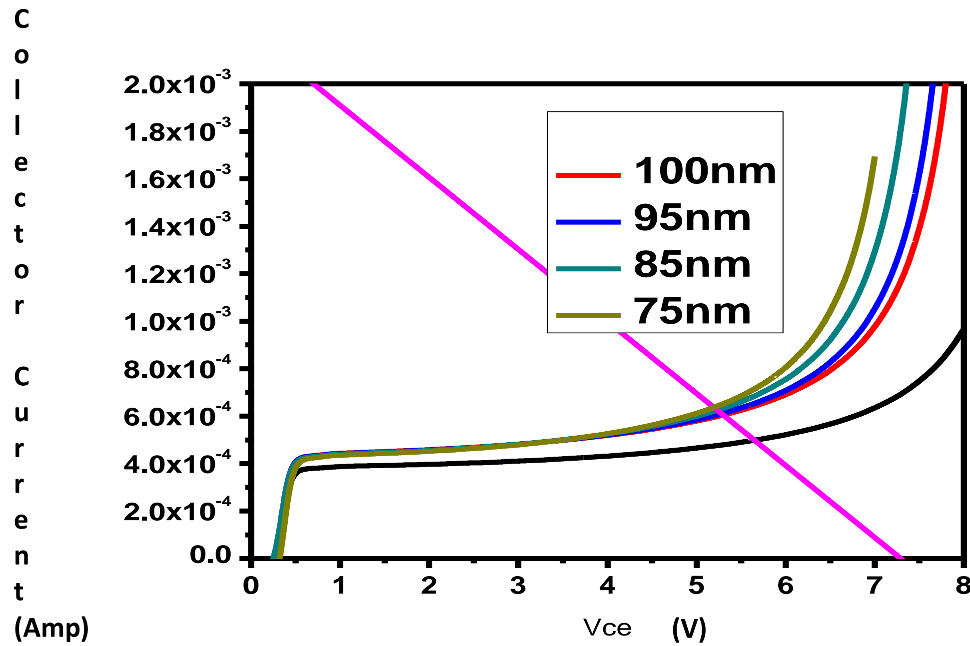

Figure 4.12 IV characteristic of Common Emitter having Different SETBACK layer Thicknesses

SETBACK	BREAKDOWN
75nm	6
85nm	6.4
95nm	6.8
100nm	7

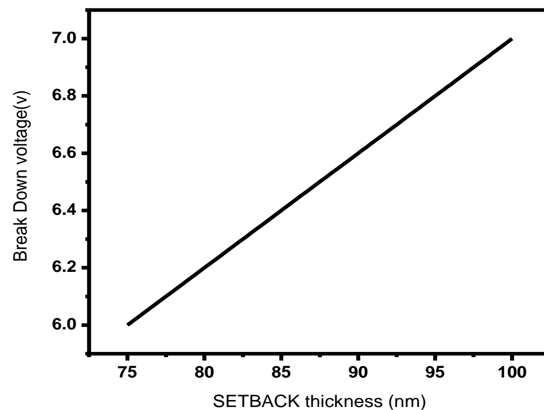

Figure 4.12 Plot of breakdown voltage with varying Setback layer thickness

4.8 Optimized Structure

The final InAlAs/InGaAs/InAlAs DHBT structure optimized for high gain performance is shown in Figure 4.9. This structure incorporates the best layer thickness values as determined from the simulations discussed in the previous sections. The changes to the transistor structure have been to the main active layers of the transistor. The design values for the contact layers and the sub-collector are the same as that of the original structure by [2]. Simulation was done at different temperatures from 300K to 400K as shown in Figure 4.14, the band diagram of the final optimized structure also shown in Figure 4.14. The IV characteristics of DHBTs show the improvement in gain without decreasing its break down voltage of the device.

LAYER	MATERIAL	THICKNESS (A)	DOPING cm^{-3}
Cap 1	InGaAs	800	2e+19(n)
Cap2	InAlAs	800	2e+19(n)
Emitter	**InAlAs**	**500**	**5e+17(n)**
Spacer	InGaAs	100	
Base	**InGaAs**	**300**	**4e+19 (p)**
SetBack	InGaAs	1000	1e+16(n)
Diopole-Ptype	InGaAs	100	4e+18(p)
Dipole-Ntype	InAlAs	100	4e+18 (n)
Collector	**InAlAs**	**1000**	**1e+16(n)**
Collector2	InAlAs	500	1e+19(n)
Subcollector	InGaAs	3500	1e+19(n)
Buffer	InGaAs	300	
Substrate	InP	500	

Table 4.2 Optimize Structure of Double heterojunction bipolar transistor.

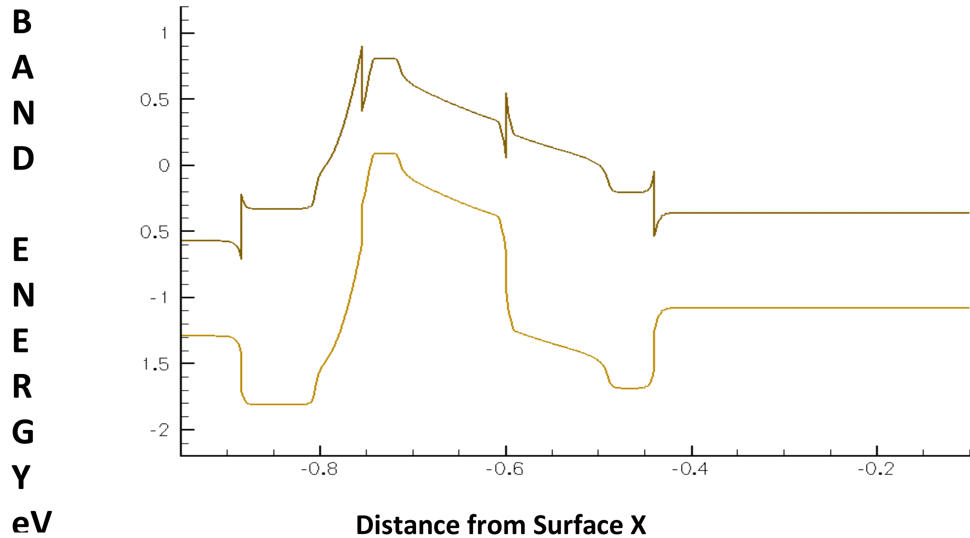

Figure 4.13 Energy Band Diagram of Optimize structure of DHBTs.

Optimize BASE	SETBACK LAYER
30nm	100nm

Table 4.3 Optimize value of Base and Setback layers

Figure 4.14 (a & b), are the common emitter IV characteristics, the following simulation is done at different temperatures i.e 300K and 400K, the red curves shows the optimize structure of DHBTs with base thickness 30nm with 100 nm SETBACK Layer and the blue curves shows the original characteristics of the device having 450nm base thickness with 750nm SETBACK layer. Figure 4.14 clearly shows the improvement in the current gain of the device and with Optimized device structure, the gain becomes ß=74.

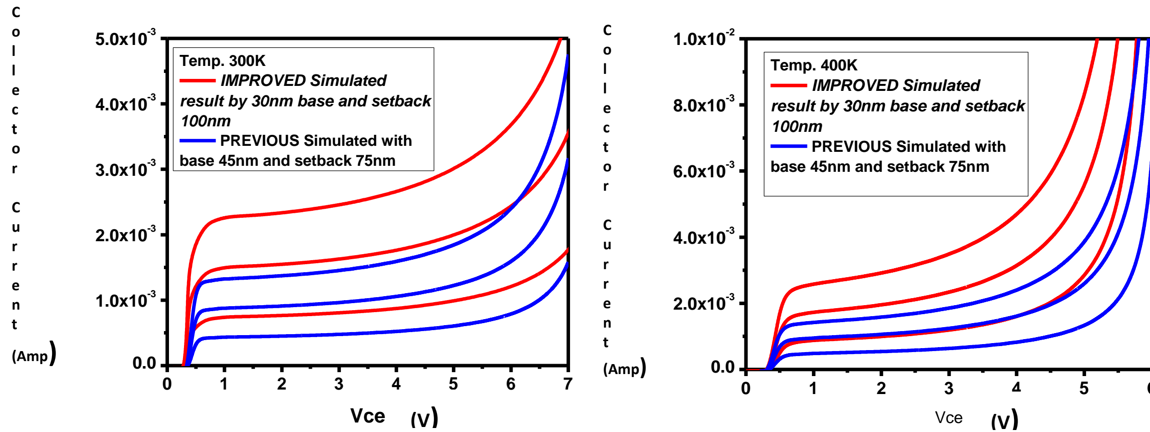

Figure 4.14 Common Emitter IV characteristics of optimized structure of **DHBT** at 300K and 400K

Conclusion and Future Work

In this work, we have investigated and simulated the performance of InAlAs/InGaAs/InAlAs Double Heterojunction Bipolar Transistors (DHBTs). InGaAs as a base in the NPN InAlAs DHBT bestows a huge advantage in terms of removing the collector blocking effect commonly found in other InAlAs-based DHBTs and also in enhancing the collector breakdown voltage. The simulation model for the transistor was developed, with its complete epitaxial structure, terminal contacts, doping, and device physics models, along with the necessary biasing. The material properties were researched in detail, such as the band energy gap, mobility, effective masses, carrier lifetime, and density of states and incorporated into the device model used for simulation.

In order to validate the transistor simulation model, we compared the simulation results with the experimental results of the fabricated device of InAlAs/InGaAs/InAlAs DHBTs. The simulated model had the same device structure[1], [7]. The common- emitter characteristics of the device were investigated and one of the unique features of this transistor is its low turn -on voltage. The

turn-on voltage of the simulated device matched the measured results with a turn-on voltage of 0.4V. For comparison of the common-emitter characteristics, the current values were properly scaled and high frequency performance of the simulated results being f_t =100 GHz. The common emitter characteristics are simulated at different temperatures and the performance of DHBTs is analyzed at different base current. Along with common emitter characteristics we have also studied BE and BC junction individually and also simulated it at different temperatures ranging from 250K to 400K.

Once we validated the transistor model, the DHBT structure is optimized to demonstrate improved in current gain performance. The effect of thickness of each layer including Base and SETBACK layer of the transistor were investigated. The optimized structure has a base layer at 30 nm and the SETBACK layer have 100nm with peak current gain becomes ß=74. The optimum values were chosen without compromising other performance measurements like the breakdown voltage.

The InAlAs/InGaAs/InAlAs transistors have a number of advantages as elucidated in earlier chapters, ranging from easy integration with optical transceivers to the simplicity of their fabrication. These advantages make it worthwhile to aggressively pursue the development of these devices in spite of stiff competition from other technologies[9]. Also, the low noise performance and the high linearity of the devices over a wide range of frequencies make these devices attractive in high growth.

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