Design and Analytical Modeling of a Complete Transmit Receive Module (TRM) for Applications in Active Microwave Sensors

By

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A Thesis Report Submitted in Partial Fulfillment of the Requirements for the Degree of
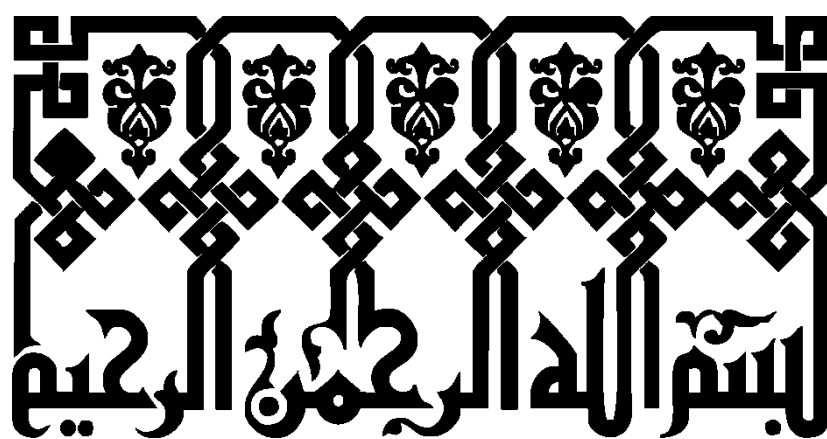
MASTER OF SCIENCE
in
COMPUTATIONAL SCIENCE and ENGINEERING
(MS-CS&E)

Research Center for Modeling and Simulation (RCMS)
National University of Sciences and Technology (NUST)
H-12 Sector Islamabad, Pakistan

September-8, 2011

بسم الله الرحمن الرحيم

In the Name of Allah,

The Most Compassionate, The Most Merciful

DEDICATEDTO

MY DEAR PARENTS,

MY CARING SISTERS

AND

MY NAUGHTY BROTHER

Certificate of Originality

I hereby declare that the thesis report titled *"Design and Analytical Modeling of a Complete Transmit Receive Module (TRM) for Applications in Active Microwave Sensors"* is my own work and to the best of my knowledge it contains no materials previously published or written by another person, nor material which to a substantial extent has been accepted for the award of any degree or diploma at NUST or any other education institute, except where due acknowledgment, is made in the thesis. Any contribution made to the research by others, with whom I have worked at NUST or elsewhere, is explicitly acknowledged in the thesis.

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List of Acronyms

TR:	Transmit-Receive
TRM:	Transmit-Receive Module
PAR:	Phased Array Radar
AESA:	Active Electronically Scanned Array
TX / RX:	Transmit / Receive
PRI:	Pulse Repetition Interval
PRF:	Pulse Repetition Frequency
MMIC:	Monolithic Microwave Integrated Circuits
HEMT:	High Electron Mobility Transistor
PA:	Power Amplifier
HGA:	High Gain Amplifier
LNA:	Low Noise Amplifier
SPDT:	Single Pole Double Throw
PCB:	Printed Circuit Board
ADS:	Advanced Design Systems

Abstract

The most advanced microwave sensors "Phased Array Radars" have received considerable importance in commercial, medical and defense applications. Lot of research has been carried out regarding development of necessary constituents such as antenna array, transmit-receive module (TRM) and back-end processing units. However the cost reduction, efficiency improvement, wide bandwidth, and fabrication technology for the TRM have been pursued as key research areas. Cost reduction techniques till date have focused on the use of high tech MMIC fabrication techniques. Literature also lacks in guiding a novice design engineer working on TRM in a cost effective manner.

The work aims at software modeling of the TR Module constituents and also present a mathematical analysis of signals involved to enable a design engineer understand the constraints involved in designing such a system. Commercially available, low cost Laminate *FR-4* has been used for the microstrip based designing in Advanced Design Systems (ADS). Due to the low operational frequency of *Fr-4*and constraints on the availability of components availability, 2.0 GHz has been used as design frequency. Regarding the *FR-4* frequency response, a study has been conducted to study the deviation in simulation and measured results, which indeed confirmed the low frequency operation of the laminate. The modules designed include the high gain block (HGA), low noise amplifier (LNA), transmit/ receive switch and phase shifter. Designed for maximum achievable gain, the amplification blocks are based on Class-A topology with HGA of the cascade type and LNA being a single stage amplifier. The TR switch is based on series-shunt configuration of the single pole double

throw (SPDT) switch as this topology achieves best results both in terms of minimizing insertion loss and maximizing isolation. Varactor diode based analog phase shifter has been designed for the phase manipulation purposes. The device achieves phase variations of the order of 150 degrees. Due to control limitations of the varactor tuning, reflection type 5 bit digital phase shifter has also been designed and the simulation results fall in close agreement to some of the commercially available modules.

The scope of the thesis being limited only to the software modeling and simulations, the current write-up presents this aspect only. However due to ever increasing applications of this technology, the designed modules are being pursued to the implementation stage to realize a prototype level TR module.

Acknowledgements

Chapter 1: Introduction

1.1 Microwave Sensor – The RADAR

Ever since its evolution, the classical microwave sensor, "The RADAR" has gone through tremendous advancements and developments. From earliest designs comprising of huge structures to today's highly sophisticated systems, it has greatly benefitted from the advancements in semiconductor technology, antenna design, and signal processing capabilities etc. Classical Radar has limited functionalities of the target detection and the range determination. Modern radar, additionally, has the ability to classify the type of target, track the target movement and minimize the unwanted interference etc. These advancements have made Radar useful also for civilian use. For example, speed detectors have commonly been employed on highways, air traffic control, air navigation and space applications etc.

Radar an acronym for *Radio detection and ranging* is based on a simple principle of reflection of energy. It transmits an electromagnetic energy over a certain volume of space; objects (targets) within that volume reflect back "echoes" some of the incident signal towards the Radar. The principle of Radar operation [1] is shown in Figure 1.
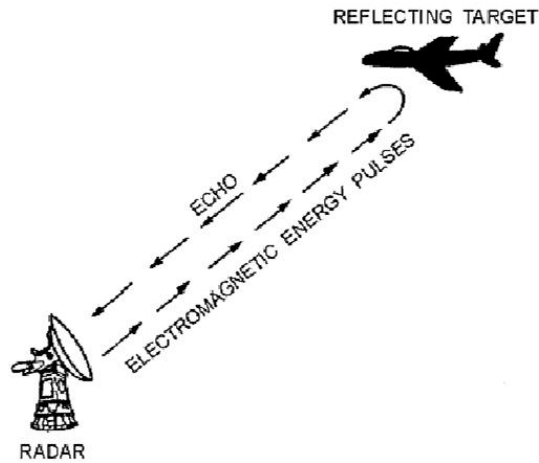
Figure 1: Principle of Radar operation[1]

The strength of the received signal and some other parameters (Doppler shift in frequency, time delay between the transmitted and received signal etc.) help determining the characteristics of objects (targets). The block diagram of the Radar system highlighting the key elements is shown in Figure 2.
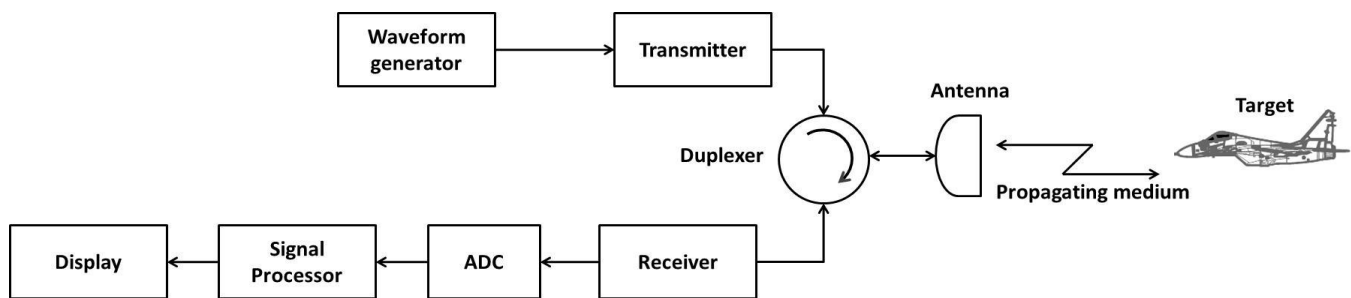
Figure 2: Functional block diagram of a generic Radar system

1.1.1 Waveform Generator

Waveform generator part of the Radar is broadly classified into two categories i.e. a) Continuous Waves (CW) and b) Pulsed Waves (PW).

a. **Continuous Waves** generators comprise of a pure or modulated sine wave being transmitted at all the times. These are mostly employed in *bistatic radar configuration,* shown in Figure 3, where separate

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antennas far apart from each other, are used for both transmission and reception.
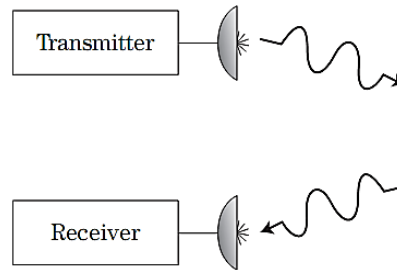
Figure 3: Bistatic radar configuration[1]

Such a configuration is employed to eliminate interference between the transmitted and received waves. Continuous wave radars are generally not preferred as the power is continuously transmitted into the medium. CW signal generation and handling is challenging.

b. **Pulsed Wave** transmission is generally employed in current radars. In such systems, a continuous wave is switched ON during the transmission interval. During the OFF interval, the radar enters into receive mode. Due to switching between the two modes, same antenna can be used for the Radar. This mechanism is also power efficient as transmitter is not active all the times. Radars employing such single antenna configuration are termed as monostatic radars. The monostatic radar configuration is shown in Figure 4.
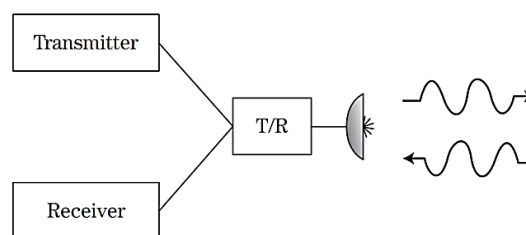
Figure 4: Monostatic radar configuration[1]

Figure 4is quite self-explanatory. For pulsed transmission bistatic radars with both antennas close to each other are also used.

The key parameters, such as the width of the pulse and pulse repetition interval (PRI), related to the Pulsed Wave transmission are highlighted in Figure 5.
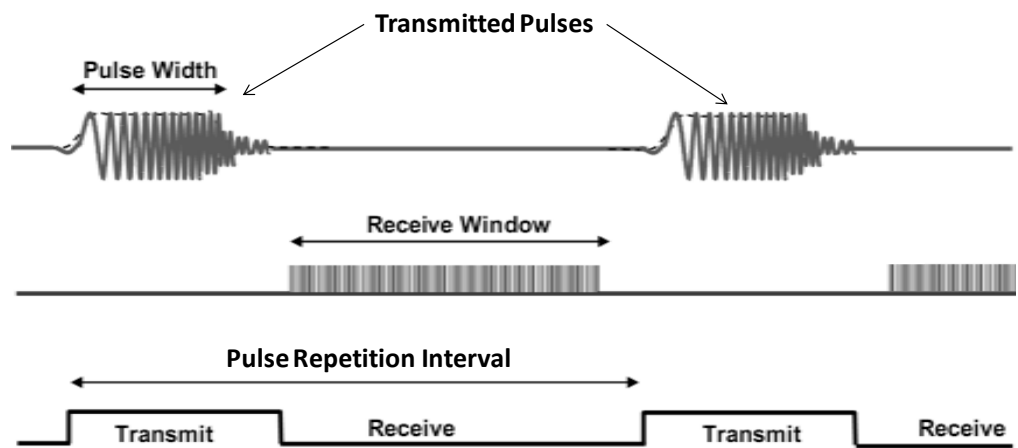
Figure 5: Pulsed wave transmission and reception

The pulse repetition frequency (PRF) in Hz is the inverse of the PRI in seconds.

1.1.2 Transmitter

Transmitter section of the radar system is where the weak signal of the generator is amplified to send it over long ranges. This amplification can be achieved over multiple stages. Second type of amplification known as Parallel amplification can be achieved by operating the amplifiers in parallel and then summing the output of each one before feeding it to the antenna. However the parallel amplification is complex and less efficient due to splitters and combiners losses. Conventional radars use vacuum tube amplifiers however in

newer systems e.g. the phased array systems, array gain can compensate for amplifier gain limitation; active electronically scanning radars employ solid state amplifiers. Multistage amplification mechanisms in a radar transmitter are shown in Figure 6.

In series configuration Figure 6(a), the number of amplifiers is limited by the dynamic range, as former module output must lie within the limits dynamic range of the later one. Also the configuration has more noise contribution as the individual module's noise also gets enhanced when applied at the input of next module. The dynamic range dependence and noise related issues are not faced in parallel configuration Figure 6(b) as all the modules are exposed to the same level of input and the combiner performs linear summation of each amplifier's output. The configuration however suffers from splitter and combiner losses.

Multi stage amplification　　　Antenna

Waveform generator
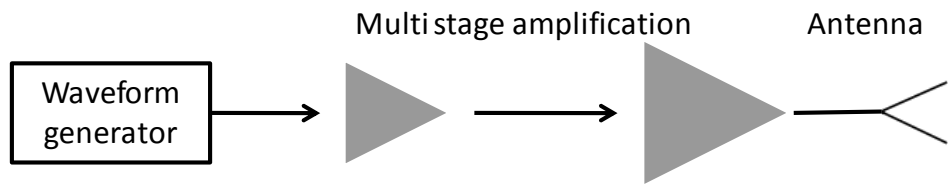
(a) Multistage series amplification

Splitter　　　　　　　　　　　Combiner

Waveform generator

Antenna

Σ
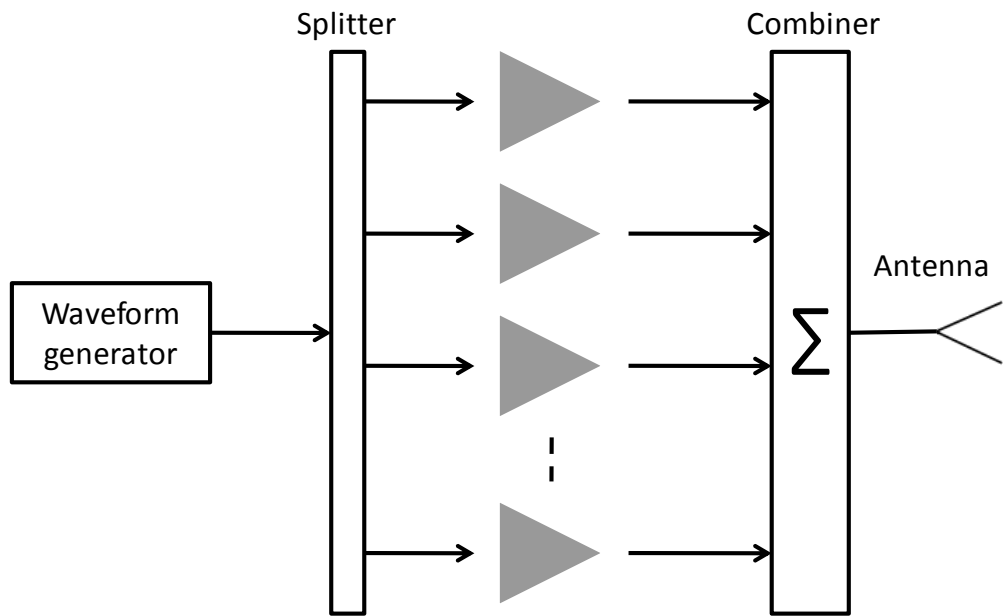
(b) Parallel amplification

Figure 6:Multistage amplification mechanisms in a radar transmitter

1.1.3 Duplexer

Duplexer is device that alternates the antenna between transmission and reception modes. During the transmission mode, it protects the receiver circuitry from being damaged by high power transmitted signal. During the receive mode, it connects the antenna to the receive section. Figure 7highlights the duplexer functionality.
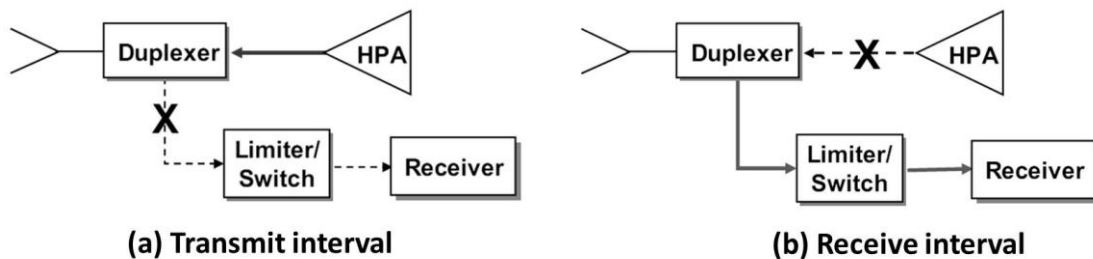
Figure 7: Duplexer operation in transmit (a) and receive (b) intervals

1.1.4 Receiver

In the receiver section of the radar, the incoming echo signal form the antenna is first filtered to minimize the unwanted noise. The filtered signal is then amplified by low noise amplifier and down converted to the baseband level. Once the signal is converted into baseband, it can be further processed by converting it into the digital format. Another important feature of the receiver section is the protection circuitry known as the limiter circuit. The limiter circuit protects the sensitive receiver circuits from being damaged by high power received signals and unintentional interfering signals. Receiver section can also employ multi stage amplification and filtering. Receive section of the radar is shown in Figure 8.
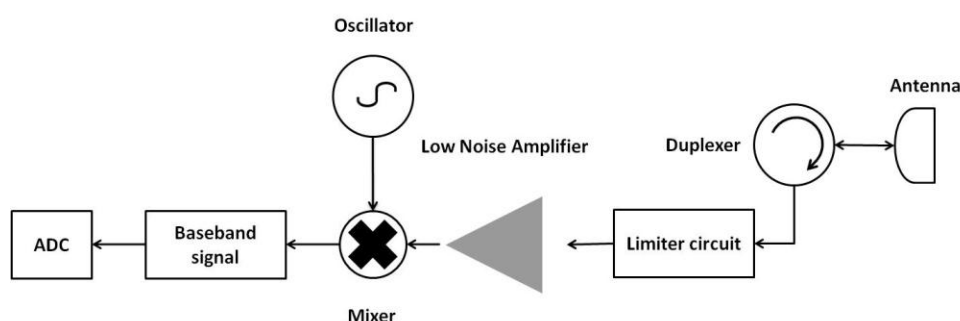
Figure 8: Receive section of the radar

1.2 Fundamentals of a Phased Array Radar

In phased array radars, the steering of radiation beams in a particular direction takes place by controlling the relative phase of the signal fed to each of the antenna element.

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If the antennas are separated by a fixed distance d, the operating wavelength is λ and the desired angle to steer the beam is $\emptyset$, then the relative phase shift that needs to be included between successive elements, Δ can be calculated by simple trigonometric relation given below:

$$\Delta = \frac{2\pi}{\lambda} d \sin \emptyset \qquad\qquad 1$$

If the first element is taken to be at reference phase, then the second element needs to have a relative phase shift of Δ, the third element 2Δ and so on. The pictorial display of such a concept is presented below in Figure 9.
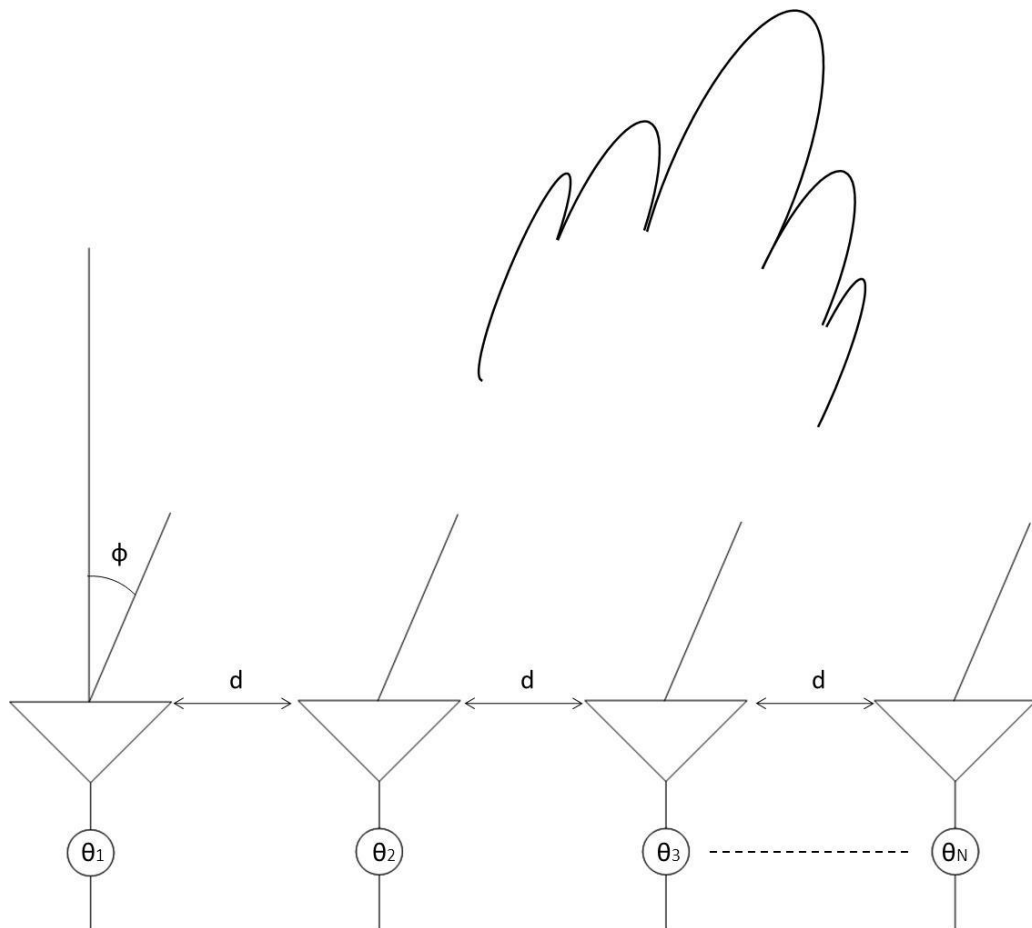
Figure 9: Beam steering in phased array antenna systems

It is not only this phase shift that makes the phased array radars so special, but the amplitude variations to each element also adds additional features to its functionality.

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The amplitude variations enable these radars to steer their nulls (minima in the radiation pattern) in the direction of interfering sources and jammers hence suppressing their impact and improving performance to a considerable level. Figure 10 shows the two dimensional plot of radiated power vs. normalized phase. It is observed that steering the radiation pattern also enables creation of nulls which directed in a particular direction can suppress the impact of jamming sources.
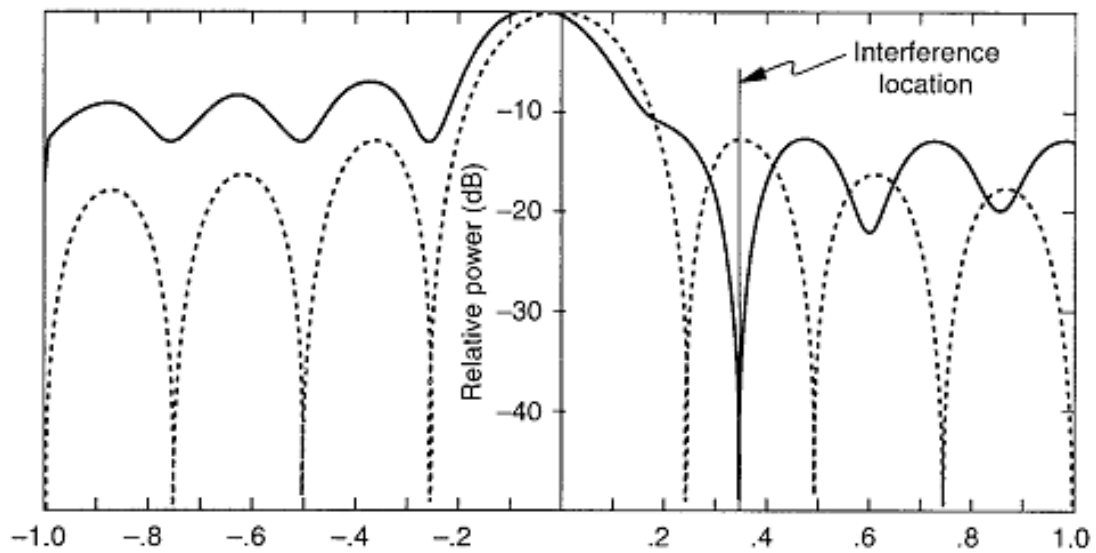
Figure 10: Interference suppression in phased array radars [2]

Based upon the signal feed type, its amplification and phase shifting mechanism etc., the phased array radars are broadly classified into two main categories i.e. the passive and active phased array radars.
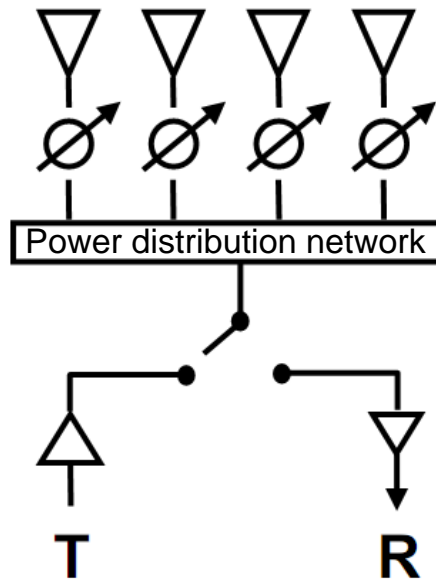
Figure 11: Passive phased array radar [3]

In passive phased array radars, model shown in Figure 11, a single transmit and receive element is shared by all the antennas. The input signal, amplified by power amplifier is fed to the distribution network. The output signal of the distribution network is phase manipulated and fed to each of the antenna element. On the receive side, a single Low Noise Amplifier (LNA) receives the beam synthesized by the network. Apart from performing fast beam steering the passive phased array radars have an advantage that they utilize single transmit and receive gain blocks same as used by the conventional radars. Hence by designing a feed network and phase shifters, conventional radars can be upgraded to have beam steering capability which would minimize the mechanical losses and power consumption required for antenna rotation. On the other hand, the main drawback with such passive radar is the use of power distribution network. The distribution network introduces significant loss in the amplified signal from the transmitter. To generate enough power, the amplifier needs to be operated at or near saturation thus reducing its dynamic range or operating margin. Also the phase shifters encounter a signal much higher in power level which

puts tight design criterion for them [3]. However despite all these pros and cons, passive phased array radars does have an edge over the conventional radars.

The active phased array radar, shown in Figure 12address all the shortcomings found in the passive one. The basic functionality is as follows. The feed signal from the exciter is supplied to each of the "*TR Module*" in which each antenna has an associated power amplifier, low noise amplifier and phase shifter thus mimicking the radar functionality at each of the antenna level. The radar is called *Active* for the same reason that amplification blocks are associated with each antenna element. Since the system has distributed characteristics, the design requirements for each element are also relaxed. The phase shifters are exposed to low power levels hence increasing their operational life. In fact this architecture of active phased array radar enabled the proliferation of solid state technology in the field of radars. The features of solid state devices mentioned in the preamble become more important when they are applied for active phased array radar's TR module.
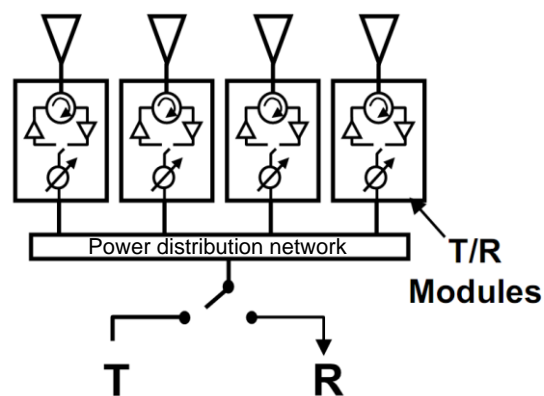
Figure 12: Active phased array radar [3]

The other important features associated with active phased array radars are [4]:

- The resiliency of solid state devices is more hence active phased array radars have lower rate of failure

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- The system undergoes *"Graceful degradation"* i.e. the failure of one component does not greatly influence the overall performance

- The system has improved sensitivity

- Digital control can be incorporated in several components

- System up-gradation become more easy due to its modular design

Apart from the flexibility, robustness and improved performance, the limitation in implementation of these active radars lies in their cost as 60%-80% of the total cost is incurred only in TR module solid state components [5] and this factor becomes significant with systems having thousands of TR modules.

1.3   TR Module and its Types

As presented in the previous section, TR Module constitutes the fundamental component of active phased array radars. Several different configurations of TR module exists, the simplified block diagram of the module is shown in Figure 13.
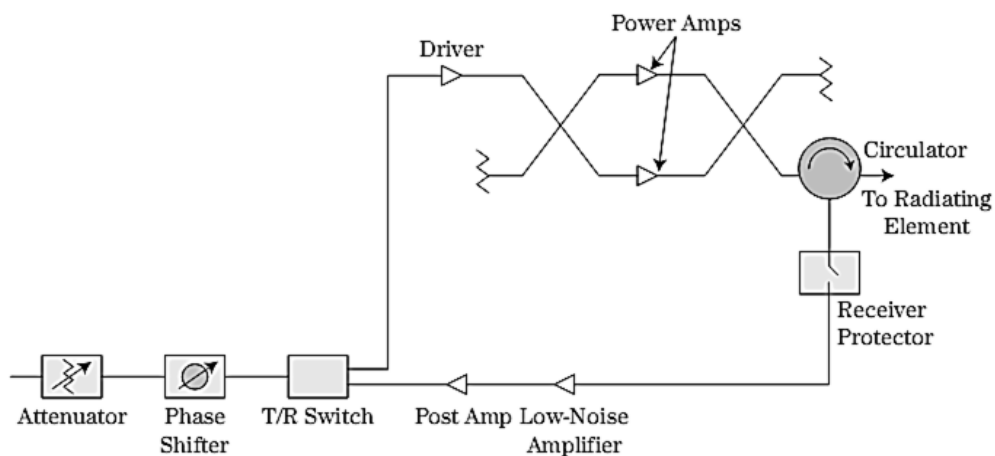
Figure 13: TR module block diagram [6]

The major constituents of TR modules and their brief description are as under:

a. *Attenuator:* The attenuator in a TR module adjusts the gain of the system to minimize the side lobes as well as to steer the nulls in the direction of interfering sources. In most of the cases the attenuator has digital inputs to control its operation.

b. *Phase Shifter:* An integral part in TR module, the phase shifter provides required phase shift to steer the antenna beam. The steering capability is greatly dependent upon the resolution of the phase shifter. Analog devices can provide continuous $0\text{-}360^0$ phase shift whereas the digital phase shifters are limited by the number of control bits.

c. *TR Switch:* Transmit-receive or TR switch controls the operation of the module. In most of the cases it is a single pole double throw (SPDT) switch, and alternately switches the system in the transmit and receive modes.

d. *Power and Driver Amplifier:* These gain blocks amplify the transmitted signal. The amplification depends upon the type of function and the range which the radar is going to cover. These amplifiers can comprise of several of the stages and are the main exploits of solid state technology.

e. *Circulator:* It is a passive device that connects the antenna to the transmit section and isolates the sensitive receive circuitry from the high transmit power.

f. *Limiter Circuitry:* This protection circuit is incorporated mainly to protect the low noise amplifier from being saturated by high transmit power reflected backward due to the antenna mismatch. Also the high power jamming signals can be isolated from damaging the system.

g. Low Noise and Post Amplifier: The radar received signals are often very weak in strength and rich in noise levels. To extract meaningful information, the signal is amplified by low noise amplifier (LNA) so as to minimize the noise injected by the system. The LNA amplified signal is then further amplified to levels enough to extract the target information.

The TR module is also accompanied by cooling circuitry to dissipate the heat generated by the amplification blocks. Different types of TR modules reported in literature comprise of the same generic blocks highlighted in TR module block diagram in Figure 13. However, the electrical architecture of the module has two configurations i.e. the common architecture and the separated architecture [7].
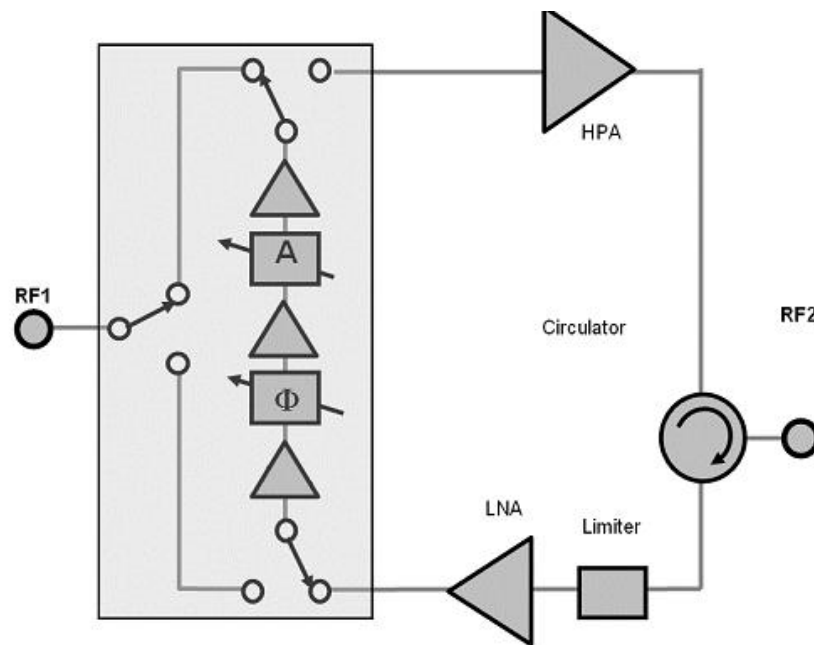
Figure 14: Common Architecture TR module [8]

The TR module architecture shown in Figure 13is also known to have a separated architecture. The selection of particular configuration depends upon the application. However the main factors that determine the selection of a particular configuration

depend upon the noise figure of the module, the power consumption, the switching times etc.

1.4   Literature Review

This section describes the TR module and its technological trends presented in literature. Two different aspects are found i.e. the development efforts and future directions based upon the constantly evolving requirements. The literature focusing on the developmental progress often concludes the research and development work on a particular type of TR module or its configuration. The main features of the system designed are highlighted and measured results compared against the benchmarks defined in the requirements gathering phase.

Cost has always been a major factor in the widespread use of any technology. Same is the case with TR modules and commercial device manufacturing has been utilized in [5]. 0.5 μm GaAs based pHEMT process is used to fabricate the MMIC. Another emphasis in this work has been on functional integration of the module components. The fabricated two channel TR module is shown below (image taken from [5]);
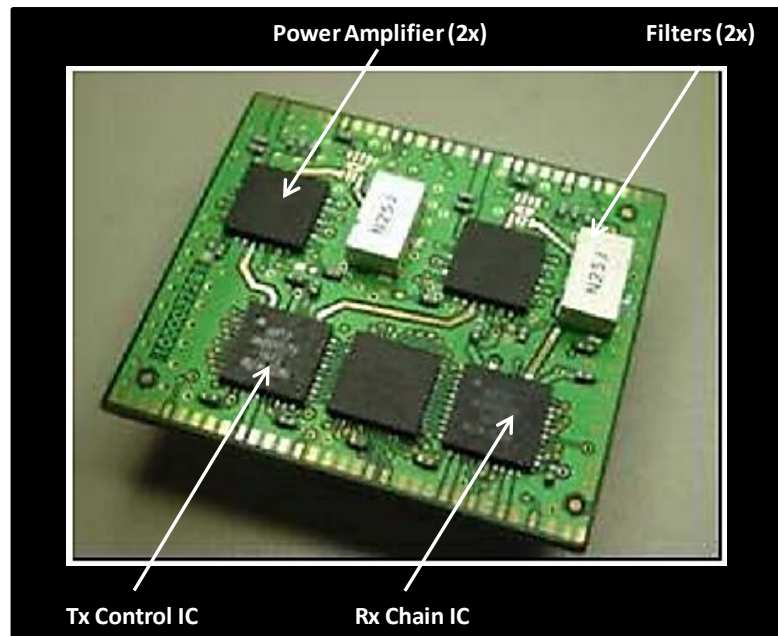
Figure 15: Low cost S-Band T/R Module [5]

Wideband system design is another key design requirement in RF system design. In [9], a wideband TR module development work has been presented. The operating frequency covers C, X and Ku bands and the key design requirements included uniform gain over the required spectrum, maximum power amplifier design, thermal management and module package design etc. The final product is that four TR modules have been integrated on the same MMIC chip. The Figure 9shows the module layout (image taken from [9]). Another work [10] also designs MMIC based wideband 2 channel TR module for multi-function AESA radar.

Power consumption has also been a critical design parameter, so is addressed in [11]. InP based HEMT technology has been used for power efficient and integrated TR module design. Separate architecture TR module with 50% efficiency per module is designed. High efficiency (more than 70%) TR module is also designed in [12]. In this work class EF amplifier based module has been designed for synthetic aperture radar (SAR). The work conducted by NASA lasted for three years to realize the final module.
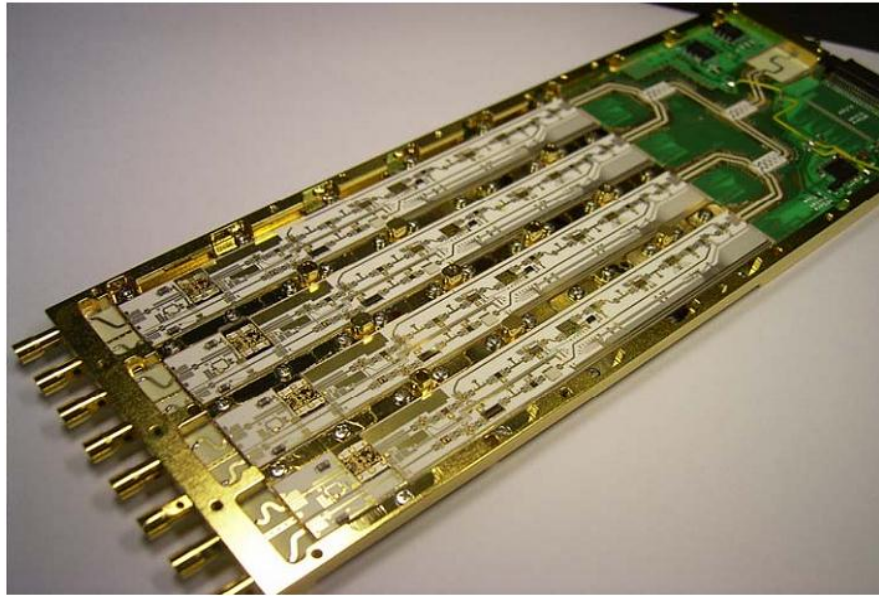
Figure 16: Four channel integrated TR module layout [9]

Solid state fabrication technology and substrate material has also been taken into account in [13]. Instead of GaAs monolithically integrated circuit (MMIC), AlGaN/GaN HEMT MMIC technology is used for the TR component fabrication. High power and better performance has been achieved by the use of GaN based technology. Below is shown the designed product image taken from [13]
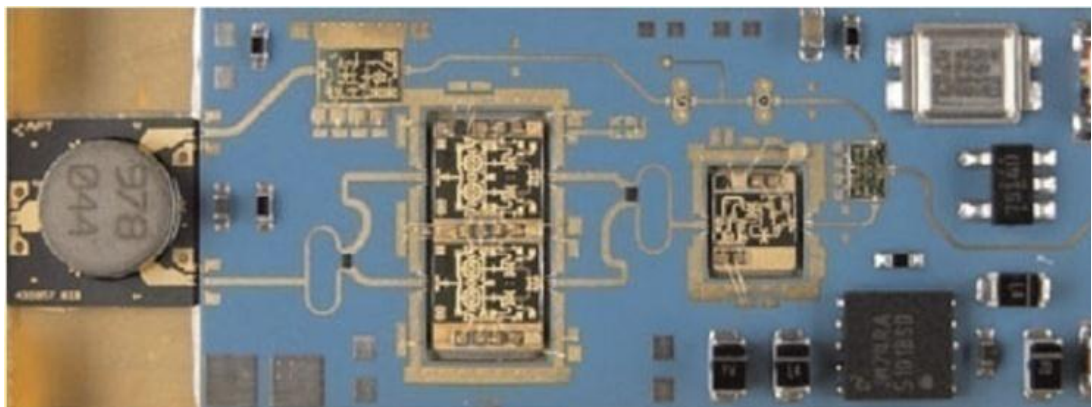
Figure 17: T/R-module front-end with GaN MMIC chips [13]

Apart from the above mentioned developmental work, there have been many other articles providing details of the designed systems. The second type of articles giving an insight about the future design and performance are mostly survey works,

summarizing the findings of work already done and giving future guidelines for performance enhancements.

In this regard, [14] is an excellent article as it covers a broad range of future demands upon TR modules e.g. light weight, low cost, mass production, efficient and wide bandwidth etc. The work suggests the use of SiGe technology for the functional integration of TR module components. Also AlGaN/ GaN based amplifiers are forecasted to be of high efficiency and increase the system robustness. Another hot area for phased array radars is the use of digital beam forming techniques to enhance their performance. For this to achieve, SiGe BiCMOS technology is proposed to have good RF performance. Another work [15] highlights the same trends in future AESA radars. Wideband and multiband systems design is emphasized to be the main developmental focus for times to come. GaN based technological has also been expected to boost performance by efficiency increase.

MEMS have also been proposed to be significant in components design of TR modules e.g. the phase shifters and switches etc.[16]

1.5 Motivation for Current Work

Chapter 1 presented a detailed overview of the phased array radars from different perspectives. Collecting information from different sources and presenting radar functionality and its components, a system level overview of the phased array radars, the development of active phased array radar, the motivation behind their usage and the technological pros that enabled them to surpass them over the conventional radar architectures was presented. The chapter also presented a detailed treatment of the *heart* of this development i.e. the TR module and highlighted some of the main features. This technology being proliferating in defense, medical and civilian

applications; current work investigated the signal analysis and system level simulation of the TR module. As this aspect of TR modules has never been addressed before, the mathematical treatment of signals involved is performed to make the reader understand the constraints involved in system design and development. The main constituent apparatus of TR modules are designed and simulated in ADS and later on integrated into a single module. The dissertation layout is as under;

Chapter 2 presents the analytical model and behavioral simulation of the TR module.

Chapter 3 highlights the design principal of the amplification modules, the transmit/receive switch and the analog phase shifter. The integrated module simulations are presented at different nodes of the module and results compared to that of behavioral simulation using ideal software blocks.

Chapter 4 summarize the design principal and simulations of the 5 bit digital reflection type phase shifter

Chapter 5 concludes the dissertation with few words on the future course of action.

Chapter 2: Behavioral Modeling of a TR Module

Phased array radars have been the key exploits of electronic beam steering offered by phased array antenna systems. Apart from the military applications, commercial applications like satellite communications [17], weather monitoring, air traffic control and security applications also utilize antenna arrays.The evolution of passive to active antenna arrays has also been instrumental in expanding the list of these applications.

This chapter presents a top down view of phased array radar system in particular active phased array radar. Starting from the concept of beam steering and antenna arrays, the focus will then be shifted to the behavioral analysis and simulation of Transmit/ Receive Module (TRM).

2.1 Phase Contribution

The electronic steering of the antenna array beam is based upon the phenomenon of constructive and destructive interference of waves. Based upon the respective phases of the signal fed to each of the antenna element, the radiation pattern adds constructively in some directions and destructively in other directions resulting in an overall steering of the beam.

Generally, N number of TR modules is required in N-element phased-array antennas system. Figure 9shows an antenna array where each antenna is fed by a signal from a TR module and the two consecutive antenna elements are separated by a fixed distance*d*. For simplicity the TR module is represented only by a phase shift block.

In order to steer the beam by an angle ϕ, the amount of relative phase shift Δ that needs to be inserted between two successive antennas is given by given byEquation **1**.

Referring to Figure 9, taking first antenna (phase contributionθ_1) as the reference, the second element must have a phase shift ofΔ, the third element 2Δ and so on. Generalizing for any antenna array, the phase shift inserted by a phase shifter in N^{th} TRM is given by:

$$\theta_N = (N - 1)\Delta \qquad\qquad\qquad \textbf{2}$$

The gain of the system directly depends upon the number of antenna elements i.e. the more the number of antennas the greater will the overall system gain [18]. The separation between the consecutive antennas is important regarding the overall radiation pattern and the directivity and side lobes level of the array is optimum at an inter-element separation of $\lambda/2$ [19].

The speed of electronic steering depends upon the speed with which the phase values are computed. Often the number of antenna elements exceeds 10,000 [20]and a processor is dedicated to perform these phase computation quickly. Such fast beam steering enables the phased array radars exceed the mechanically rotated systems whose speeds are 4-6 rpm for ground or ship based systems and 30 rpm for Air-borne applications[21].

In this regard, [22] presents the simulations of antenna array and beam steering concept for 4-element planar antenna array.

2.2 Mathematical Analysis of Signals

As described in chapter 1, most of the current radars have pulsed operation, the RF oscillator signal needs to be modulated with a clock signal with ON time equivalent to the transmit duration of the radar. The period of the clock signal is equal to the pulse repetition frequency (PRF) of the radar.

An oscillator generates a sinusoidal signal of the form:

$$x(t) = a_0 \sin(w_o t) \qquad\qquad \textbf{3}$$

Where w_o is the carrier frequency i.e. 2 GHz at which the simulations are performed. Mathematically, the pulsed/ clock signal, has a description as under:

$$c(t) = \begin{cases} 1 & 0 < t < \tau \\ 0 & \tau < t < T \end{cases} \qquad\qquad \textbf{4}$$

Where the period $T = \frac{1}{PRF}$. The multiplication of $x(t)$ and $c(t)$ generate a pulsed RF signal which is fed to the input of power distribution network. The pulsed RF will have the following mathematical notation:

$$s(t) = c(t) \times x(t) \qquad\qquad \textbf{5}$$

In order to better understand the signals involved at different positions of TR module, a detailed block diagram of the module is presented with different nodes marked.
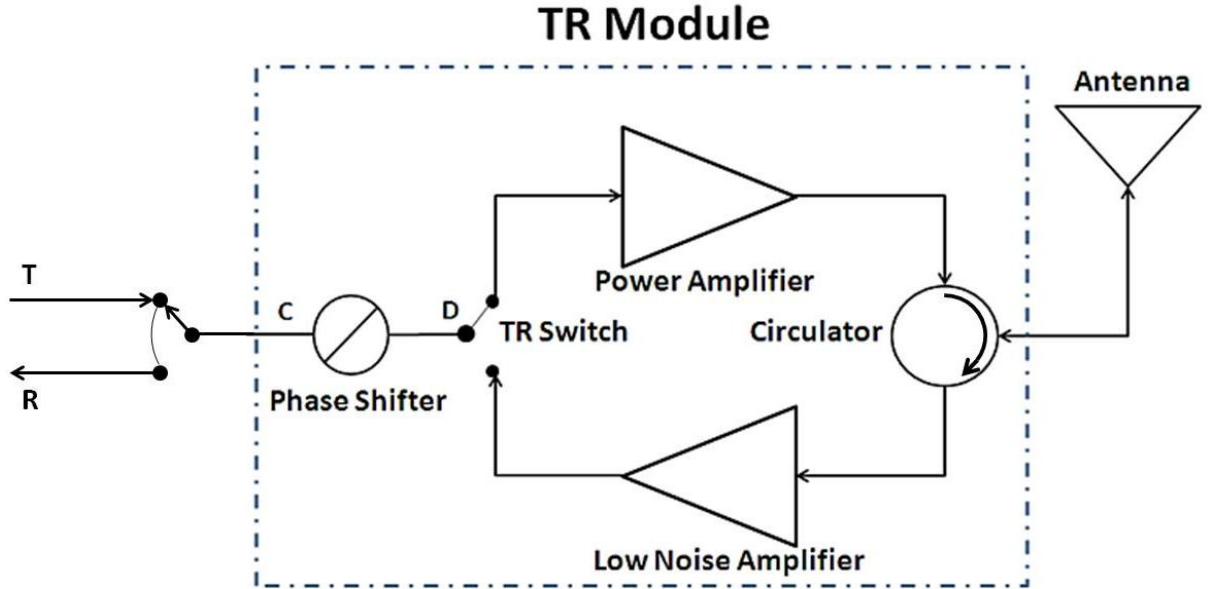
TR Module

Figure 18: TR Module functional block diagram

The modulated signal applied at the input of the TR module at position "C" has the mathematical notation as under:

$$s(t) = \begin{cases} a_0 \sin w_0 t & 0 < t < \tau \\ 0 & \tau < t < T \end{cases}$$

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The pulsed RF signal $s(t)$ at node "C", is then applied at the input of TR module where it first encounters the phase shifter. The phase shifter, depending on its respective antenna position, introduces a phase shift given by equation2. Assuming the phase shifter to be an ideal device with no insertion loss, the signal that is fed at the input, node "D", of Nth TR switch is represented as:

$$s(t)_N = \begin{cases} a_0 \sin(w_0 t + \theta_N) & 0 < t < \tau \\ 0 & \tau < t < T \end{cases}$$

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Through the TR switch, the phase shifted signal is passed to the transmit arm of the module where it is amplified by the power amplifier (PA) by a factor of G_p and sent to the antenna which further adds its gain G_A to the signal. The Nth module signal that escapes into the air can be represented as:

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$$a(t)_N = G_p G_A a_o \left(\sin w_o t + \theta_N \right) \qquad \qquad \textbf{8}$$

As the beam steering phenomenon is governed by constructive and destructive interference of waves, the total radiation pattern of the system is the linear summation of the radiated signals from the antenna elements i.e.

$$
\begin{aligned}
R(t) \quad &= \sum_{i=0}^{N-1} a(t)_i \\
&= \sum_{i=0}^{N-1} G_p G_A a_o \left(\sin w_o t + \theta_i \right)
\end{aligned}
\qquad \qquad \textbf{9}
$$

The preceding equations **3** to **9** presented a time domain view of the signal at different points of the TR Module. It is equally important to have a view of the signal frequency spectra as it provides the design engineer an understanding of the bandwidth considerations involved in system design.

Mathematically equation **3** in spectral domain comprise of two impulses located at $|w_0|$

$$|X(w)| = \frac{a_o}{2} \; at \; |w| = w_0 \qquad \qquad \textbf{10}$$

The $|n|$ indicates the absolute value of the of n.

The spectral representation of equation **4** is a ***sinc*** function. In fact the bandwidth of transmitted signal is directly related to the width of the ***sinc***, which depends on the ON time and PRF of the pulsed signal. Thus system is not only dependent on the range or external parameters but also on the internal control circuitry. The pulse train being a periodic signal, its spectral content comprise of the Fourier series coefficients of the of signal i.e.

$$|C_n(w)| = \frac{\tau \ \sin\left(\frac{nw\tau}{2}\right)}{T(nw\ \tau/2)} \ , |C_0(w)| = \tau/T$$

11

$$= \frac{\tau}{T} \ sinc\left(\frac{nw\tau}{2}\right)$$

For example, if T=1ms and τ=0.1ms, the first null bandwidth from the center depends upon the width of the pulse ($1/\tau = 10 \ KHz$) and separation between spectral components depends upon the period ($1/T = 1 \ KHz$) of the pulse train.

This is illustrated in Figure 19.
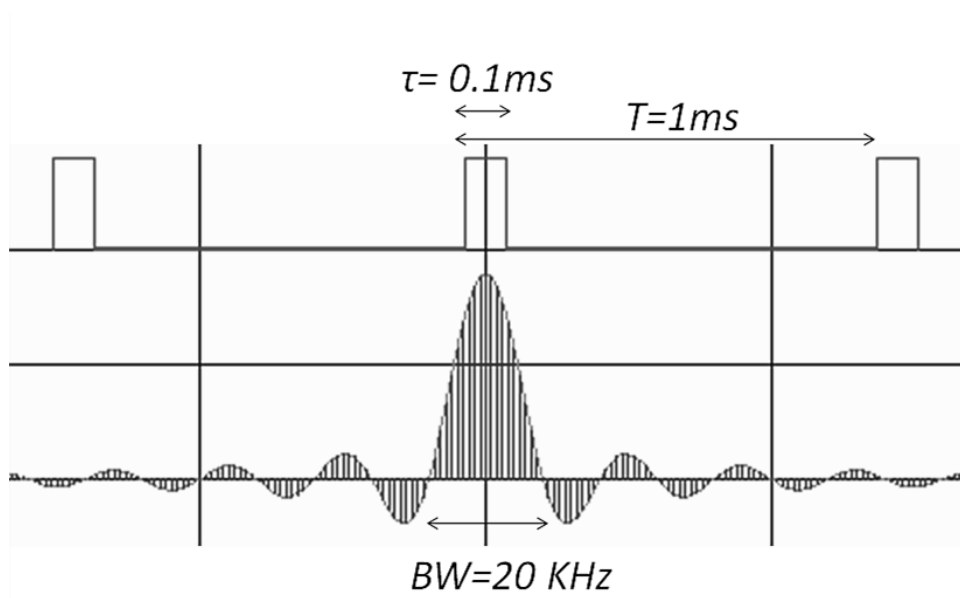
Figure 19: Time and Frequency representation of pulse train

Since in mathematical notation, multiplication in time domain is equivalent to convolution in frequency domain the pulsed RF signal in spectrum will be equivalent to shifting of the *sinc* shaped spectrum at w_0.

$$|S(w)| = C_n(w) * X(w)$$
$$= \frac{\tau}{T} \ sinc\left(\frac{n(w - w_0)\tau}{2}\right)$$

12

|S (w)|illustrates the spectrum actually occupied by the pulsed RF signal at a given PRF and carrier frequency.

The summed signal shown in equation 9when propagates through the air, in addition to other environmental degradations, undergoes from free space loss (FSL). The FSL is main degradation as it decays the signal strength as a square of distance i.e.

$$FSL = \left(\frac{4\,\Pi\,d}{\lambda}\right)^2 \qquad\qquad \textbf{13}$$

In equation**12**, d is the distance the radar pulse has propagated from the antenna and λ is wavelength of the carrier frequency.

Radar target is any object being tracked or searched and scatters some of the energy back to the direction of arrival. Apart from the desired one, the unwanted scattering bodies are termed as clutter. The most important characteristic of any radar target is its *"radar cross section (RCS)"*which is a measure of reflective strength of the radar. It is defined as:

$$RCS = 4\Pi\,\frac{P_s}{P_i} \qquad\qquad \textbf{14}$$

P_s is the power per unit solid angle scattered in a particular direction and P_i is the incident plane wave power per unit area. Typical values of RCS are $10^{-5}m^2$ for insects to $10^{+6}m^2$ for large ships [23].

The scattered signal becomes very weak in strength and also contains a lot of environmental noise. This signal falls on the radar antenna, gets multiplied by the antenna gain and is fed into the input of the LNA. Mathematically the signal input to LNA can be of the type shown below:

$$r(t) = R'(t) + n(t) \qquad\qquad \textbf{15}$$

$R'(t)$ is the Signal content at the LNA input of Nth T/R module and $n(t)$is the noise contribution from the wireless path.

Since the LNA is designed to have low noise contribution, the signal at the input is amplified with minimum noise contribution. The amplified signal available at its output is adjusted for its phase to minimize the directional impact of the plane wave that falls upon the antenna array. The adjustment of the phase of all the modules requires the reverse process of that involved in beam steering and hence enables the system to determine the directional aspects of the target.

2.3　The Behavioral Model

Agilent Advanced Design Systems (ADS) a versatile RF & Microwave designing tool is used to model the functional behavior of TR module as shown in Figure 18.

The simulation model comprises of the predefined software blocks e.g. the phase shifter, switch, amplifiers and circulator etc.

Since the objective of this behavioral simulation is to validate the functional aspects of TR module's blocks in light of the proceeding mathematical representation, the simulation parameters are selected keeping in view the validation of functionality and are not as based on any real system or model. However these parameters are based on the design constraints of the constituent elements of TR module i.e. the availability of PCB laminate for microstrip based designing, the frequency ranges of the PIN diodes for designing the phase shifter and TR switch and Transistor specifications for designing gain block and low noise amplifier etc.

These aspects are however discussed in detail in following chapters.

The simulation parameters for the behavioral model are given in Table 1

RF carrier frequency	2 GHz
Pulse period	25 nsec
Pulse Repetition Frequency (PRF)	40 MHz
High time/ ON time	5 nsec

Table 1: Parameters for TR module behavioral simulation

2.3.1 Pulsed Waveform Generator and its Simulation Results

The pulsed waveform generator is modeled by using the following software blocks;

a. **P_1 Tone:** P_1 Tone generates single frequency sinusoidal waveform.

b. **VtPulseDT:** The time domain pulsed source generates a clocked/ pulsed signal with a desired duty cycle and pulse repetition frequency

c. **Mixer:** The mixer block computes the product of the two input time domain signals

The simulation parameters and the respective blocks are displayed in the waveform generator below;
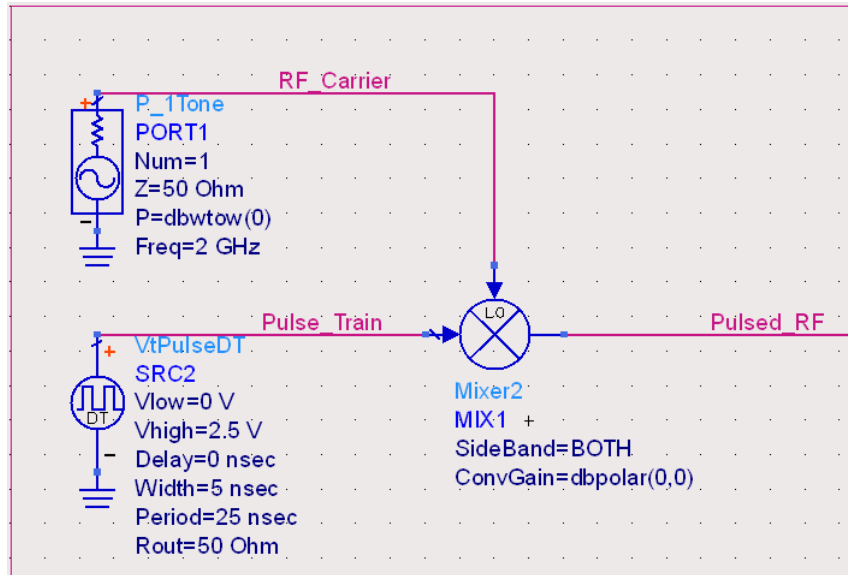
Figure 20: Modulation of RF carrier and Pulse train

The simulated signals in time domain are shown in Figure 21;

(a)   (b)
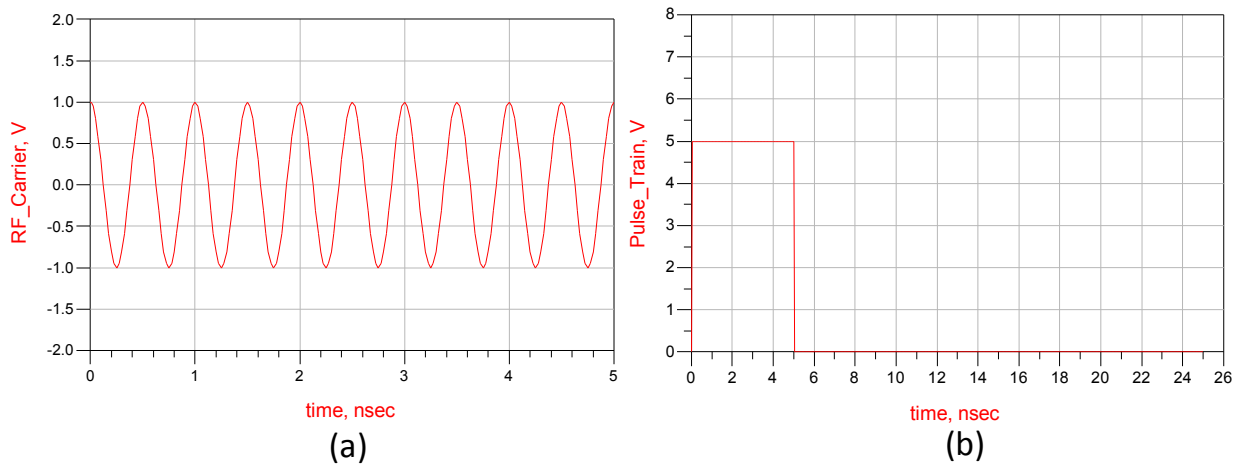
Figure 21: Time domain representation of signals

RF carrier, (b) Pulsed signal

The pulsed RF signal i.e. the product of two signals is shown below in Figure 22:
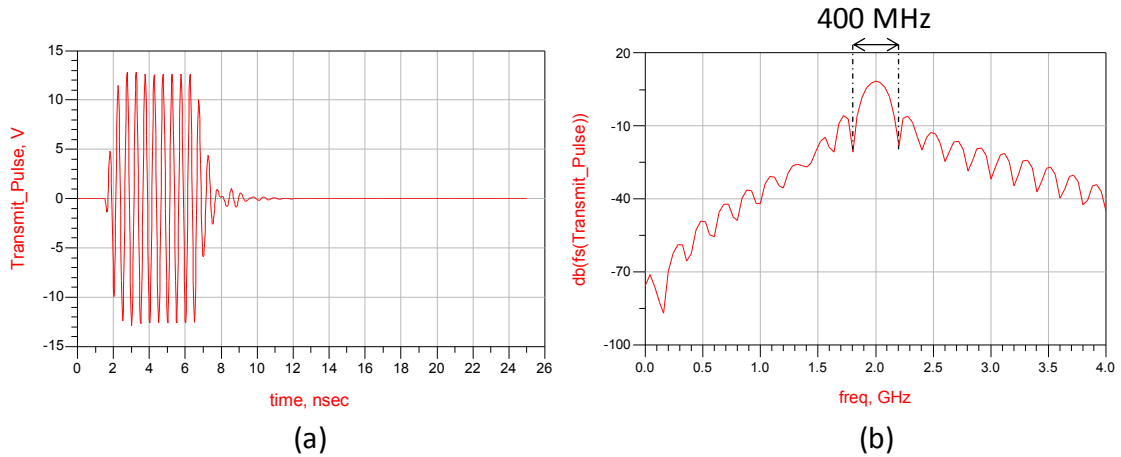
Figure 22: Pulsed RF signal (a) Time domain, (b) Frequency domain

The frequency domain representation is important to be discussed here. Referring to Figure 19, at the simulation parameters of T=25 ns and τ=5 ns, the first null bandwidth from the center comes out to be $1/\tau = 200\ MHz$ and separation between spectral components $1/T = 40\ MHz$.

In Figure 22 (b), the first null bandwidth comes 400 MHz which validates the respective mathematical expression.

2.3.2 TR Module Behavioral Model and Results

The software blocks used to model the TR module are;

a. **PhaseShiftSML:** Evident from its name, this block perform the phase shifting function

b. **SPDT_Dynamic:** Single pole double throw (SPDT) is used as a TR switch as well as in LNA input protection section. The receiver protection switch connects the receive terminal to a matched load of 50 ohms during the transmit interval. In this way, the leakage due to finite isolation of duplexer is not transferred to the LNA input.

c. **Amplifier:** Models high gain and low noise amplification section

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d. Circulator: A passive device to model duplexer.

The simulation model is as under, with antenna modeled as a 50 ohm termination;
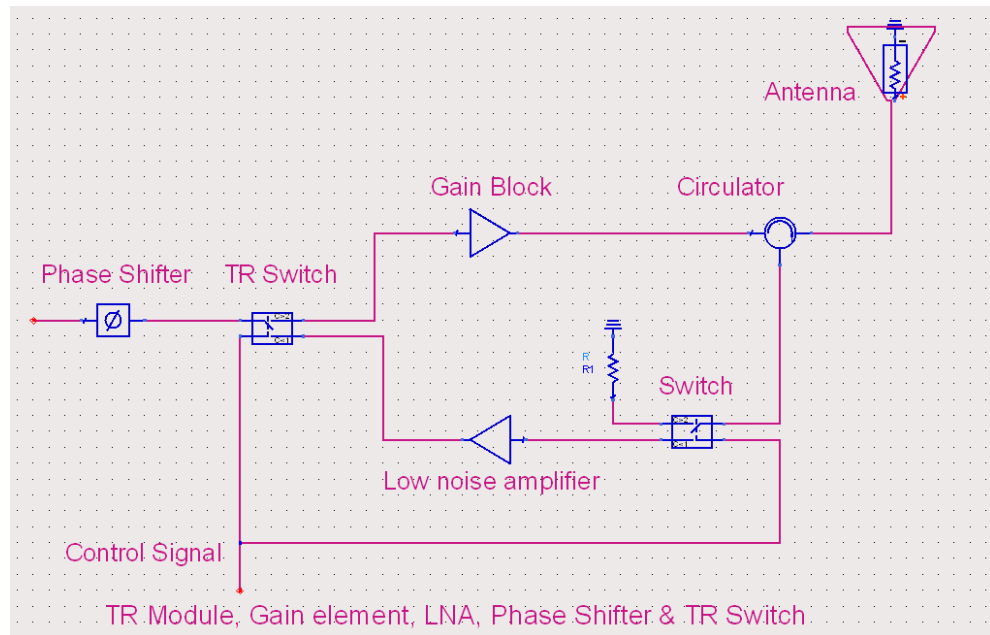
Figure 23: Toplevel model of TR module for behavioral simulation

The control signal of the switches is synchronized with that of the

pulsed source.

The Pulsed RF signal is applied at the transmit chain of the module.

Gets amplified by the amplifiers gain and is transmitted into the air.

The simulated output plots during the transmit stage are shown in

Figure 24
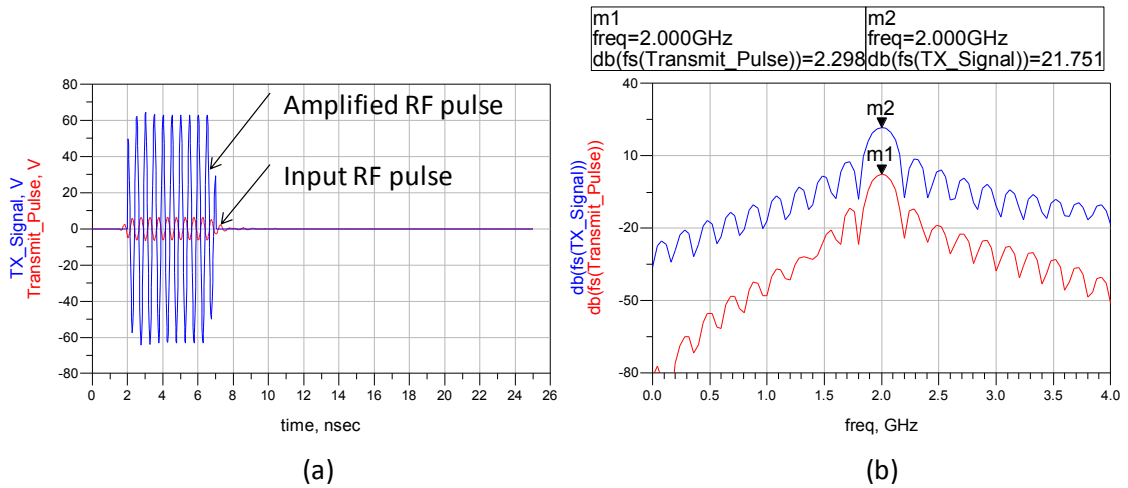
Figure 24: Pulsed RF signal at input and output of amplifier (a) Time domain, (b) Frequency domain

The amplifier gain is adjusted as per the specifications of the designed high gain amplifier which provides a gain of approx. 18 dB. On the receive side of the module, the receiver protection switch connects the circulator terminal to the input of the low noise amplifier (LNA). The 50 ohm termination is bypassed in the receive mode. The signal at the output of LNA is amplified by a designed amplifier gain of approx. 17 dB.
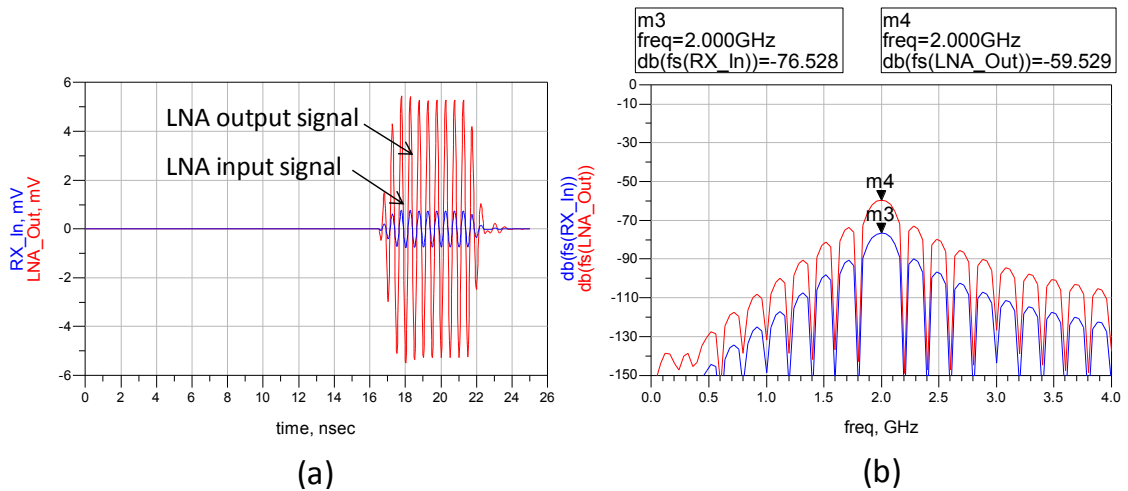
Figure 25: LNA input and output (a) Time domain, (b) Frequency domain

The loss between the transmitted signal and received signal is included in terms of free space loss as given by equation **13**. Two ways free space loss is

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included in simulations for both transmit and receive sides. Also the transmitted signal is delayed by 12-14 ns so that transmit and receive pulses do not overlap in the time domain representation.

The complete simulation model of the TR module using ideal software components is shown in Figure 26.
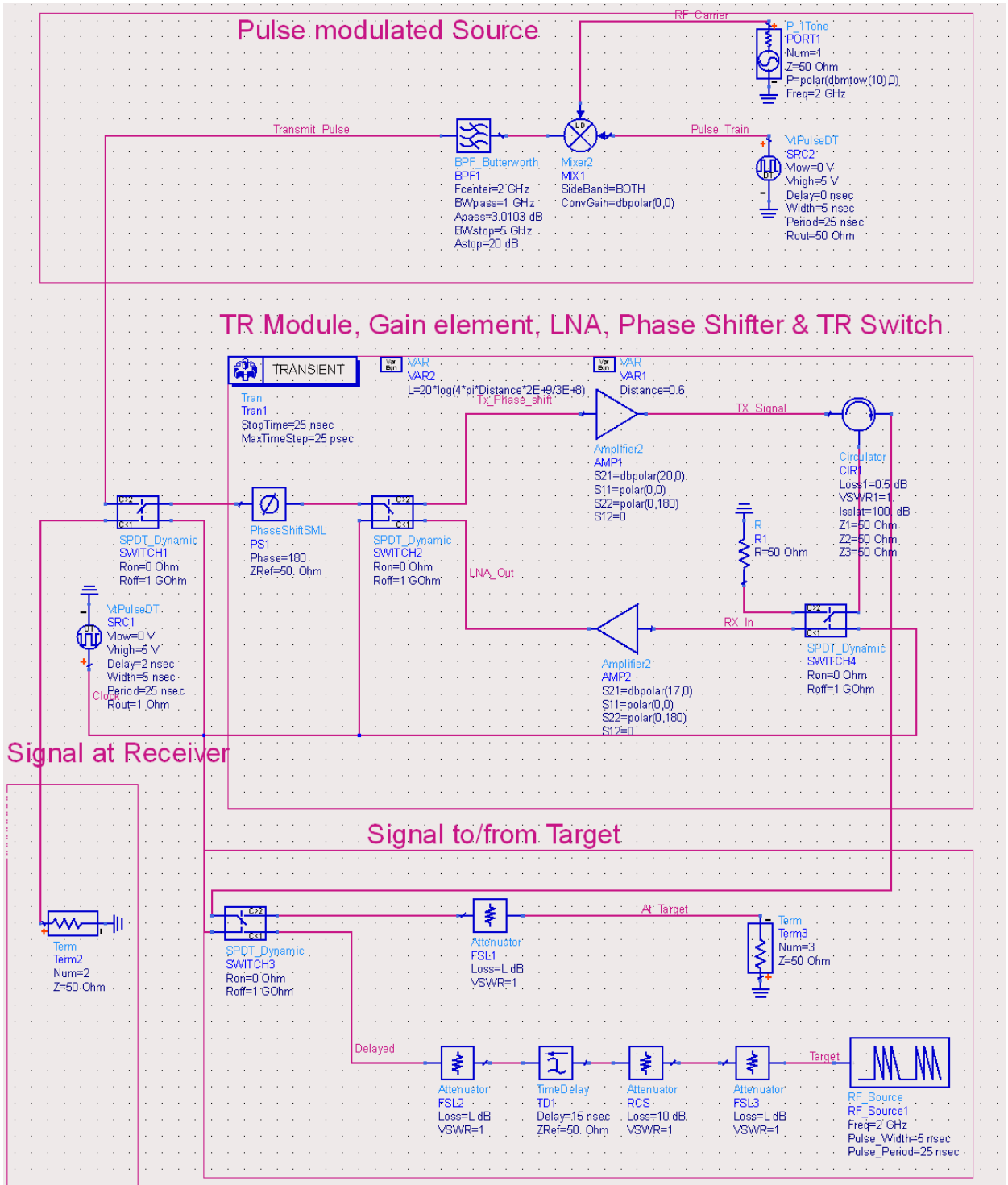
Figure 26: Detailed model of TR module behavioral simulation

2.4 Summary

The chapter is summarized in a research paper published in the proceedings of IEEE International Conference on Emerging Technologies 2011 (ICET 2011) held in Islamabad, Pakistan, on September 5-6, 2011. The paper is titled as;

"Signal Analysis, Design Methodology, and Modular Development of a TR Module"

Chapter 3: Actual Design of the TR Module

State of the art TR modules design and development requires high tech MMIC device simulation and manufacturing technologies. Chapter # 1 presented a brief overview of current research and development in this field. Apart from these resources, such practices take years to produce a working prototype of the modules. In view of these technical requirements, current work focused on a low cost and fast process to design and simulate different components of TR Module on PCB (printed circuit board) laminate and integrate them into a complete module.

In this regard, the key components of the TR module i.e. the phase shifter, TR switch, Gain block and Low noise amplifier (LNA) have been simulated on microstrip. This chapter presents the design process and simulation results of each of the component. The simulated results of the integrated module are also presented afterwards.

3.1   Analysis of Microstrip Substrate used

Commercially available PCB laminate *FR-4* is used as a substrate for simulation the microstrip based circuits. FR-4, made of woven fiberglass cloth with an epoxy resin binder, is selected for this purpose because of the following reasons.

  a.   Readily available commercially used PCB laminate

  b.   Low cost as compared to other high frequency laminates e.g. laminates made by Rogers Corporation

  c.   Circuit fabrication using chemical etching techniques can easily be accomplished using FR-4 substrate

d. The substrate parameters yield moderate sized designs

In this regard, a study has been carried out to analyze the frequency based performance of FR-4. Side feed circular microstrip antennas has been designed at different frequencies from 2 GHz to 10 GHz. The study showed that FR-4 yield close performance between measured and simulated results at lower frequencies of the order of less than 3 GHz. At higher frequencies, even the simulated results of the antennas deviated from the design frequency and the measured results deviated even farther. This study has been summarized in [24].

Besides low cost and easy fabrication, the availability of active and passive components has been another driving factor in selecting the operating frequency is the availability of discrete components like transistors, the pin diodes, surface mount resistors, DC feed inductors and de-coupling capacitors etc. Taking all these parameters into consideration, the TR module constituents are designed and simulated at 2 GHz. Although the design process has also been carried out at 3 GHz but due to unsatisfactory performance of the PIN diodes in TR switch, the frequency was reverted back to 2 GHz.

The substrate parameters used in the simulations in[24] and design process of TR module are presented in Table 2;

Parameter	Value
• Substrate Thickness	1.6 mm
• Dielectric Constant	4.5
• Conductor thickness	35 um
• Conductivity	5.88×10^7 Siemens/meter
• Loss tangent	0.019

Table 2: FR-4 Substrate simulation parameters

The following sections provide a brief design approach followed for each of the sub module.

3.2   Design of Sub-Modules

The designed sub-modules are

   a. Phase shifter

   b. TR switch

   c. High gain block

   d. Low noise amplifier

3.2.1 Phase Shifter

Phase shifters are two-ported devices that alter the phase of an output signal in response to an external signal. Variable phase shifters change the output signal phase by applying variable control signal. There are two basic types of variable phase shifters (a) Analog phase shifters and (b) Digital Phase Shifters.

a. **Analog phase shifters** can provide continuous phase shift from 0 to maximum shift that the device can support. The change in the output phase occurs with a continuous control signal, usually voltage. In turn, the control voltage determines the range in which the device can change the phase of the output signal.

b. **Digital phase shifters** manipulate the signal phase in discrete steps. The number of bits in the control signal determines resolution of the device. If n equals the number of bits in the digital control signal, then the number of output states (phase changes) is 2^n and device resolution equals $360^0/2^n$.

Performance specifications of RF phase shifters include frequency range, phase shift range, insertion loss, input voltage standing wave ratio (VSWR), and input power.

3.2.2 Phase Shifter Types and Design

The phase shifters are classified into two broad categories;

1. Diode based Phase Shifter
2. Ferrite based Phase Shifter

3.2.2.1 Diode based Phase Shifter

The main principle of Diode Phase shifters is that PIN diodes are usually used to switch elements in or out of the network. This switching allows signal to propagate through different states of the circuit with each of the stage can introduce a fixed amount of phase shift. PIN diode based phase shifters are digital phase shifters.

Another type of diodes used to design analog phase shifter. VARACTOR Diodes operating in reverse biased state offer voltage dependent junction capacitance. The variations in capacitance produce phase shift in the circuit. The VARACTOR based phase shifters are smaller in size but suffers from low power handling capability of the diodes. Diode Phase shifters are typically designed by using one of three techniques:

    a. Switched Line

    b. Hybrid Coupled

    c. Loaded Line

a. Switched Line Phase Shifter

Switched line phase shifters are the simplest of digital phase shifters. They are simply based on time delay approach to introduce the desired phase shift by switching between the two paths. PIN diodes are often used as switching elements.

Among the two lines, one is called the reference line "I" and the other is called the delay line "II".
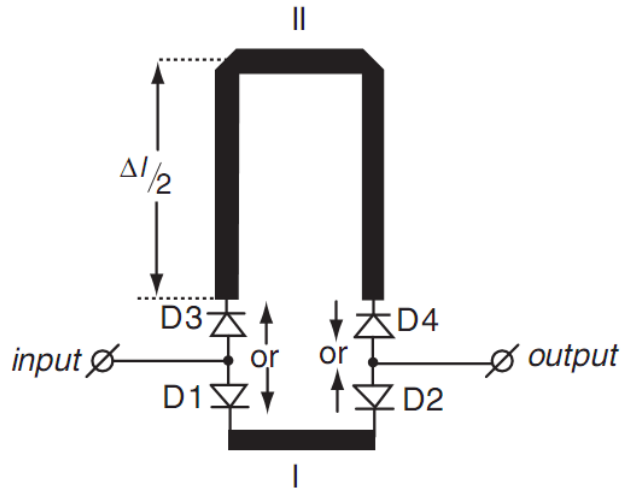
Figure 27: Switched line phase shifter

The relative phase shift between the two lines depends upon the path difference ΔL between them.

$$\Delta\Phi = 2\,\pi\,\frac{\Delta L}{\lambda}$$

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Depending on the application, any number of phase shifting sections can be cascaded and the resolution of the device depends upon the number of sections.

b. **Hybrid Coupled Phase Shifter**

The hybrid-coupled (reflection type phase shifter) technique uses a microwave hybrid and effectively changes the distance at which the reflection takes place. This technique is usually used in binary increments, and two diodes are required for each phase state. The phase shifting mechanism is described in detail in chapter 4.
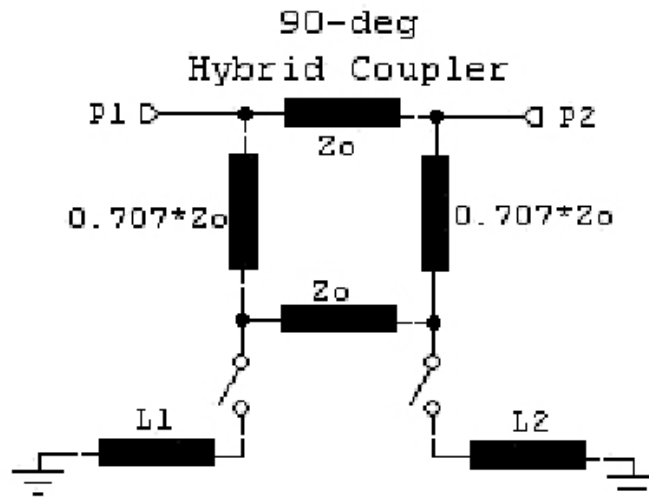
Figure 28: Hybrid Coupler phase shifter [25]

The diode phase shifters described above is limited in its ability to handle high power levels. Depending on size and frequency, the devices are normally restricted to power levels of less than 1 kW. For higher power levels, the loaded-line technique is used.

c. Loaded Line Phase Shifter

Loaded line phase shifters work by switching symmetric pair of reactance connected in shunt to a section of transmission line. The separation between the reactive elements is $\lambda/4$ such that the reflections due to reactance are out of phase at the input terminal and hence cancel each other.
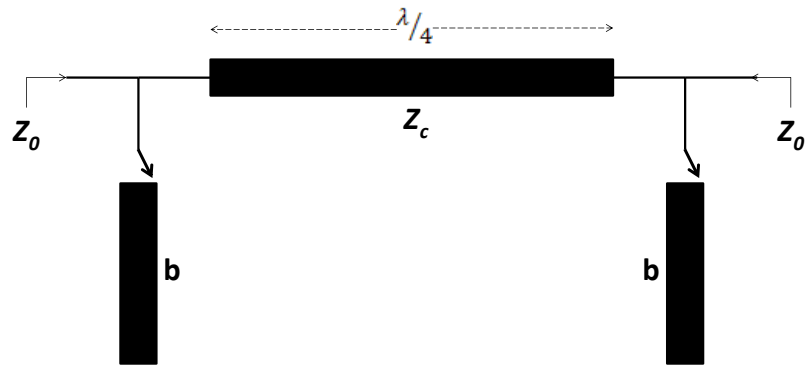
Figure 29: Loaded line phase shifter

The characteristic impedance and the phase variations are mathematically shown as;

$$b = \tan{^{\Delta\Phi}/_2} \qquad\qquad\qquad \textbf{17}$$

$$z_c = z_0 \cos{^{\Delta\Phi}/_2} \qquad\qquad\qquad \textbf{18}$$

The loaded line phase shifters have simplicity in their structure but are limited in steering the phase values by less than 90^0[26].

3.2.2.2 Ferrite based Phase shifter

The ferrite phase shifters are nonreciprocal devices, and use discrete lengths of ferrite to implement each of the bits (180°, 90°, 45°, etc.). In these devices, a current pulse is passed through each bit which saturates the ferrite **toroid**. When the current is removed, the ferrite **toroid** is said to be latched and retains its magnetization owing to its hysteresis properties. If the current is in a forward direction, the ferrite is latched with a particular phase (e.g., 180°). The ferrite maintains the phase until a current pulse in the opposite direction is applied. The ferrite phase shifter is then latched to the reference phase (0°). This

change in phase with a change in current direction is due to the nonreciprocal nature of the device. The ferrite devices are heavier and bulkier diode based devices.
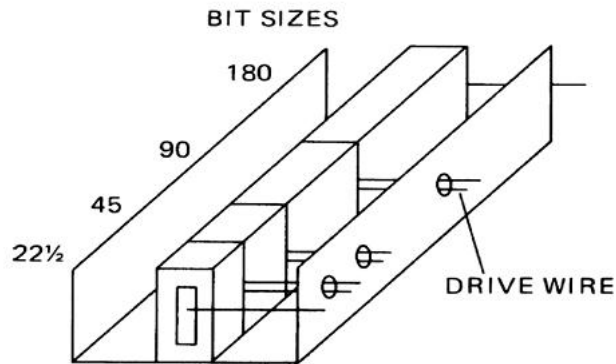
Figure 30: Digital ferrite phase shifter using Toroids

3.2.2.3   Analog Phase Shifter design

A 3-dB quadrature coupler based analog phase shifter has been designed and simulated for TR module. The major elements of such a phase shifter are;

    a. 3-dB Hybrid Coupler

    b. Varactor Diode

a.   3-dB Hybrid Coupler/ Branch line coupler

Directional couplers are used frequently in dividers, combiners, attenuators, phase shifters, discriminators, balanced and double-balanced mixers, balanced amplifiers, and feed networks in antenna arrays.

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A directional coupler is a reciprocal four-port device, which provides two amplitude outputs when a signal is applied to its input.

A hybrid network (or 3-dB directional coupler) is a special class of directional coupler in which the signals at the two output ports are equal.

The important characteristics of directional couplers are coupling, directivity, isolation, matching, insertion loss, phase balance, power split, and bandwidth.

i.   **Coupling (C):**

Coupling (C) is calculated as the ratio in decibels of the incident power fed into the input port of the directional coupler, to the coupled port power of the auxiliary line when all ports are terminated by reflection less terminations. Coupling tolerance is the allowable unit to-unit variation in nominal coupling as specified. Coupling flatness is the amount (in decibels) of the maximum variation in coupling that may be expected over a specified frequency range.

ii.   **Insertion loss:**

Insertion loss is the ratio (in decibels) of input power and output power of the main line with reflection less termination connected to ports of the directional coupler.

iii. Directivity:

Directivity is calculated as the ratio (in decibels) of power at the coupled port and at the isolated port when all ports are terminated by reflection less terminations.

An ideal directional coupler have infinite directivity however in an actual directional coupler, the isolated port is never completely isolated due to mismatching of terminations, losses, discontinuities, and tolerances.

iv. Isolation:

Isolation is the ratio in decibels of power at an isolated port to available power at the input port. Isolation is equal to the sum of the coupling and directivity. The branch line coupler has the design model as shown in Figure 31;
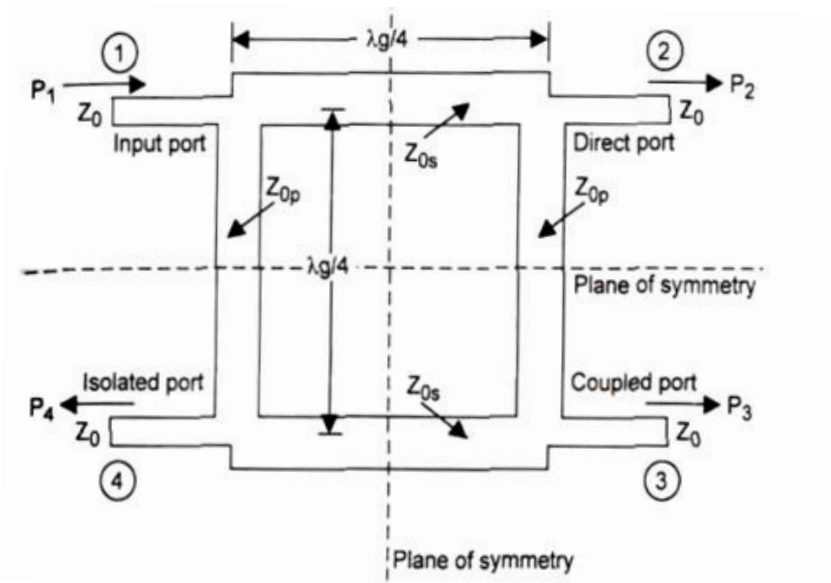
Figure 31: Branch line coupler

Detailed analysis of this coupler has been presented in [27]. The

basic design relations for a generalized branch line coupler are

presented here.

$$S_{21} = -j\,\frac{z_{0s}}{z_0} \qquad\qquad \textbf{19}$$

$$S_{31} = -j\,\frac{z_{0s}}{z_{0P}} \qquad\qquad \textbf{20}$$

$$S_{11} = 0 \qquad\qquad \textbf{21}$$

$$S_{41} = 0 \qquad\qquad \textbf{22}$$

The scattering matrix for a symmetric structure is expressed as;

$$[S] = \begin{bmatrix} 0 & -j\,\dfrac{z_{0s}}{z_0} & -j\,\dfrac{z_{0s}}{z_{0P}} & 0 \\[2mm] -j\,\dfrac{z_{0s}}{z_0} & 0 & 0 & -j\,\dfrac{z_{0s}}{z_{0P}} \\[2mm] -j\,\dfrac{z_{0s}}{z_{0P}} & 0 & 0 & -j\,\dfrac{z_{0s}}{z_0} \\[2mm] 0 & -j\,\dfrac{z_{0s}}{z_{0P}} & -j\,\dfrac{z_{0s}}{z_0} & 0 \end{bmatrix} \qquad\qquad \textbf{23}$$

If the structure is assumed to be loss less, equations **19** and **20**

yield;

$$S_{21}{}^2 + S_{31}{}^2 = 1 \qquad\qquad \textbf{24}$$

$$\frac{z_{0s}{}^2}{z_0} + \frac{z_{0s}{}^2}{z_0} = 1 \qquad\qquad \textbf{25}$$

For 3.0 dB coupling, and the characteristic impedance value of

50 Ω,

$$|S_{21}| = 0.5 \ or - 3.0 \ dB \qquad\qquad \textbf{26}$$

$$|S_{31}| = 0.5 \ or - 3.0 \ dB \qquad\qquad \textbf{27}$$

$$Z_{0S} = 0.707 \ Z_0 = 35.4 \ \Omega \qquad\qquad \textbf{28}$$

$$Z_{0p} = 50 \ \Omega \qquad\qquad \textbf{29}$$

The model in Figure 31 reduces to;
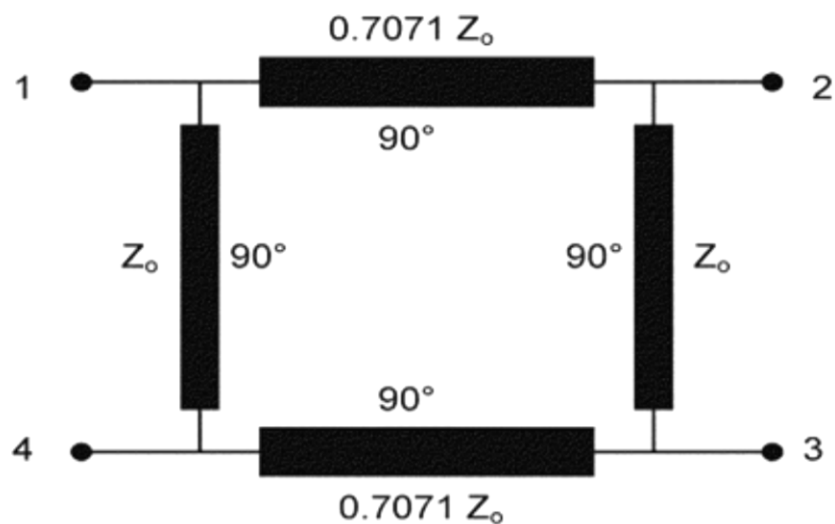
Figure 32: 3-dB branch line coupler

b. **Varactor Diode**

One important characteristic of any PN junction is an inherent capacitance. When the junction is reverse biased, increasing the applied voltage causes the depletion region to widen, thus increasing the effective distance between the two "plates" of the capacitor and decreasing the effective capacitance.

By adjusting the doping gradient and junction width, the capacitance range and capacitance variation profile can be

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controlled. A four-to-one capacitance range is easily achieved; e.g. a typical varactor diode (sometimes called a "varicap diode") might vary from 60 Pico farads (pF) at zero bias down to 15 pF at 20 volts.

Varactor diodes are used in electronic tuning systems, to eliminate the use of and need for moving parts.

3.2.2.4 Simulation Model and Results

As per the simulation parameters of the TR module behavioral simulation, the module's components designed on the same lines. This section describes the ADS simulation model of the varactor based phase shifter.

The Figure 33 shows the ADS schematic.
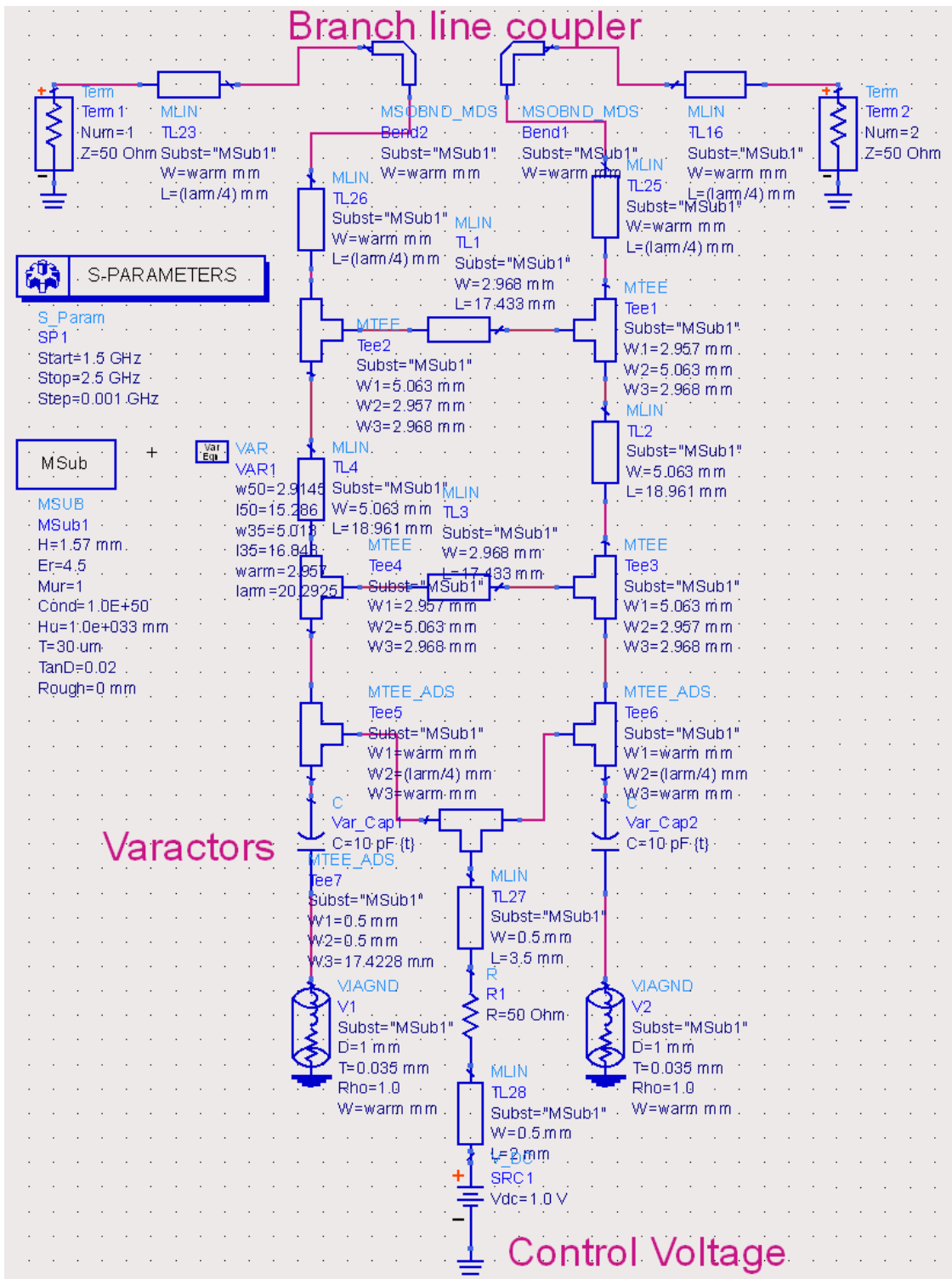
Figure 33: Analog phase shifter simulation model

S-Parameter simulation has been performed for the device. The simulated results mainly depict the return loss i.e. the input impedance

mismatch, insertion loss and the phase of the signal from input port to the output port.
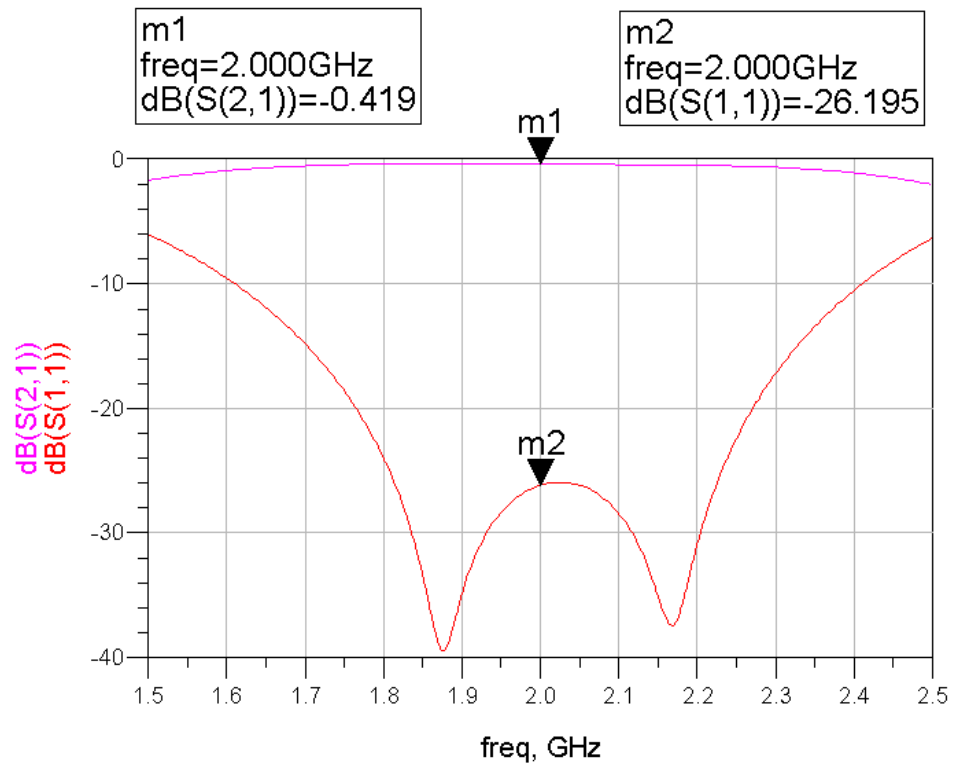
Figure 34: Return loss and Insertion loss of the Phase Shifter

The simulation results are such that;

- The insertion loss indicated by marker *m1* is 0.419 dB.

- The return loss values of the order of less than -20 dB indicate a close match to the port impedances of 50 ohm over the band of 500 MHz

- The current design has this range of approximately 168^0 i.e. as shown in Figure 35, the phase response of the device shows a variation from 158.90^o to -9.70^0 when the capacitance is varied from 0.1 pF to 30 pF

Commercial analog phase shifting products have the insertion loss values ranging from 1 to 3dB. However those products have full phase shifting range i.e. 0-360^0.

In order to increase this range, a cascade of the design module can be used but that configuration increase the insertion loss to higher values.
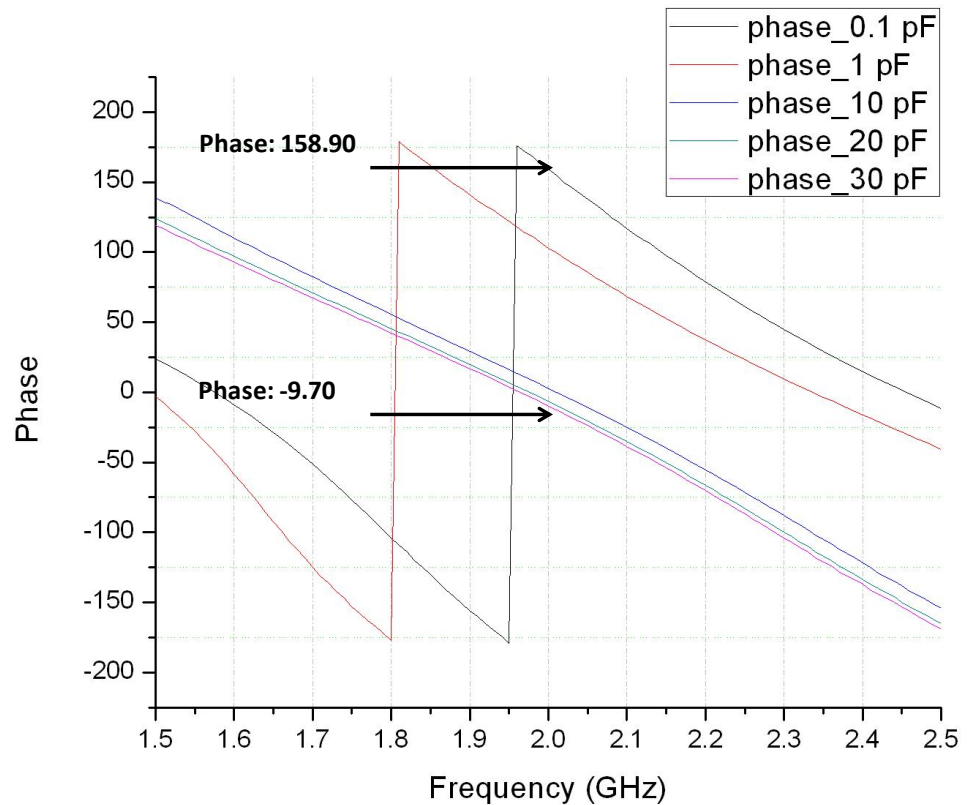
Figure 35: Phase Variations of the Phase Shifter

3.2.3 TR switch

One of the most important building blocks of today's wireless communication is RF switches. An RF switch routes high frequency signals between different devices or different ports of the same device. Most important parameters are of any RF switch are;

    a. High **isolation** between the alternate paths

    b. Low **insertion** loss

c. High-**power handling** and

d. Fast switching.

a. Isolation:

Isolation is defined as the ratio of the power level in the path where the switch's is "OFF" to the power level where the switch is "ON". Good isolation prevents the stray signals from leaking into the desired signal path. If these stray signals are allowed to get through, measurement integrity is severely compromised.

b. Insertion Loss:

Insertion loss, expressed in decibels (dB), of a switch is determined by measuring the power loss of a signal that is sent in through the common port and out from the port that is in the "ON" state.

Insertion loss plays an important role in many applications. In receiver applications, the effective sensitivity and dynamic range of the system is lowered by insertion loss. In system applications where the additional power needed to compensate for the loss is not available (amplifiers in particular), insertion loss will be a critical specification of a switch.

c. Power Handling:

The power handling ability of a switch refers to the operation of the switch at higher powers. The vertical structure of a PIN diode is a relative advantage for power handling. The heat that is generated by Joule heating within the intrinsic layer of the diode

can easily be conducted downwards through the diode's cathode layer to the system heat sink.

3.2.3.1 TR Switch Design Topologies

Depending on the application, RF switches are classified into different categories;

a. **Single pole single throw (SPST)**

As evident from its name, the SPST switch can only be used to turn the RF signal ON or OFF.

b. **Single pole double throw (SPDT)**

SPDT switch switches an RF signal between one of the two paths. The signal from the common port (single pole) is switched between any of the two ports (double throw).

c. **Double pole double throw (DPDT)**

A DPDT throw switch can route signals from two input ports to two output ports.

PIN diodes are used to design the RF switch. Before the details of TR switch are presented, the following paragraph describes the basics of PIN diodes.

3.2.3.2 PIN Diodes

The PIN diode doesn't actually have a junction at all. Rather, the middle part of the silicon crystal is left undoped. Hence the name for this device: P-Intrinsic-N, or P-I-N. Because this device has an intrinsic middle section, it has a wide depletion region when unbiased.

However, when a forward bias is applied, current carriers from the P-
and N-type ends become available and conduct current even through
the intrinsic center region. The end regions are heavily doped to
provide more current carriers. Major applications of PIN diodes
include RF switches, Attenuators etc.

3.2.3.3   SPDT Switch design topologies

Since the TR switch in a Transmit/ Receive Module is required to
connect the common port signal to either of transmit or receive paths,
Single pole double throw (SPDT) is designed for the TR module.
Based upon different design parameters of the switch design and
configuration of the PIN diodes, the SPDT switched are further
categorized in three topologies.

    a. Series SPDT switch

    b. Shunt SPDT switch

    c. Series-Shunt SPDT switch

    a. Series SPDT switch

In series SPDT switch, the PIN diode is connected in series
to the RF path. The bias control voltages 'Va' and 'Vb' turn
ON or OFF the respective diodes which in turn connects the
TX or RX port to the RF port. Since the PIN diodes have
low ON state resistance, the series topology has a low
insertion loss profile.
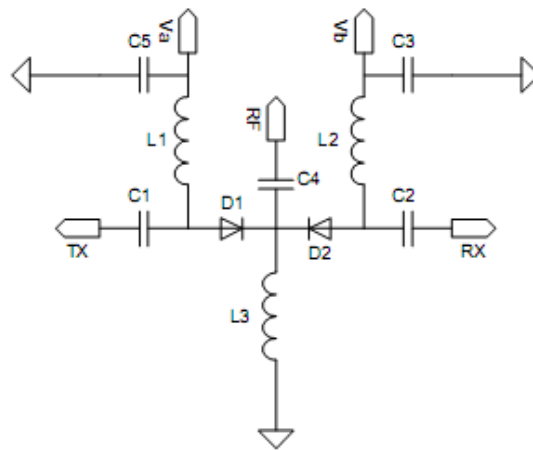
Figure 36: Series diode SPDT switch[28]

b. **Shunt SPDT switch**

Shunt SPDT switch employs PIN diode in shunt configuration with quarter wave transmission lines connecting each of the TX or RX port to the RF port. This configuration is suited for its high isolation characteristics and the quarter wave transmission lines are critical in achieving this property.
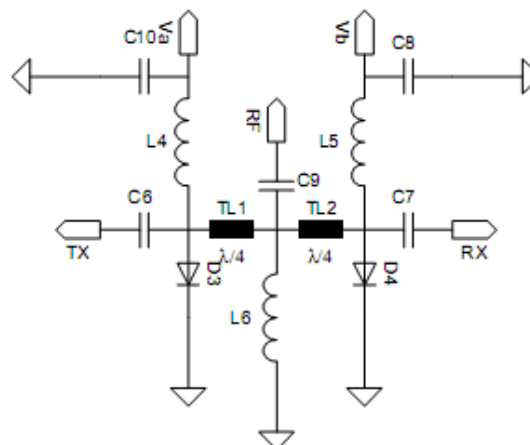
Figure 37: Shunt Diode SPDT switch[28]

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c. Series-Shunt SPDT switch

The series-shunt diode configuration employs both the series and shunt configuration of the PIN diodes and excels in both low insertion loss and high isolation.
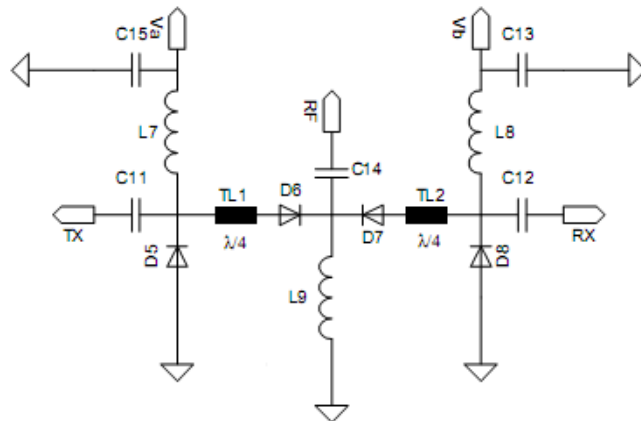
Figure 38: Series-Shunt diode SPDT switch[28]

3.2.3.4 Transmission line theory

The transformation of impedance from one end of the transmission line to the other is the basic concept used in SPDT switches. Since the biasing of PIN diodes effectively leaves the quarter wave transmission lines open or short circuited to the ground, only these two scenarios are discussed.

(a) **(b)**

Figure 39: (a) Open termination line, (b) Short termination line

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a. **Open termination quarter wave transmission line**

The input impedance of the open circuited transmission
line is;

$$Z_{in} = j\, Z_0 \cot(\beta\ell) \qquad\qquad 30$$

The propagation constant is;

$$\beta = {}^{2\,\pi}/_{\lambda} \qquad\qquad 31$$

If the length of this line is ${}^{\lambda}/_{4}$, $\beta\ell = {}^{\pi}/_{2}$ and the
input impedance becomes $Z_{in} = 0$, i.e. the open
termination in a quarter wave transmission line is
transformed into a short circuit at the input.

b. **Shorted termination quarter wave transmission line**

Similarly, the input impedance of the short circuited
transmission line is;

$$Z_{in} = j\, Z_0 \tan(\beta\ell) \qquad\qquad 32$$

For a line of length ${}^{\lambda}/_{4}$, $\beta\ell = {}^{\pi}/_{2}$ and the input
impedance becomes $Z_{in} = \infty$, i.e. the short termination
in a quarter wave transmission line is transformed into
an open circuit at the input.

In view of the above transmission line analysis, when the TX bias
voltage is at high potential, the shunt diode D5 becomes open and
transforms the quarter wave transmission line to zero impedance at the

input of series diodeD6. On the other hand, the low bias at RX port makes the D8 forward biased and D7 reversed biased. The forward biased D8transforms the short circuit into open circuit at D7 and enhance the isolation already provided by D7.

The following section presents the design and simulations of the TR switch.

3.2.3.5   TR Switch Design and Simulation Results

Figure 38 is revisited below with more detail. The values of respective inductors and capacitors as used in simulation are highlighted in the simulation schematic.

The 100pF capacitors shown on the circuit diagram are the DC block capacitors i.e. these capacitors are preventing the DC currents from flowing towards the TX, RX and RF ports. Similarly the low pass combination of 100μF capacitor and 100μH inductor prevents the DC control DC circuitry from being damaged by the high power RF signals.

The insertion loss and isolation plots of the designed switch are displayed in Figure 41with blue and red plots displaying the insertion loss and isolation respectively. As marked the switch has a very low insertion loss i.e. -0.46 dB and an isolation value of -22dB.These values fall in close limits to some of the designed products available e.g. in [28] these parameters for SPDT switch have values of < 0.65dB and >18dB respectively.
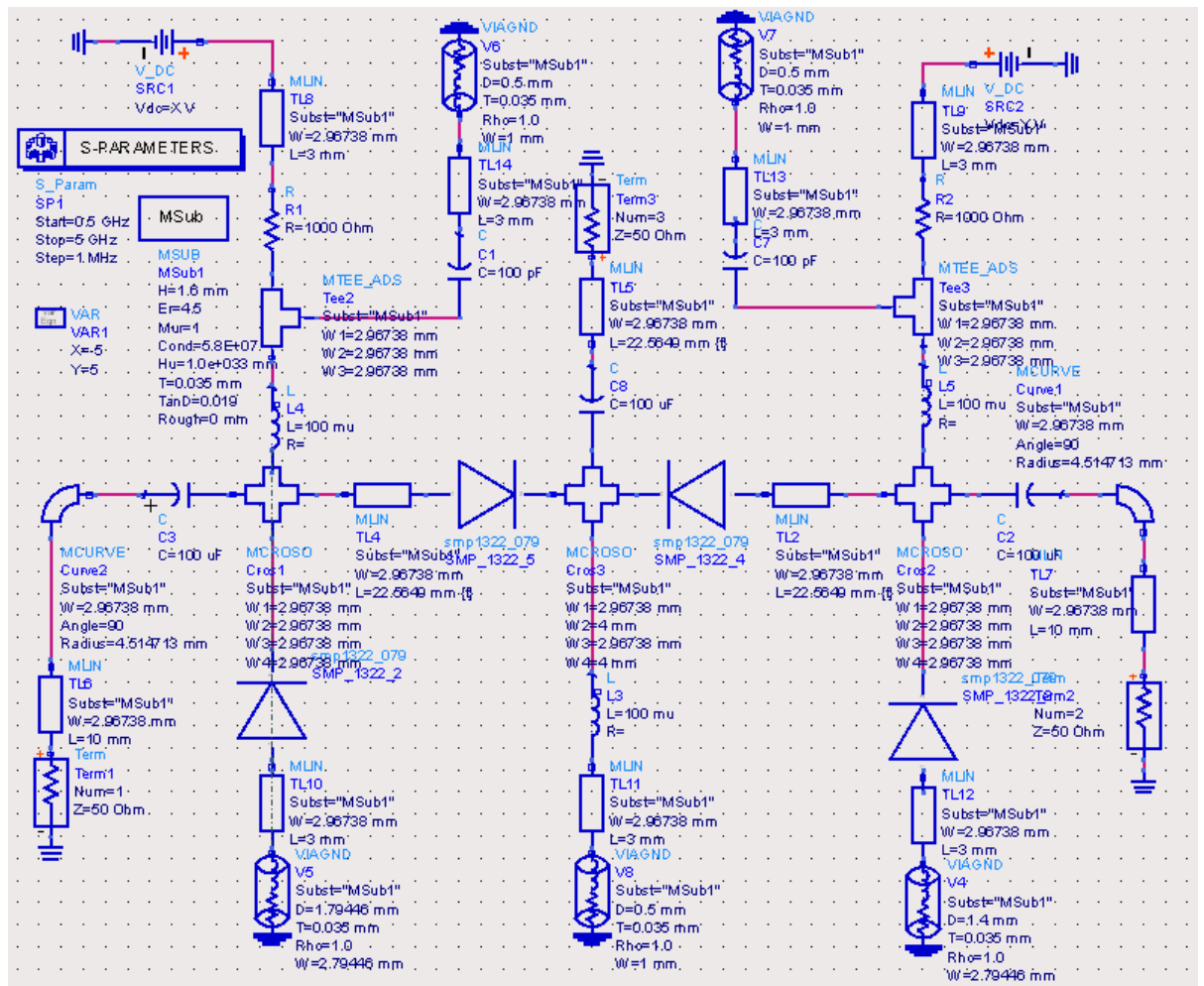
Figure 40: Simulation schematic of a TR switch
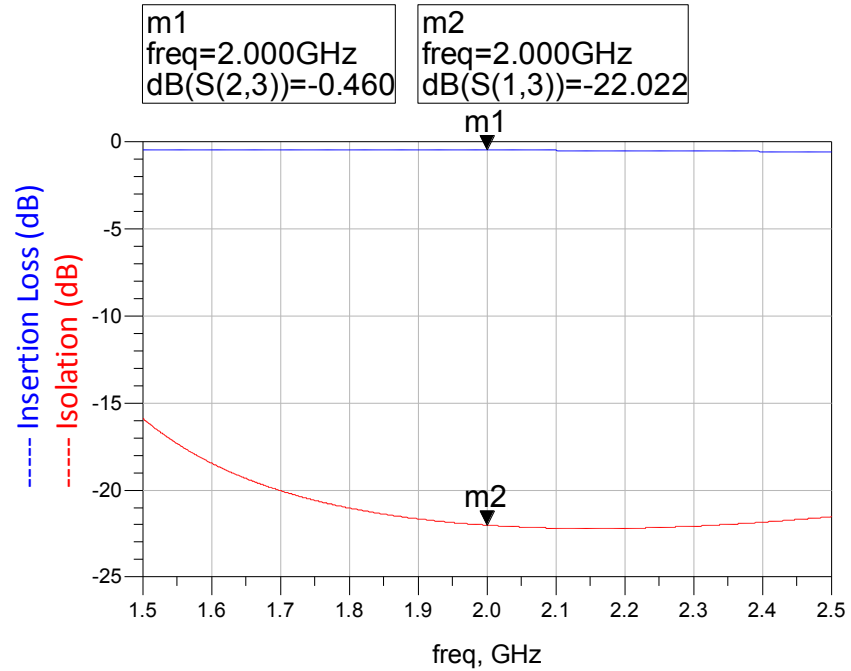
Figure 41: Insertion loss and isolation of TR switch

The section has comprehensively presented a design methodology of the TR switch. The amplification blocks of the TR module i.e. High gain block and low noise amplifier design methodology is presented in the next section.

3.2.4 Amplification Modules

The amplification modules involved in TR module include a High gain amplifier in the transmit path and a low noise amplifier in the receive path. Before the design details of each of the sub-module are presented, it is customary to present some theoretical concepts common to both and then building upon these concepts the design and simulations presented afterwards.

A design model of any microwave amplifier is based upon the following model;

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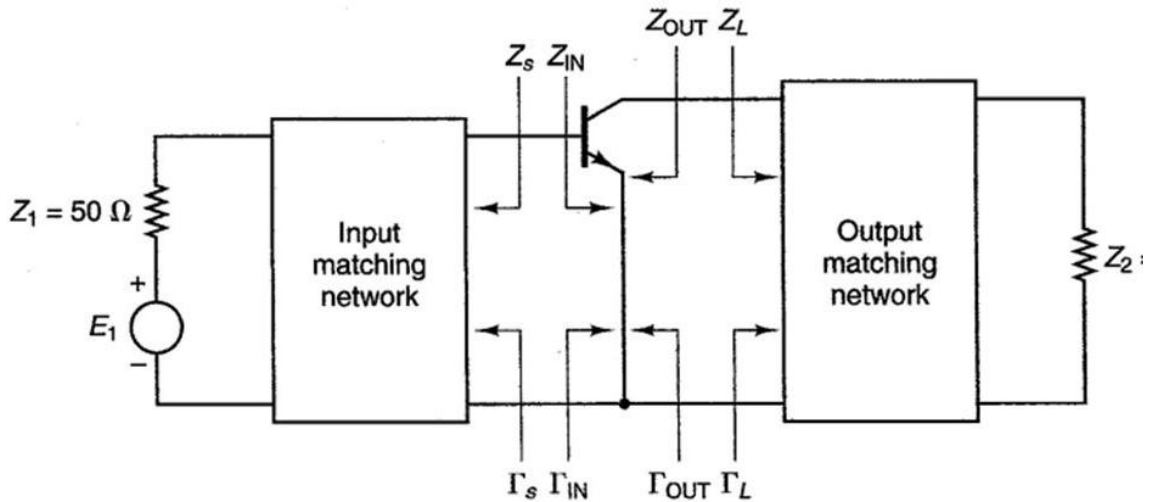
Figure 42: Design model a Microwave Amplifier

Some of the parameters used to design amplifier as per the model in Figure 42are described below;

- P_{IN}Power input to transistor or to input matching network

- P_{AVS}Power available from source under source matched condition

- Matched conditions at the source means that$\Gamma_{IN} = \Gamma_S^*$

- P_LPower delivered to load or output matching network

- P_{AVN}Power is available from transistor under output matched condition

- Matched conditions at the load means that$\Gamma_{out} = \Gamma_L^*$

The amplifier design process has been described in depth in [29], this section presents the brief/ summarized concepts.

3.2.4.1   Gain

It is the ratio of output power of a system to the input power. There are different types of gain which are as follows;

- **Power Gain**

It is the ratio of output power to the input power.

$$G_p = {P_L}/{P_{IN}} \qquad \text{33}$$

- **Available Power Gain**

It is the ratio of power available from load under matched condition to the power available from the source under matched condition.

$$G_A = {P_{AVN}}/{P_{AVS}} \qquad \text{34}$$

- **Transducer Power Gain**

It is the ratio of power delivered to the load to the power available from the source under matched conditions.

$$G_T = {P_L}/{P_{AVS}} \qquad \text{35}$$

- **Maximum Gain**

Maximum gain is achieved when conjugate matching is done i.e.

$$\Gamma_{IN} = \Gamma_S^* \qquad \text{36}$$

$$\Gamma_{IN} = \Gamma_S^*$$

3.2.4.2 Stability

It is the ability of a device to satisfy BIBO (bounded input bounded output) criterion.If the transistor is not stable it will tend to oscillate.In order to check the stability of a transistor K-Delta test is used where

- **K-Delta test**

Given the S-parameters of a transistor, delta is given as;

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| \qquad\qquad \textbf{37}$$

K is given as under;

$$K = \frac{1 - |S_{11}|^2 + |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \qquad\qquad \textbf{38}$$

If $K > 1$ and $\Delta < 1$ the transistor is said to be unconditionally stable.

3.2.4.3 Noise

Noise is unwanted electrical or electromagnetic energy that degrades the quality of signals and data. Noise is especially considered in low noise amplifier (LNA) design. The LNA, as the name implies has a minimal impact on the signal in terms of adding noise and noise contribution is considered in its design process.

More specifically it is actually a measure of reduction in signal to noise ratio of the system.

F= Signal to noise ratio at the input / Signal to noise ratio at the output

$$F = \frac{S_i/N_i}{S_o/N_o} \qquad\qquad \textbf{39}$$

The design process of both LNA and high gain amplifier comprise of several stages. Some of the design steps are as under;

- DC Biasing of the transistor
- Matching network design at the input
- Matching network design at the output

All these stages follow an indepth design methodology and often the process is summarized in a single report. Since the objective of current work is not to highlight and report the design methodology, the following section presents only the final simulation model of the respective modules.

Before the simulation results of the two modules are presented, the following figures Figure 43 and Figure 44presents the stability plots of the two transistors used in low noise amplifier and high gain amplifier's simulation. The figures show that the tow transistors are indeed stable and fulfill the K-Δ stability criterion.
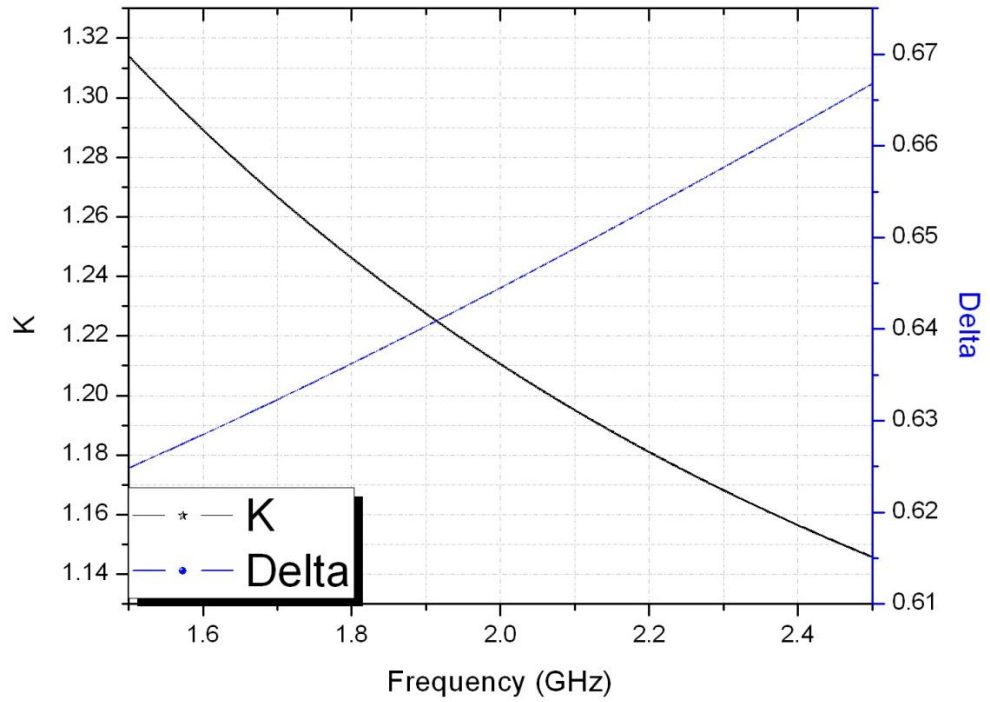
Figure 43: LNA transistor (ATF-36163) stability
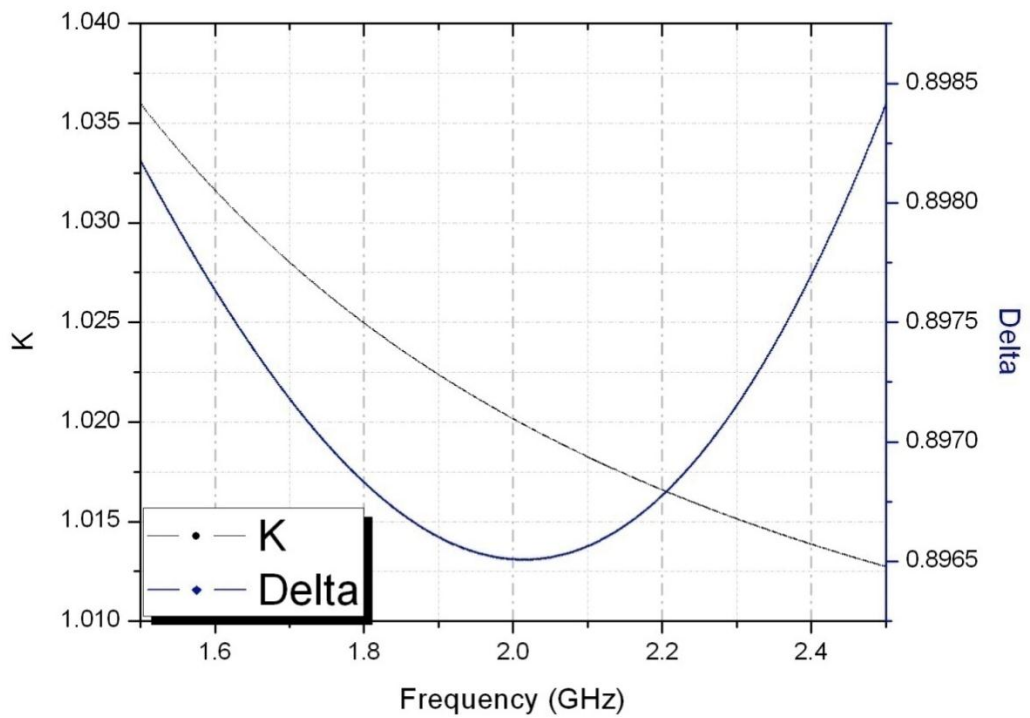
Figure 44: HGA tansistor (ATF-36163) stability

3.2.4.4 LNA Design and Simulation Results

The transistor used to design the Low noise amplifier is **Avago'sATF-36163**which is a low-noise PseudomorphicHigh Electron Mobility Transistor(PHEMT). The device datasheet is attached in appendix for more detailed parameters. The simulation schematic of the module is shown in Figure 45
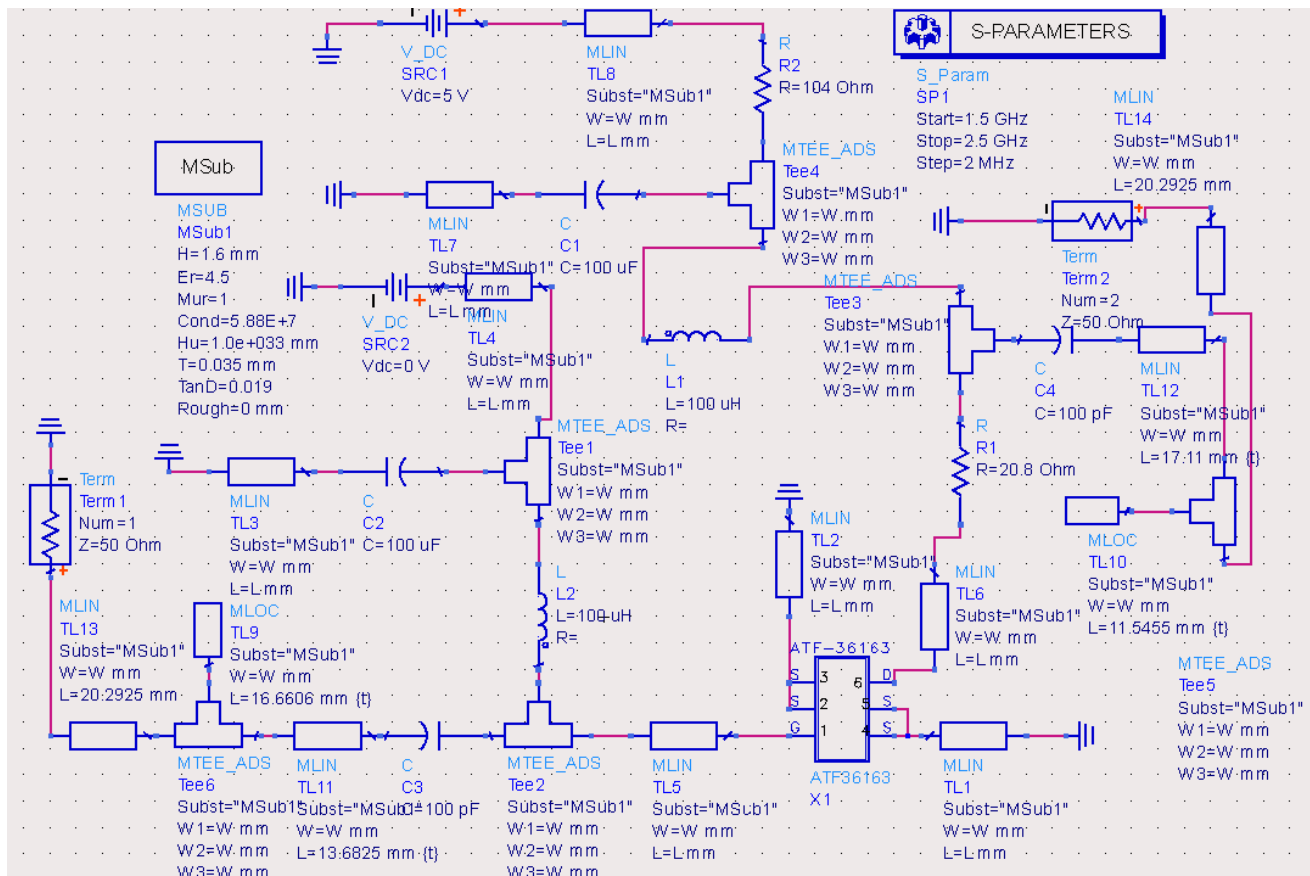
Figure 45: LNA simulation model

The following figures present the simulation results of the module.

All the figures are self explanatory and are commented where necessary.
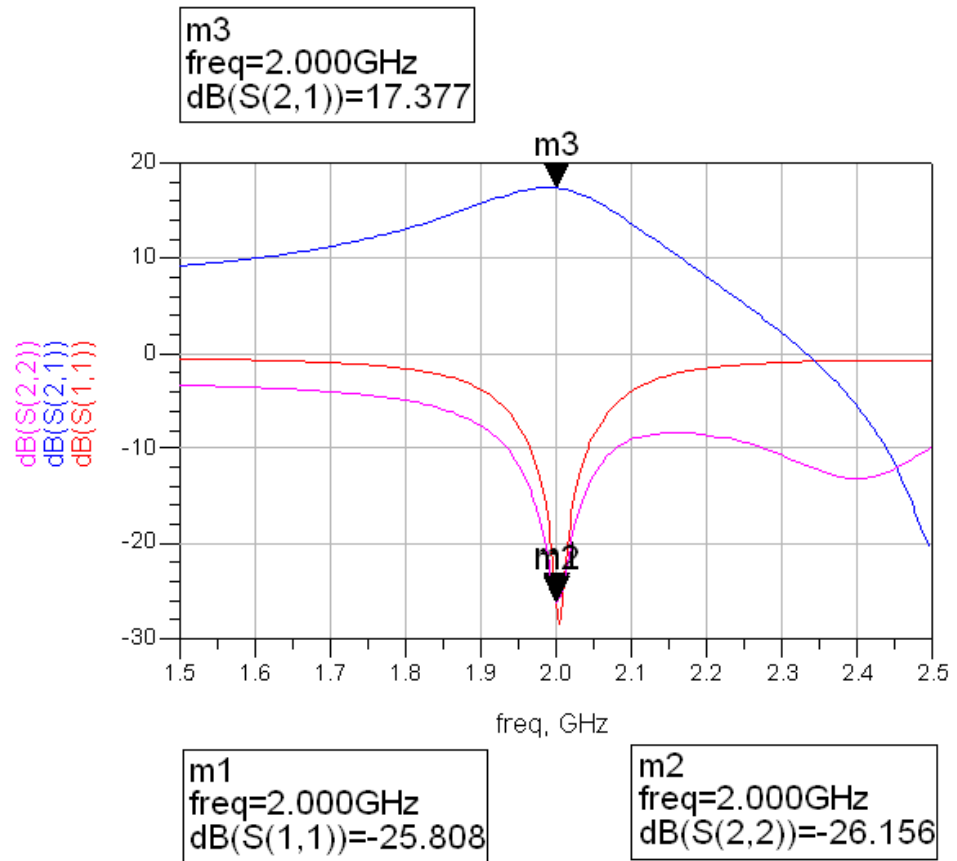
Figure 46: LNA gain and input/ output matching

Markers *m1* and *m2* highlight the input and output reflection coefficient values. Typically values of the order of less than -10 dB are acceptable. The results however show that the device input and output is closely matched to 50 ohm terminations. Following figure present this impedance matching characteristic on *Smith Chart.* The device gain is highlighted by *m3.*
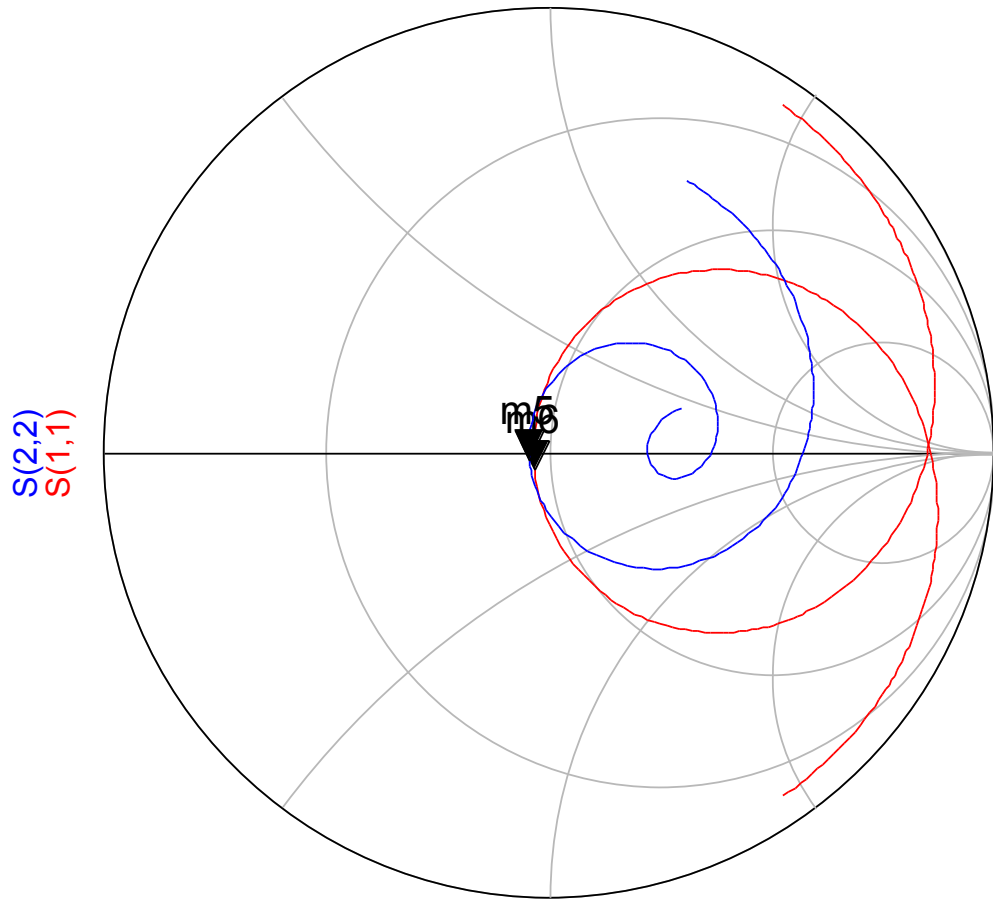
freq (1.500GHz to 2.500GHz)

```
m6
freq= 2.000GHz
S(1,1)=0.051 / -133.749
impedance = Z0 * (0.929 - j0.069)
```

```
m5
freq= 2.000GHz
S(2,2)=0.049 / -163.455
impedance = Z0 * (0.910 - j0.026)
```

Figure 47: LNA Input/ Output impedance matching on Smith Chart

Since LNA **Noise Figure** is an important figure of merit. Figure 48display this parameter.
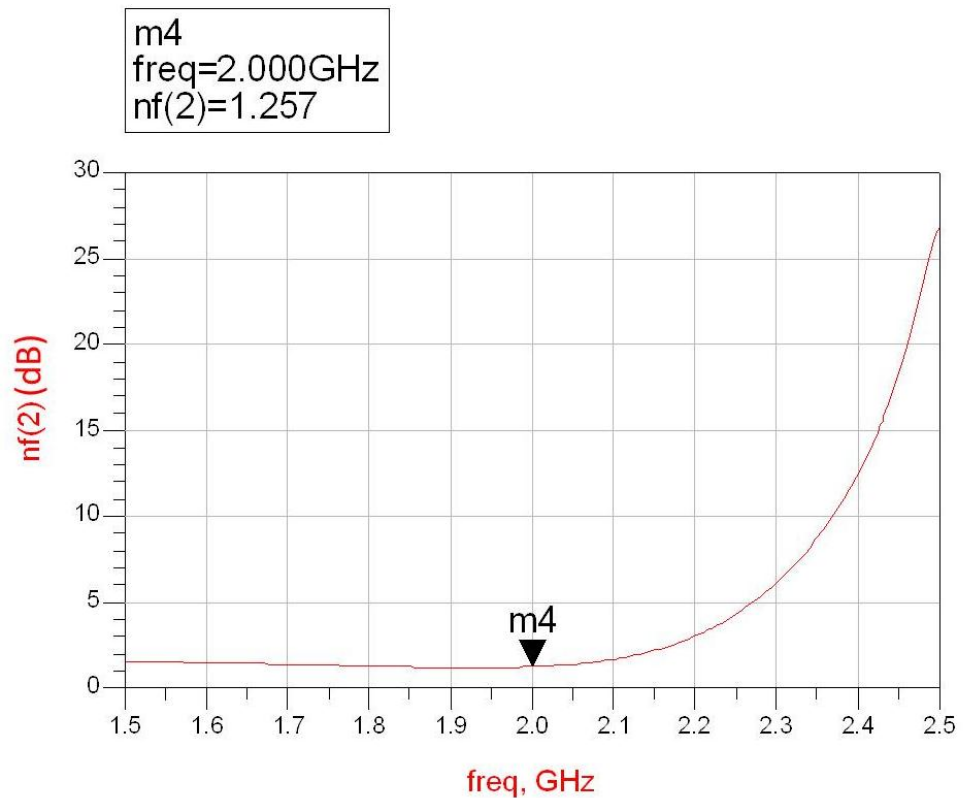
Figure 48: LNA noise figure

The noise figure values of the amplifier are also on the lower side as the minimum value that can be obtained by the transistor itself is0.6 dB.

3.2.4.5   High Gain Amplifier design and Simulation Results

Avago'sATF-36163is used to simulate the High Gain Amplifier (HGA). Achiving maximum possible gain being the design objective for HGA, cascade topology is used to design and simulate the block. Just like the LNA simulation results, the section describes the simulation results of the HGA. The simulation schematic of the module is shown below in Figure 49
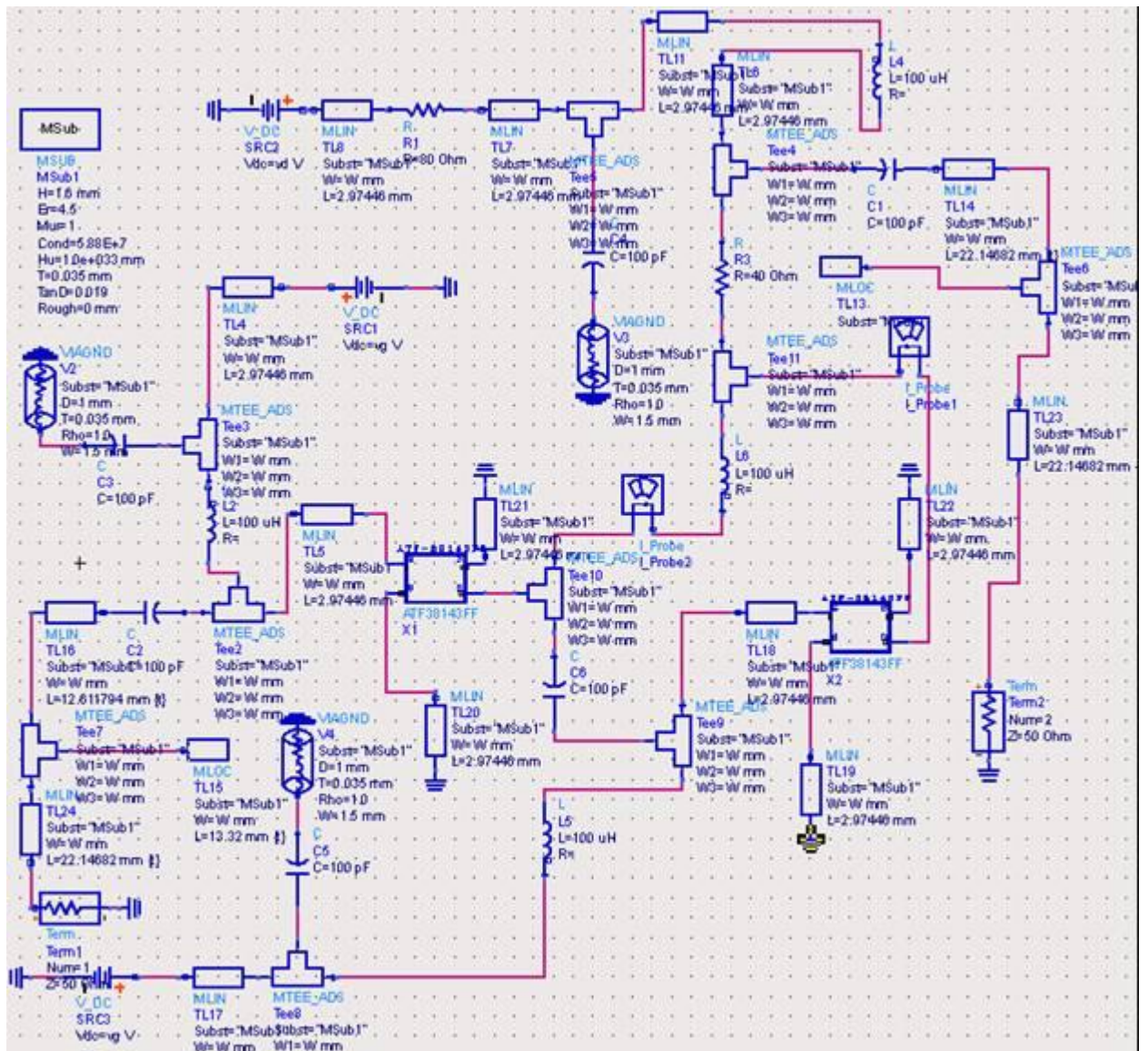
Figure 49: High gain amplifier (HGA) simulation model

The IO matching and gain of the amplifier is as under;
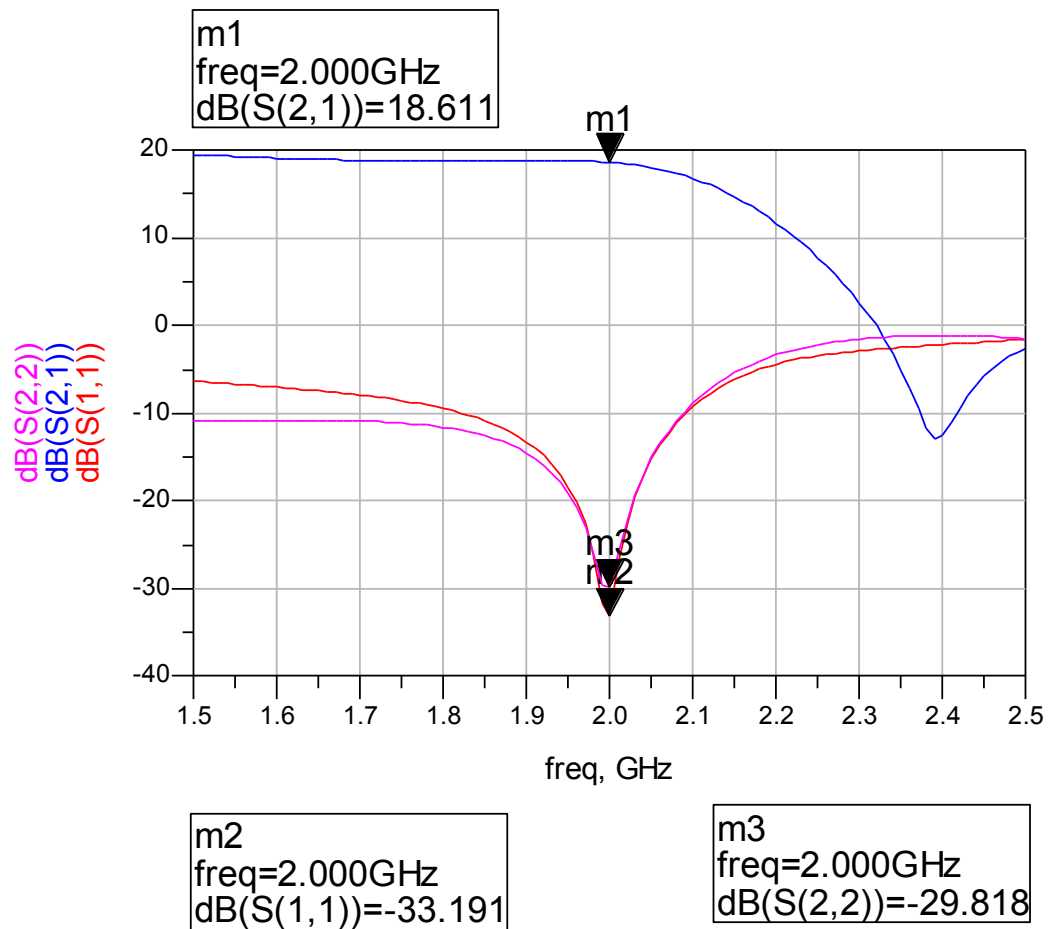
Figure 50: HGA Gain and input/ output matching

The amplifier has a high gain value indicated by *m1* at the design frequency. Similarly the input/ output matching characteristics are even better than that of the LNA. The HGA deals with relatively high power signals therefore the output matching becomes important as the poor match would cause unwanted reflections particularly at the output port hence reducing the efficiency of the system.

The impedance matching values are also displayed on the **Smith Chart** below;

Figure 51: HGA Input/ Output impedance matching on Smith Chart

Section 3.2, elaborated the design methodology of the sub modules of

the TR module. Another design element of the module could have been

the RF circulator or the duplexer. But since the module required non reciprocal ferrite material for its modeling requiring 3-D structure modeling, the ADS circulator model is used in the integrated module design and simulations.

Next section describes the integration of the TR module and the simulation results of the integrated module.

3.3   Integrated TR Module

Section 3.2 presented a detailed overview of the TR Modules component's design and simulation. The results fall in close agreement of the design frequency along with good input and output impedance matching. This section presents the integrated TR module schematic and performs time domain simulations to analyze the signal content at different nodes.

3.3.1   Integrated Module Schematic

ADS software has the capability to create instance of a design and reuse those instances in other schematics. The same methodology is applied in this case and the design schematics of the individual modules are converted to instances and reused in the final integrated module. The following figure shows the integrated design;
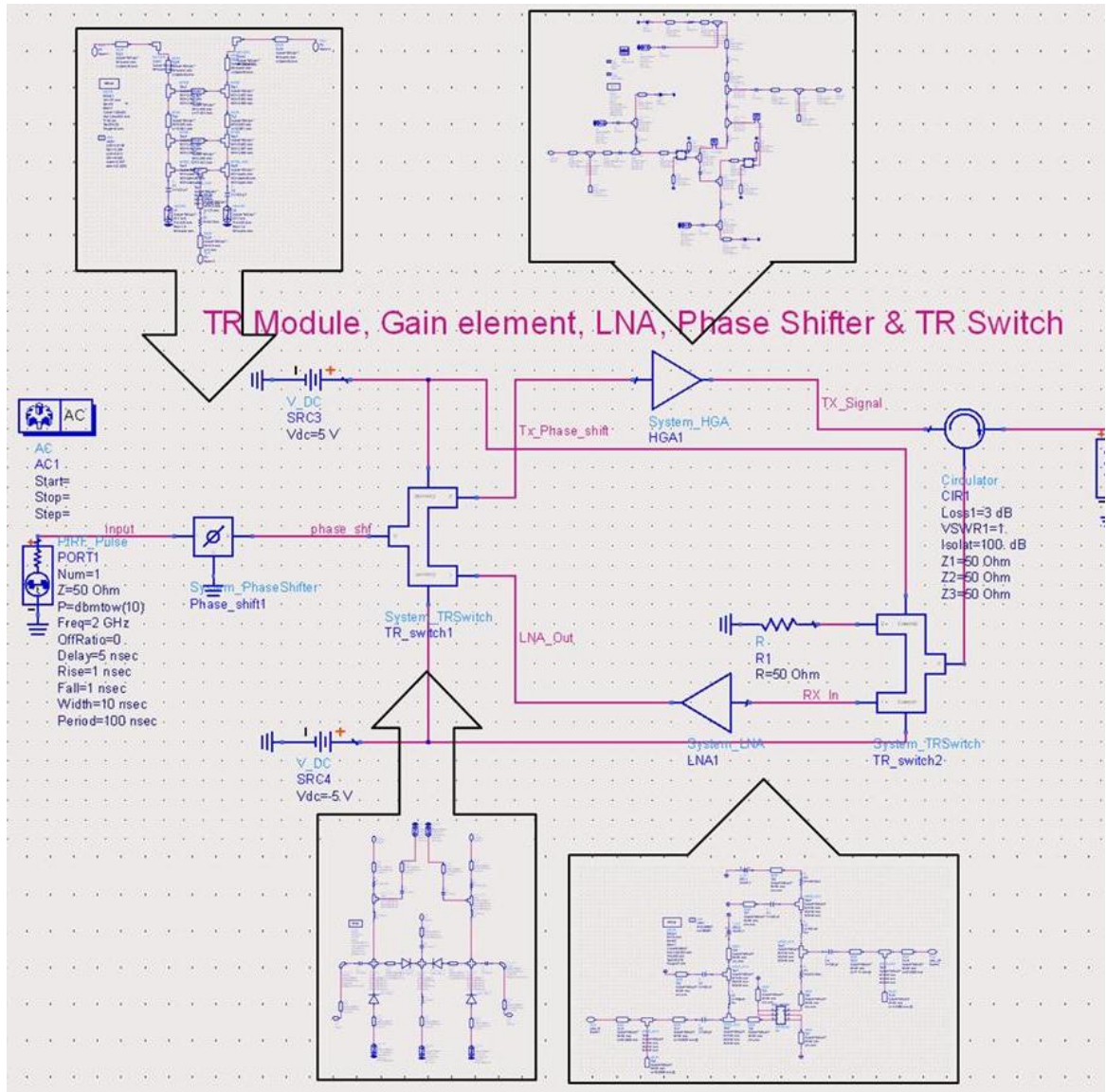
Figure 52: Integrated TR module with sub-module captions

In this schematic, the main modules shown are High gain amplifier (top right), Low noise amplifier (bottom right), Phase shifter (top left) and TR switch (bottom left). On the receive mode, the TR switch is integrated in a receive circuitry mode.

The following sections show the simulation results excited by an AC source at 2 GHz.

3.3.2 Simulation results

The signal applied at the input of the TR module is a 2 GHz RF sinusoidal. The signal fed at the input of phase shifter undergoes a desired phase shift to steer the beam. In the Figure 53 the varactors of the phase shifter are tuned to provide a phase shift of 140^0.
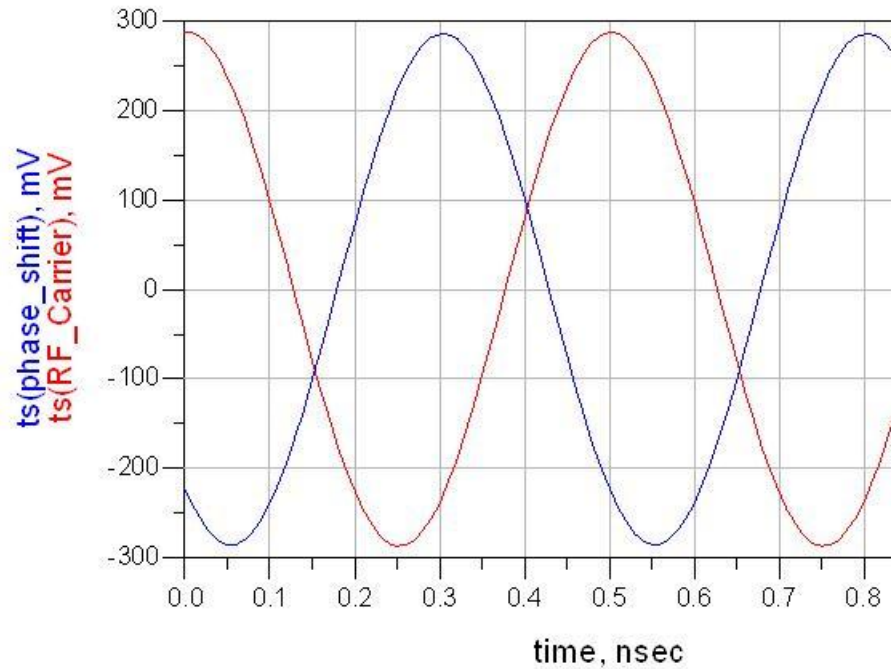
Figure 53: Input and Phase shifterd signal of an Integrated TR module

The phase shifter output is applied at the input of TR switch and the then the input of high gain block. The amplified signal is then transmitted to the antenna for radiation into the air. It is important to observe that there is a phase lag between the input and amplified signal. This phase lag is accounted to the propagation of signal through the microwave circuit i.e. the high gain block. This change in phase is the inherent property of microwave circuits and it does not cause any deformation in the steered pattern as all the amplification modules have same value of this phase lag, hence the relative phase shift between the modules remains unchanged.
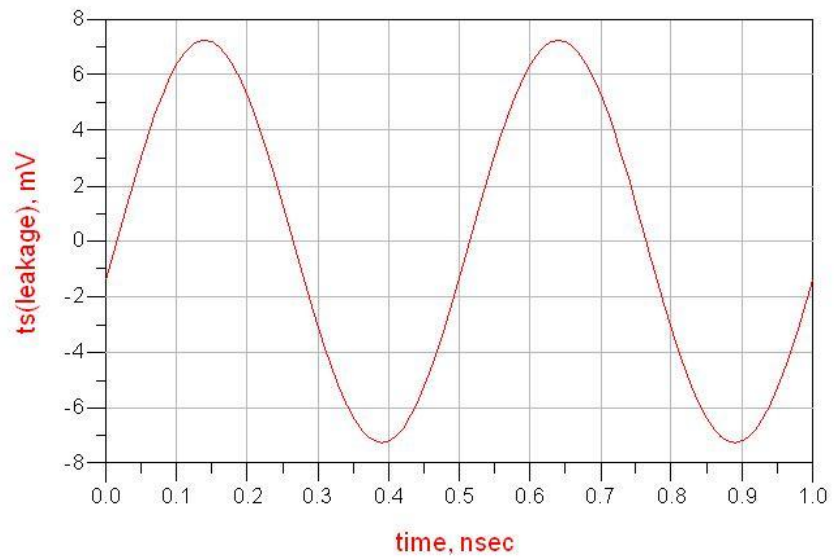
Figure 54: Leakage signal at the limiter termination
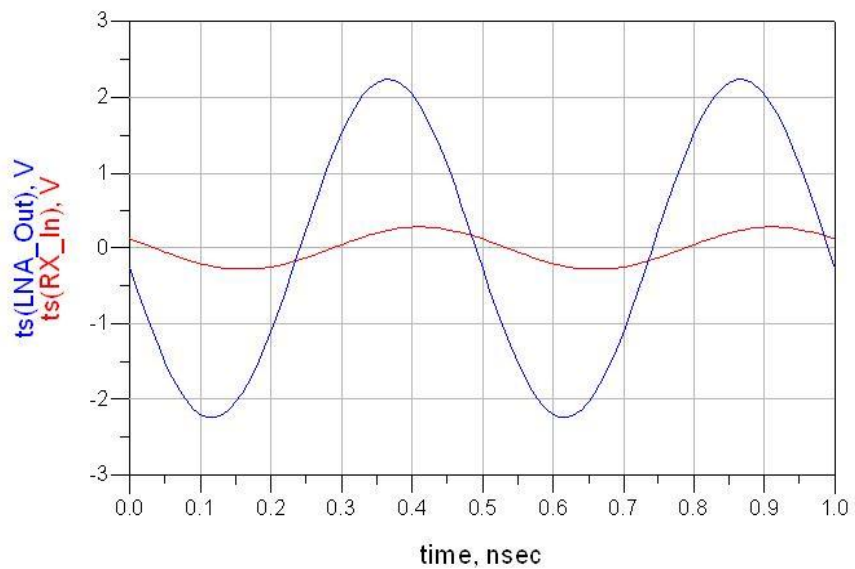
Figure 55: LNA input and output signal

The signal at the limiter circuitry employed to terminate the leakage circulator power is displayed in Figure 54. The peak value of the signal is 7 mV whereas the peak value of the transmitted signal is 2.5 V.

Similarly the signal an the input and of the low noise is displayed in Figure 55

To have a close overview of system response in time domain, Figure 53 to Figure 55, presented a system response focused at a single frequency of 2 GHz i.e. the TR module excited at a single frequency by performing AC analysis. However when the module is excited with an RF pulse source, the signal representation at different nodes closely match to that of the transient analysis performed with the ideal software blocks. This close agreement validates the overall design of the system in terms of its performance, impedance matching, gain response etc. The Figure 56 to Figure 58 present the results at different nodes of the receive chain of the module.
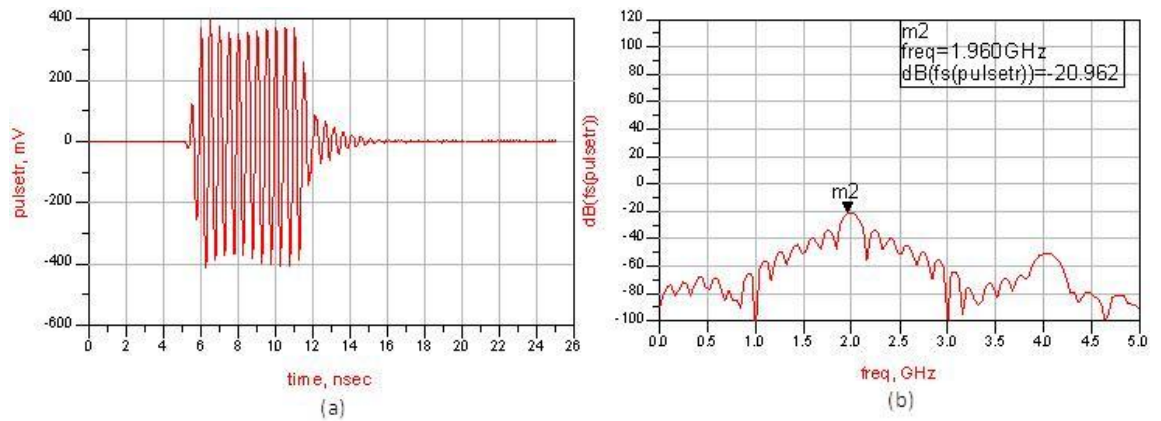
Figure 56: Input signal at the receive chain (a) time domain, (b) frequency domain
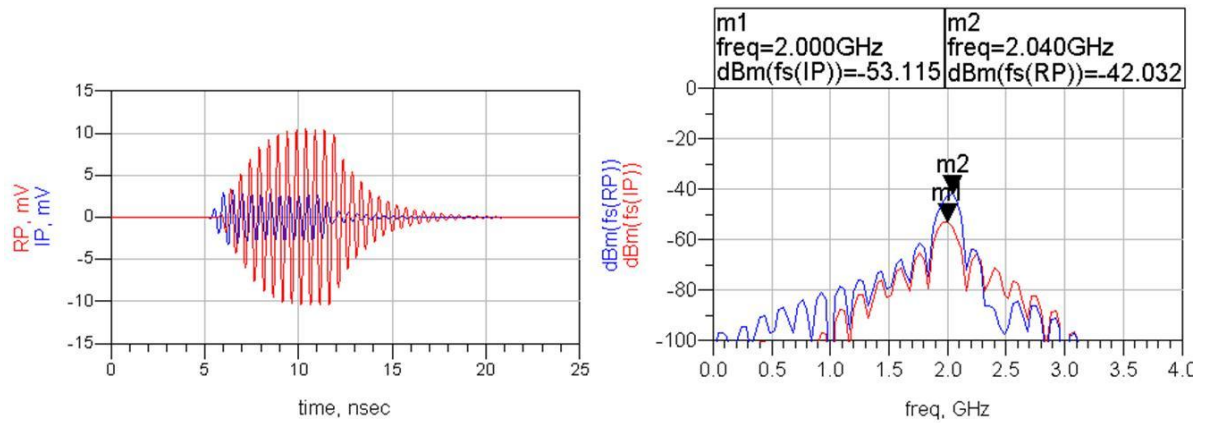
Figure 57: Signal at the input and output of LNA (a) time domain, (b) frequency domain
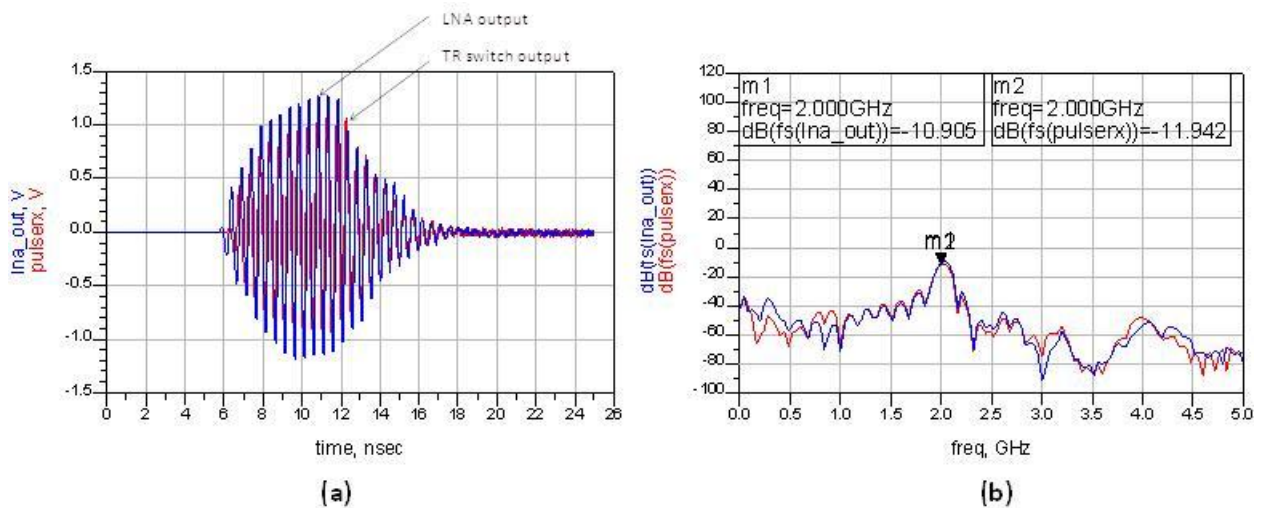
Figure 58: Signal at the input and output of TR Switch (a) time domain, (b) frequency domain

The main highlight of the designed system simulations is the dispersion on the pulse not observed in ideal case. This dispersion can be credited to the different group delay offered to different frequencies comprising the RF pulse applied at the input of LNA or for the matter of any other microstrip or waveguide. Another important observation lies in Figure 59in which there is an amplitude reduction of 1 dB in the output of the TR switch which is validated by the spectral representation in Figure 59(b). This loss is attributed to the insertion loss of the switch; similarly the signal will undergo some when passed through phase shifter.

The final signal output at the phase shifter is routed forward to the signal processing unit to extract the target information. Such an analysis is beyond the scope of this work.

3.4 Summary

This chapter presented a detailed design methodology of the transceiver sub-modules design and simulation. The simulations presents a close approximation with respect to the parameters based on which the modules are designed. However the limitations from the designed modules come from the fact that the design requirements were limited to very few criterion e.g. input and output matching, maximizing gains, minimizing insertion losses etc. Other design criterion like bandwidth, distortion reduction, gain flatness etc. could have included in the design requirements but that would have made the design process resulting in a design focused on single module.

Apart from these limitations, the integrated transceiver module yields acceptable results at the designed frequency. The amplification blocks, the TR switch and the phase shifter in the integrated module generate similar simulation results as generated in individual simulations.

Chapter 4: Design and Development of 5-Bit Digital Phase Shifter: *A sub-module of TRM*

Towards the development of a complete TR Module a further step has been taken: A 5-bit digital phase shifter has been designed, final lay out is ready for prototyping. BOM has been generated.

Analog phase shifter designed in Chapter 3, Section 2.1 offers the advantages of small size, low insertion loss and good input and output match. However such a design module suffers from certain limitations which are as under;

- The phase steering phenomenon is dependent on the values of the two varactor diodes. The close matching between the diode values is essential as any difference in capacitance yields degradations in steering values. In other words the varactor diodes must be closely synchronized to each other.

- The resolution non-linearly depends on capacitance i.e. the change in phase values is more at larger capacitance values than at larger capacitance values. Hence the module requires voltage control calibrated with those of varactor diodes.

This chapter presents the design and simulations of 5 bit digital phase shifter. The design process provides all the details of components involved for the end product.

4.1 Microstrip Couplers and Phase Shifters

The design methodology for the hybrid coupler has been presented in Chapter 3. This section provides an overview of how a 3-dB hybrid coupler/ branch line coupler changes the phase of a signal.

Generic block diagram of a directional coupler often cited in text is shown in Figure 32
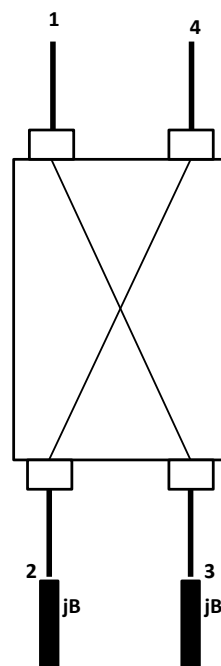
Figure 59: Reactive loading of Hybrid Coupler

As per the pin configuration shown in Figure 32, if pin # 1 is applied with input signal, port # 3 is the coupled port and port # 4 is the isolated port. Such couplers are known as the forward couplers. Other types of couplers are known as backward couplers have port # 3as the isolated and port #4 the coupled. In case of forward couplers and under the perfect matched condition i.e. all the ports are terminated with 50 ohm loads, the input signal is equally split between the through port (port#2) and the coupled port (port#3). However when port#2 and port#3 is matched with ideal and equal reactive loads, all the incident power gets reflected to the isolated port..

As depicted in Figure 59, let the susceptance of the loads be jB, the reflection coefficient of the at each of the port#2 and port#3 is

$$\Gamma = \frac{Y_0 - jB}{Y_0 + jB} \qquad\qquad \textbf{40}$$

The angle contributed by this reflection coefficient is represented as;

$$\phi = \tan^{-1}\left| \frac{-2B/Y_0}{(1 - (B/Y_0))} \right| \qquad\qquad \textbf{41}$$

Consider an input signal $\sin(\alpha\Theta)$ is applied at the input of a hybrid coupler; this signal reaches the port#2 with a phase difference of 90^0 and port#3 with a phase difference of 180^0. The reflected signal at port#2 and port#3 respectively becomes;

$$\text{Reflected Signal at Port\#2: } \sin(\Theta\alpha + 90^0 + \phi) \qquad\qquad \textbf{42}$$

$$\text{Reflected Signal at Port\#3: } \sin(\Theta\alpha + 180^0 + \phi)$$

The reflected signal from port#2 can go to any of the port#1 or port#4. At port#1 and port#4 the signal has phase characteristics of;

$$\text{At port \# 1: } \sin(\Theta\alpha + 90^0 + \phi + 90)(a) \qquad\qquad \textbf{43}$$

$$\text{At port \# 4: } \sin(\Theta\alpha + 90^0 + \phi + 180) \qquad (b)$$

Similarly the reflected signal from port#3 can go to any of the port#1 or port#4. The signal has phase characteristics of;

$$\text{At port \# 1: } \sin(\Theta\alpha + 180^0 + \phi + 180)(a) \qquad\qquad \textbf{44}$$

$$\text{At port \# 4: } \sin(\alpha + 180^0 + \phi + 90) \ (b)$$

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Adding **43**(a) and **44**(a), the contribution due to the reflected signals at port#1 becomes;

$$\sin(\Theta\alpha + 180^0 + \phi + 180) + \sin(\Theta\alpha + 90^0 + \phi + 90) = 0 \quad \mathbf{45}$$

Similarly the addition of **43**(b) and **44**(b), defines the overall signal at port#4.

$$\sin(\Theta\alpha + 90^0 + \phi + 180) + \sin(\Theta\alpha + 180^0 + \phi + 90) \quad \mathbf{46}$$
$$= 2 * \sin(\Theta\alpha + \phi + 270)$$

Hence, at the input port#1 the reflected signal cancels out each other and no power is returned back to the input. However the output signal at port#4 adds in phase. The phase of this signal includes the inherent phase shift added by the coupler along with the phase change contributed by the susceptance. In an array, the inherent phase shift added by each phase shifter remains the same for all the devices and the actual contribution takes place due to the incremental phase shift added by each one. PIN diodes are used to include or exclude desired susceptance in the network.

The next section present only the simulation results of FR-4 based 3-hybrid coupler/branch line coupler as the design methodology has been presented in the previous chapter. The design frequency for the coupler is 2 GHz.

4.2   3-dB Hybrid and Simulation Results

The 3-dB coupler simulations are performed in ADS with the simulation parameters are same as those of mentioned in Table 2. The schematic resembles the coupler in Figure 33hence it is not mentioned here.
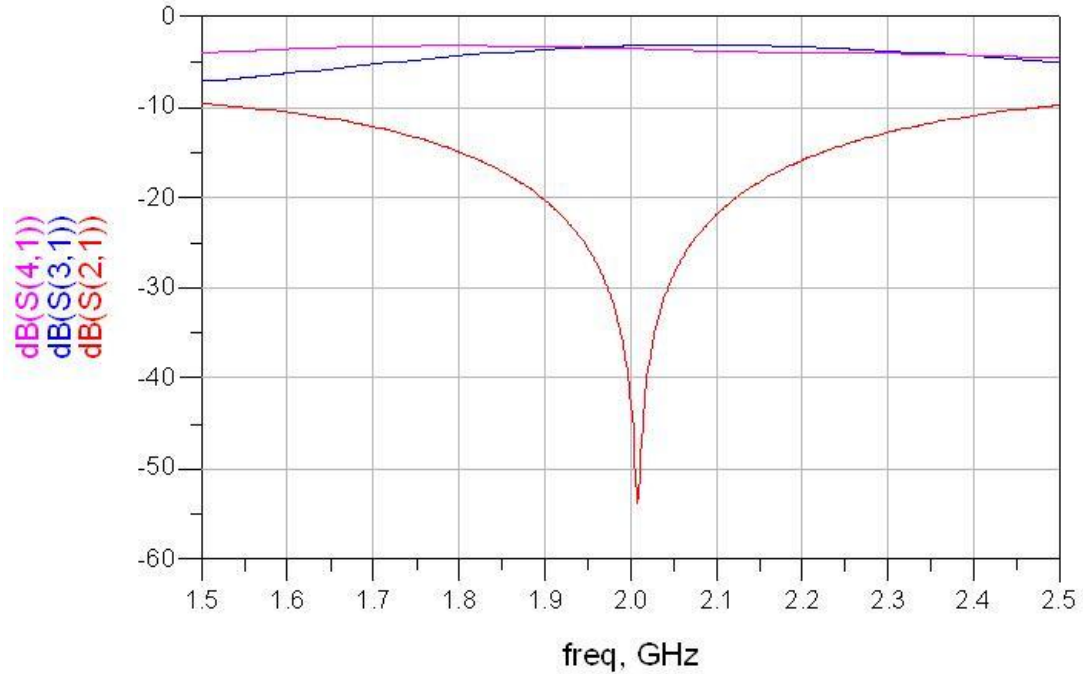
Figure 60: Simulation results of 3-dB Hybrid Coupler

The isolation of the coupler is less than -40 dB whereas the coupling between the two ports is approximately -3 dB. The following section describes the design of a 5 bit digital phase shifter using branch line couplers.

4.3 *5*-Bit Digital Phase shifter

5-Bit digital phase shifter provides phase shifting from 0^0 to 360^0 in steps of 11.25^0 ($360/2^5$). Basically it consists of 5 individual phase shifting networks with phase changing capability of 11.25^0, 22.5^0, 45^0, 90^0 and 180^0. Each of the phase steering stage comprise of a quadrature coupler and appropriate susceptance except for the 11.25^0 stage which is designed on simple topology of loaded lines for its low phase steering as the loaded line topology is suitable only for low steering angles[26]. Figure 61shows the schematic of single stage (45^0 phase contribution) of the phase shifter. All the phase bits are replicas of this module with appropriate variations in load dimensions.

85
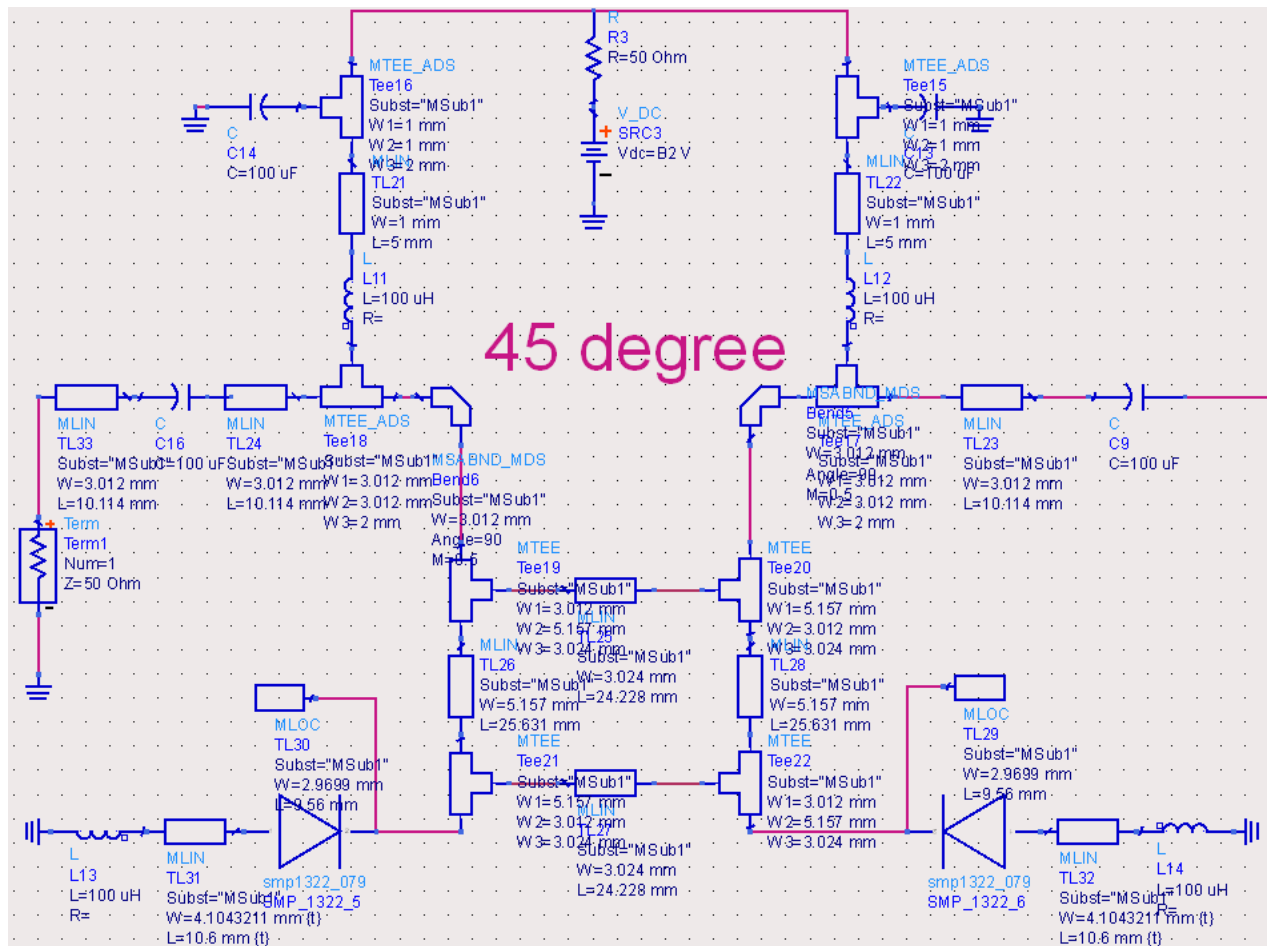
Figure 61: 5-Bit digital phase shifter

The susceptance values of each of the stage are calculated based upon the incremental

phase difference between the two elements.
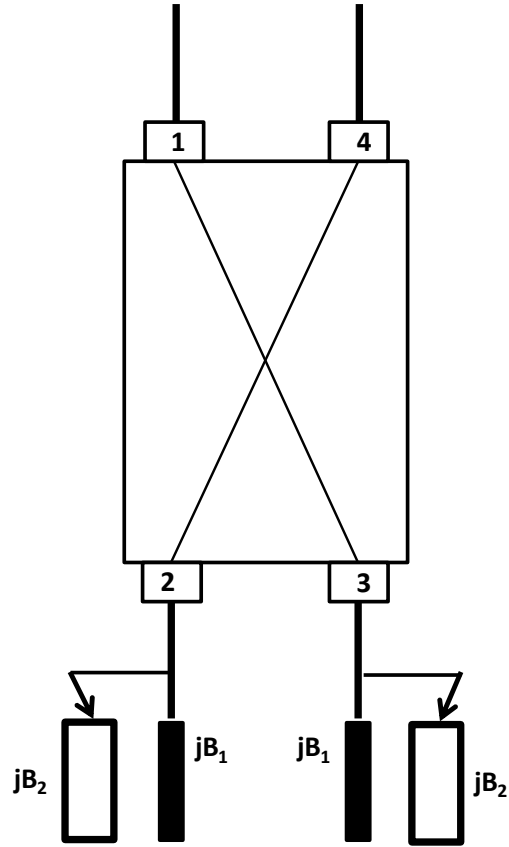
Figure 62: Single stage of a 5-Bit gidital phase shifter

The block diagram of the single stage of a phase shifter is shown in Figure 62. The phase increment is provided by switching between the fixed the fixed load B_1 and the parallel combination of the two loads B_1 and B_2. A diode is used to switch load B_2 in and out of the circuit.

The incremental phase shift provided by the device is represented by the following equation[30, 31];

$$\Delta\phi = 2\left[\tan^{-1}\left(Z_{L_{max}}/Z_0\right) - \tan^{-1}\left(Z_{L_{min}}/Z_0\right)\right]$$

47

The reflection type phase shifters can achieve phase shifts of the order of 360^0[31]. From the equation, it is evident that if the loading impedances are varied from $+\infty$ to **-**

∞, the phase shifting from $+180^0$ to -180^0 can be achieved yielding an effective incremental phase shift of 360^0.
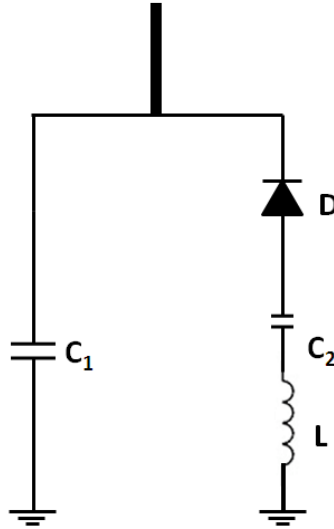
Figure 63: Lumped element load model

The lumped components representation of the loads is shown in Figure 63. Which shown that the reference impedance is provided by the capacitor C_1. When the diode is turned ON, an LC resonant circuit offers the desired loading and hence the desired incremental phase shift.

In the following analysis the diode is assumed to be an ideal device which introduces certain tolerances in the calculated values. Such tolerances are catered for in simulations by tuning the values close to desired results.

Under the OFF state of the diode, the impedance /reactance of the capacitor as seen by the coupler port is represented as;

$$Z_{L_{OFF}} = {-j}/{\omega\,C_1} \qquad\qquad \textbf{48}$$

When the diode is turned ON, the LC parallel circuit is defined to have the following impedance;

$$Z_{L_{ON}} = \left.j(\omega^2 L C_2 - 1)\middle/[\omega(C_1 + C_2 - \omega^2 L C_1 C_2)]\right.$$

<div align="right">49</div>

Z_{LON} is a complex relationship and [32] specify that if the two impedance states are conjugate of each other, the bandwidth of the system is optimized e.g. if the desired phase shift is 90^0, the two phase states should yield +45 and -45.

Based upon the above mathematical treatment, the phase shifter is designed and simulated. The following section presents the simulation results and fabrication schematic of the final module.

4.3.1 Simulation Results

The phase shifter is simulated over a frequency spectrum of 1.7GHz to 2.3GHz.

Figure 64present the insertion loss of the complete module. The insertion loss varies between 3dB to 4dB, which if achieved in measured results, matches with some of the commercially available products in the same frequency band e.g. a six bit digital phase shifter has insertion loss of 3.5dB [33] where as another product 7 bit phase shifter has an insertion loss of 5.5dB [34]. The insertion loss of the 180^0 bit is slightly more than the other ones but this can be attributed to the large size of the reflective loads used to achieve the desired shift.

Figure 65present the input return loss (impedance matching) values which are less than 15 dB over a bandwidth of 250MHz. [34] also report these values to be around 16dB.

Figure 66present the phase variations of the device. For a minimum resolution of 11.25^0, the device offers linear phase for more than 200MHz of the spectrum centered at 2.0 GHz.
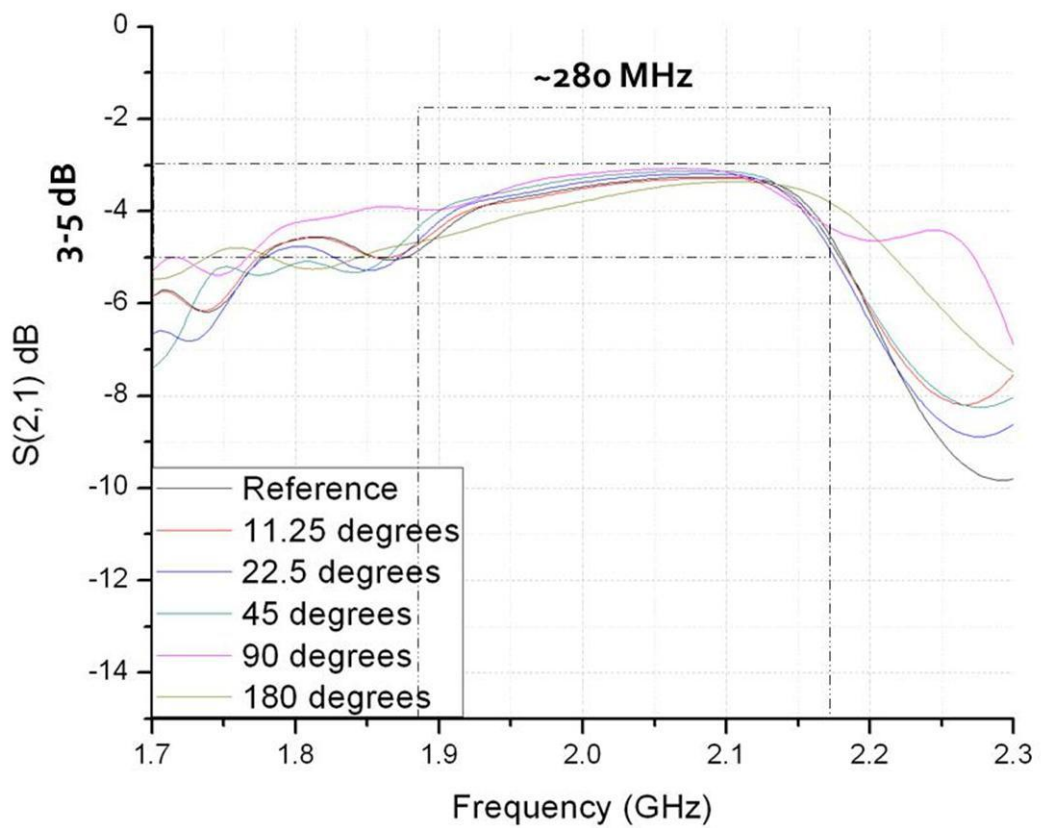
Figure 64: Insertion loss of the Phase Shifter
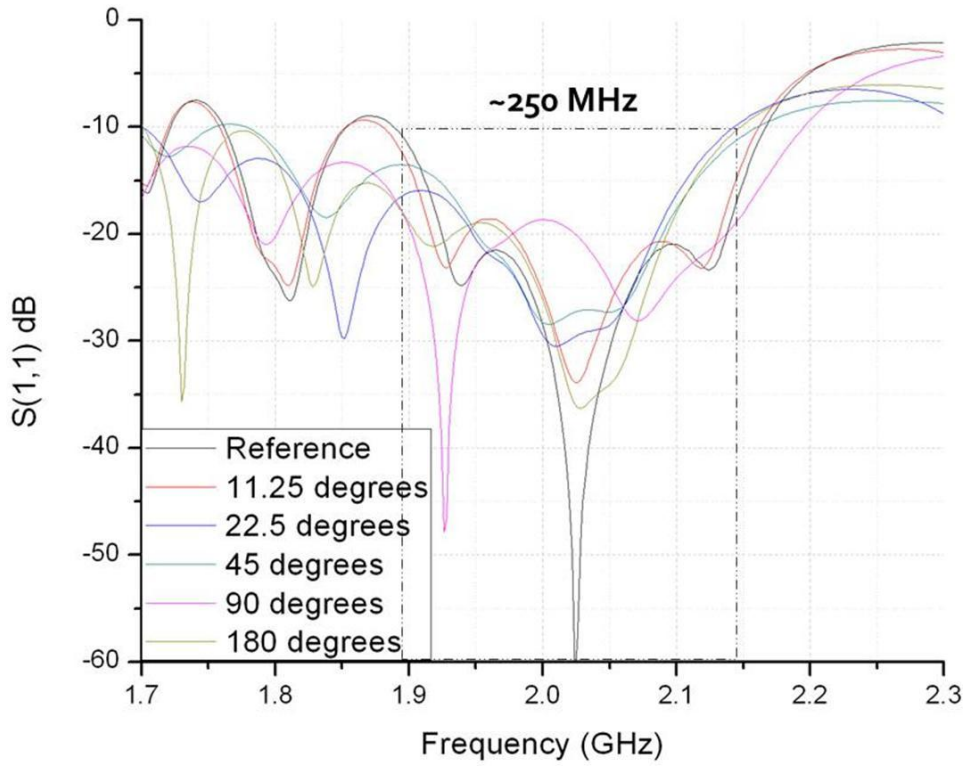
Figure 65: Return loss of the phase shifter at Port # 1
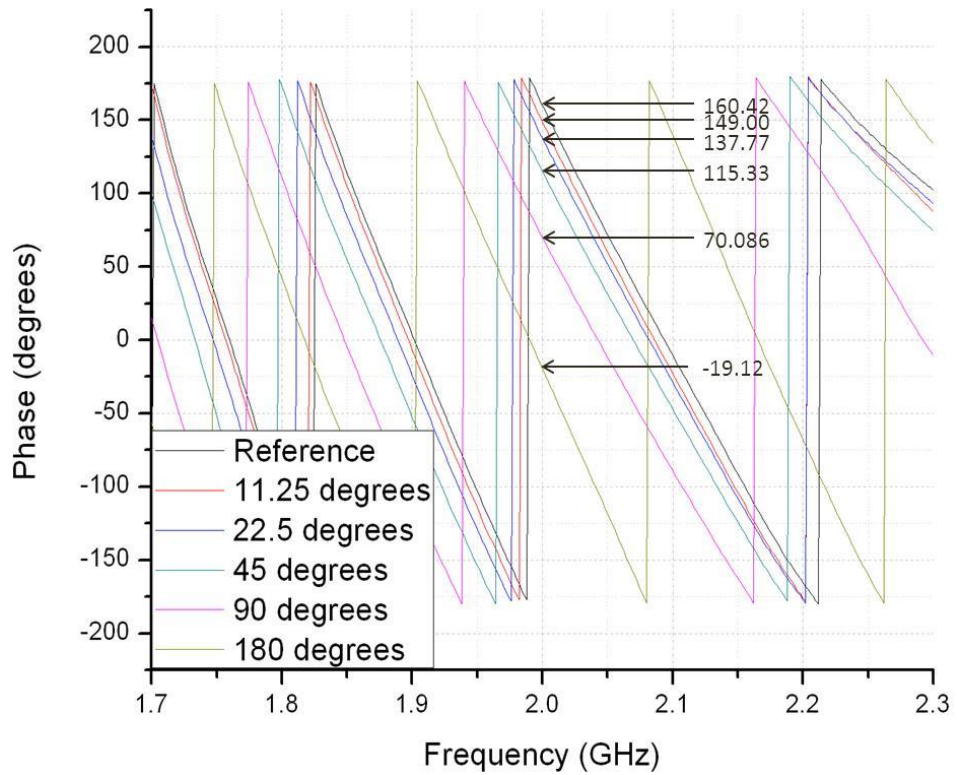
Figure 66: Phase changes of the Phase Shifter

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4.4 Summary

The chapter presented the design methodology of the digital phase shifter and presented the simulation results which agree well expected design. Although beyond the scope of this work, the simulation model is to be fabricated in order to realize the phase shifter and analyze the design through measured results. In this regard Figure 67represents the fabrication layout of the phase shifter.

Output line

Control Bits

Input line

180.00^0

90.00^0

11.25^0

22.50^0

45.00^0
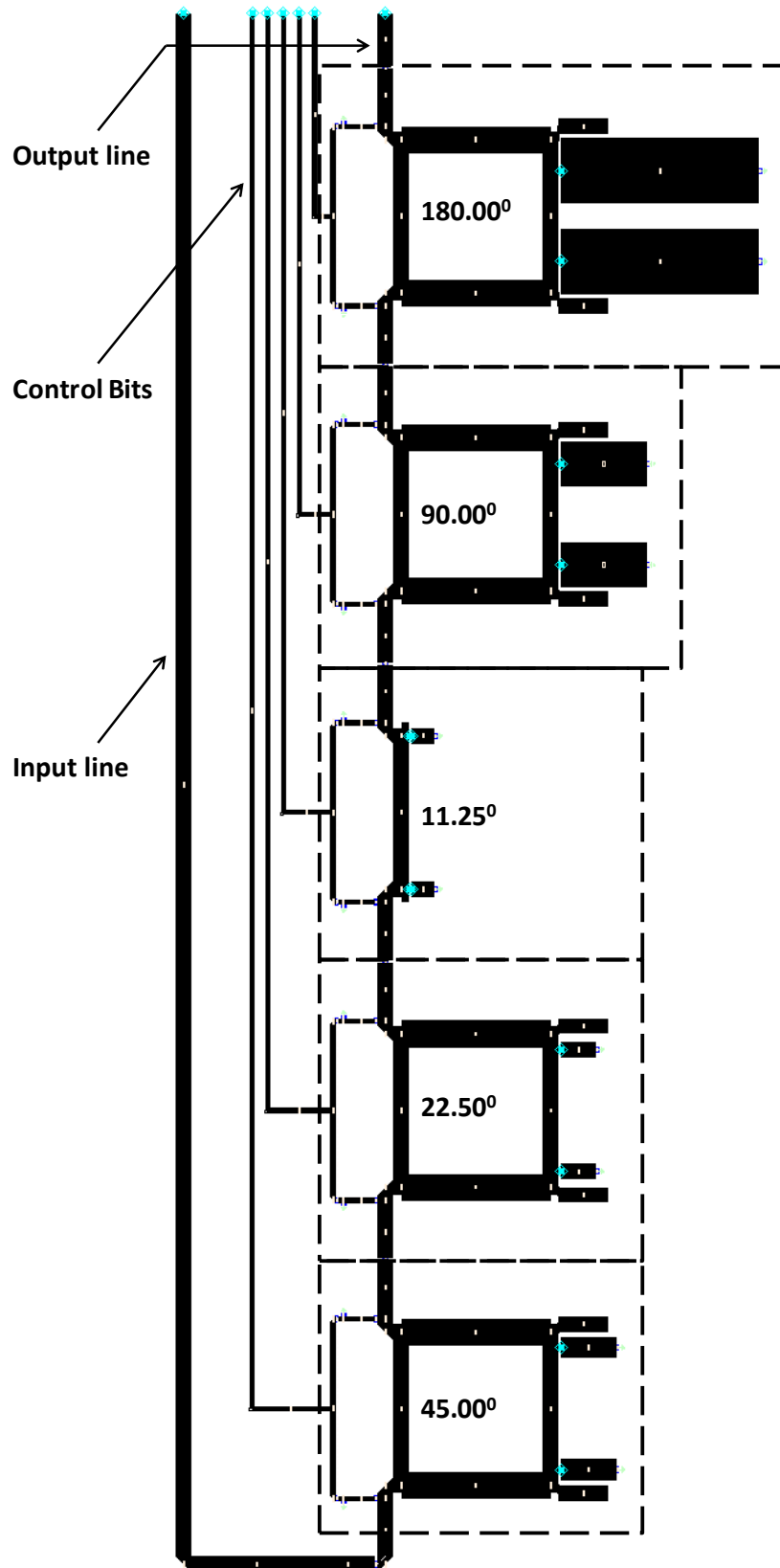
Figure 67: Fabrication layout of the Phase Shifter

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Chapter 5:Conclusions & Future Work

At MS thesis level, the work is aimed at a bigger project of active microwave sensors and has presented a complete design methodology of a TR Module in a single document including mathematical and behavioral modeling and detailed designing of each sub-module of a TRM. The integrated TRM simulation results follow the trend as per the mathematical expressions presented in Chapter 2. As an extension of this work, cost effective prototype development of TRM sub-modules in the lab environment has been initiated and a path towards development of active microwave sensors indigenously has been paved.

Summarizing the content, the first four chapters of this dissertation presented a sequential approach related to the design of transceiver module for active microwave sensors. Starting from the first chapter, where the phase array radars and its constituents have been presented at an introductory level, the next three chapters built upon a step wise approach in realizing the simulations of the complete TR module. The analytical study of the transceiver module presented a different perspective of the TR module which has never been presented before. The design and simulation results of different microwave devices presented single point information related to the basics, types, design parameters and methodology of each of the sub-modules e.g. phase shifter, TR switch, low noise amplifier, high gain block etc. Finally section on the integration of the modules presented collective simulation results of the individual schematics catering for the mismatches between them. Chapter 4 highlighted some of

the shortcomings of the analog phase shifters and presented some the analytical expressions and design methodology for the design of digital module. The simulation results if achieved in fabricated modules will fall in close approximation to some of the commercially available products.

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Appendix

Publications

- **A. A. Qureshi**, M. U. Afzal,T. Tauqeer,M. A. Tarar, "**Signal Analysis, Design Methodology, and Modular Development of a TR Module**", *Proceedings of the IEEE International Conference on Emerging Technologies 2011 (accepted)*, pp. 1-4, Sep, 2011, NUST-SEECS, Islamabad Pakistan

- **A. A. Qureshi**, M. U. Afzal,T. Tauqeer,M. A. Tarar, "**Performance analysis of FR-4 substrate for high frequency microstrip antennas**," in *Microwave Conference Proceedings (CJMW), 2011 China-Japan Joint*, 2011, pp. 1-4.

- M. U. Afzal, **A. A. Qureshi**,M. A. Tarar,T. Tauqeer, "**Analysis, Design, and Simulation of Phased Array Radar Front-end**", *Proceedings of the IEEE International Conference on Emerging Technologies 2011 (accepted)*, pp. 4-8, Sep, 2011, NUST-SEECS, Islamabad Pakistan

- M. U. Afzal, **A. A. Qureshi**, M. A. Tarar, T. Tauqeer, "**Modeling and simulation of an X-band planar phased array antenna**," in *Microwave Conference Proceedings (CJMW), 2011 China-Japan Joint*, 2011, pp. 1-4.