A FULLY INTEGRATED CMOS POWER AMPLIFIER FOR WLAN AND BLUETOOTH APPLICATIONS

By

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ABSTRACT

In today's wireless communication systems one of the most important parts of transceiver system is the Power amplifier. A good power amplifier is one which can maintain its linearity and provide good efficiency over the change of input power. Different techniques have been used to achieve linearity and efficiency whilst keeping the size of amplifier as low as possible.

In this thesis the design consideration of such a power amplifier is considered for the frequency of WIFI and Bluetooth to provide output power of 16 dB for single stage with 40% Power added efficiency (PAE) and 30 dB for two-stage power amplifier. The techniques which are used to achieve the desired objectives are optimum impedance matching and harmonic suppressions circuits using both the transmission lines and lumped components. Here the harmonic suppression circuit helps to ground the harmonics which overall enhances the efficiency of Power amplifier up to 7% and provides linearity over the gain.

Simulation results show that the power amplifier delivers 17.5 dB gain for single stage with 52% maximum Power added efficiency and 36 dB gain for two-stage power amplifier. The value of Stability factor should be above 1 in order to prevent the amplifier from oscillating. In this Power amplifier the stability factor was measured to be 1.17 and it remains above 1 for the whole bandwidth of WIFI and Bluetooth.

The CMOS design of the proposed Power Amplifier is also presented. The CMOS IC consists of 5 pins where Pin 1 and 2 are RF input and output respectively, Pin 3 is V_{CC} whereas Pin 4 and 5 are Ground pins. Two coupling capacitors C1 and C2 are connected at the input and output ports and a resistor R1 is placed at the V_{CC} pin.

The measured results show that the Power amplifier delivers output gain of 16.7 dB in case of single stage amplifier and 30.5 dB in case of two stage Power amplifier

DEDICATION

Dedicated to my parents, especially to my mother, and my dear ones for their continuing support and encouragement throughout my Master's course work and research

ACKNOWLEDGEMENT

First of all I would like to say thank you to my supervisor Associate Professor Dr. Farooq Ahmad Bhatti who helped me and assisted me during my research work. His kindness and encouragements had always been a morale booster whenever I had problems during my research phase. I am impressed by his humble and kind nature. Besides, I would also like to say thank you to my thesis committee members respected Col. Dr. Imran Rashid, Lt Col. Dr. Adil masood siddique and Dr. Mir Yasir Umair.

I can never forget the efforts of my parents which brought up to this stage of my life and without their prayers and support I could never be so much successful in my life.

And above all, Thanks to Allah Almighty for everything.

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Chapter 1

INTRODUCTION

1.1 Brief Description

Radio frequency power amplifier is an amplifier that turns a low power signal to a high power signal. Usually the power amplifier is connected just after the transmitting antenna. The important parameters of any power amplifier are output power, Gain, frequency bandwidth, power added efficiency, Linearity, input-output matching circuits and heat dissipation.

There are different classes of amplifiers depending upon design goals. These classes are Class-A, Class-B, Class-AB, Class-C, Class-D, Class-E, Class-F and Class-G. Each of these classes has their own use in different fields of amplifier designing.

Back in 1900's there were no transistors and only vacuum tubes were used for amplification purpose. In 1947, after the invention of transistor by John Bardeen, Walter Brattain, and William Shockley soon the electronic circuits began to get deduced in size and improved efficiency. These transistors can be BJT (bipolar junction transistor), FET (Field effect transistor) or MOSFETs (Metal oxide semiconductor Field effect transistor). Even after the invention of transistors, the vacuum tubes are still being used for high power transmitters.

1.2 Research Work Already Undertaken

A lot of work has been done on Power amplifiers where different parameters are taken into consideration and any improvement has been brought into it. A Fully integrated 2.4GHz Power amplifier is designed for wireless networks where the cascade topology with inductively degenerated common source is implemented. The design shows improved gain and stability together with linear functionality of transistor over the desired frequency range [1]. Another novel method of designing a dual band Power amplifier is show in [2]. The technique includes the use of resonators with microstrip line at both input and output matching networks. This design works for 1.5GHz and 2.4GHz frequency. Some work has also been done on adaptive biasing technique using a feed forward control circuit. Here the bias current is automatically adjusted according to the input power for enhancing its efficiency [3]. Another research is done on a two stage power amplifier for 2.4GHz frequency

where a cascade topology is implemented. This topology includes a driver stage and a power stage for gain enhancement [4].

1.3 Relevance to National Needs

In wireless communication the power amplifiers play a very important role of increasing the strength of a signal so that it may travel to a longer distance. Without the power amplifiers, the distant users will not be able to receive signals and hence the communication will not be possible. Different organizations, whether it is private or government sector, is working on the design and improvements in power amplifiers for different wireless systems. Hence research in the area of power amplifiers will be beneficial to different government and private sector organizations and this will eventually lead to strengthen and nourish the field of telecommunication in our country.

1.4 Motivation behind Research

Power Amplifiers are very useful in almost every wireless device which improves the signal strength of transmitter. Nowadays science and technology is trying to make electronic devices smaller in size and wireless in nature and in order to make such wireless devices transmit their signal to a longer distance, they need an efficient, small sized with high output gain power amplifiers so the power amplifier is one of the best topic to work on and to bring something new and improved version of what is already designed.

1.5 Advantages

The primary advantage of Power amplifiers is that they help to send any signal to a distant location where any user might wants to connect to the network. Since usually the user end device transmits and receives a signal with low power because of its limitations in battery power, so the power amplifiers on any base station has to be powerful enough in order to transmit the signal to longer range. So here at base stations a Power amplifier with high output Gain is required usually with more than 2 stages, while in user end devices the efficiency of Power amplifiers is to be taken care of, so that it may transmit signal while

using the battery power efficiently and designing such Power amplifiers will result in a more efficient wireless communication.

1.6 Literature Survey

1) **Santosh B. Patil and Rajendra D. Kanphade "Design and Analysis of a 2.4 GHz Fully Integrated 1.8V Power Amplifier in TSMC l80nm CMOS RF Process for Wireless Communication" 2015 International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA)**

DESCRIPTION:

In this paper the design of a fully integrated Power amplifier is suggested which will be working on 2.4GHz frequency and 1.8 V_{CC} Supply voltage. The design uses a cascade topology for single stage amplifier which is composed of inductively degenerated with source grounded. This design assures enhanced gain with a stable Power amplifier and also linearity is good enough for a wide range frequency. The input and output matching circuits are designed in optimum fashion so that noise figure would be minimum which will help in providing more gain and efficiency. This design is tested on Cadence EDA Tool where results show its output power to be 14dBm and Power added efficiency to be 37%. The S_{11} and S_{22} are -12.66dB and -9.22dB respectively. Final layout of CMOS Power amplifier is $0.079mm^2$

2) **Changhyun Lee and Changkun Park "2.4 GHz CMOS Power Amplifier with Mode-Locking Structure to Enhance Gain" 2014 Hindawi Publishing Corporation the Scientific World Journal.**

DESCRIPTION:

In this paper the design of a RF CMOS Power amplifier is proposed with mode-locking method. This amplifier uses an optimized cascade structure which helps in efficiency enhancement. In any typical Power amplifier the typical the cross-coupled transistor is changed into the proposed technique of mode-locking which improves matching impedance and increases the output power and efficiency. For testing the design a 2.4GHz CMOS power amplifier is designed using a 0.18um CMOS process. Test results show that total output

power is 23.32dBm while the Power added efficiency comes to be 34.9%. The final Chip size is 1.4mm x 0.6mm.

3) **Xiangning Fan, ChenXu, Jiakai Lu and Zaijun Hua "Design of a 2.4GHz Power Amplifier" 2015 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP).**

DESCRIPTION:

This paper represents a 2.4GHz power amplifier using a 0.18um CMOS RF process. In this paper the main focus is kept on high efficiency and gain. In the fabricated design the effect of inductance at the source is suppressed by using a differential structure. The input and output matching networks are optimized such that to reduce the overall chip size. Providing a DC supply voltage of 1V, an 8dBm output gain and PAE of 19% is seen. S_{11} and S_{22} of this amplifier is -23dB and -9dB respectively. All these test results are taken at an input power of -10dBm.

4) **Shichang Chen and Quan Xue "Highly Efficient Dual-band Power Amplifier Based on Cascaded CMRCs" Proceedings of APMC 2012, Kaohsiung, Taiwan, Dec. 4-7, 2012.**

DESCRIPTION:

This paper presents a power amplifier with dual-band characteristics where a class-F topology configuration is used. The power amplifier is designed for 2.4GHz and 3.5GHz band. A Multi-harmonic control circuit is implemented using two compact microstrip resonant cells in series with an open stub. Using this approach the overall size of the amplifier is greatly reduced as compared to previous designs. Test results show that Power added efficiency of 63% and 71% is obtained with a total power of 40.8dBm and 41.6dBm respectively for the two frequencies.

5) **J. J. Moreno-Rubio, E. F. Angarita-Malaver, L. F. Pérez-Mancera, N. R. Burgos, and W. A. Cuevas-Carrero "Harmonic Tuned RF/Microwave High Efficiency Power Amplifier Design Accessing The Intrinsic Drain" PROCEEDINGS OF THE 2014 IEEE CENTRAL AMERICA AND PANAMA CONVENTION (CONCAPAN XXXIV)**

DESCRIPTION:

In this paper the design of a power amplifier using an FET device is presented using special harmonic tuned technique. The main focus is on how to use the drain's intrinsic characteristic for harmonic tuning. Different equations are presented here for optimized output matching technique which can be implemented in any power amplifier using a harmonic tuning. The implementation of a hybrid amplifiers are done here in order to prove the proposed design. The first is the Tuned load power amplifier while the second is an inverse class F amplifier. The results have shown the improved gain, power and efficiency of the inverse class F amplifier. The efficiency is seen to be 70% while in saturated mode. This design can be implemented using GaNHEMT devices for frequencies ranging between 2GHz-3GHz.

1.7 Objectives

- To design and develop a high gain Power amplifier at 2.4 GHz frequency.
- Gain should be of up to 16 dB for single stage and 27 dB for two stage power amplifiers.
- Power added Efficiency (PAE) of up to 40% would be achieved from such a design.
- Design of CMOS Power amplifier at 2.4 GHz.

1.8 Areas of Application

- Mobile communication
- Wireless routers
- Wifi devices
- Bluetooth devices

1.9 Report Structure

Each chapter covers the following contents:

Chapter 1: Brief description, motivation, advantages, Literature survey and objectives.

Chapter 2: CMOS technology.

Chapter 3: Components of RF Power amplifier and its classes.

Chapter 4: Design techniques of RF Power amplifier which includes impedance matching techniques, Gain and Efficiency enhancement techniques. This chapter also highlights the CMOS design methodology of Power amplifier.

Chapter 5: This chapter will cover the fabrication process of the Power amplifier along with the simulated and measured results of the proposed Power amplifier.

Chapter 6: It will conclude the overall thesis and any future work which can be done on this design.

Chapter 2

CMOS Technology

2.1 Introduction

CMOS device was invented in 1960s, which brought a revolution in the field of microelectronics. Currently, a vast series of nanometer CMOS devices are making wonderful development in faster, efficient and smaller-in-size devices technology.

To know the working of CMOS device is necessary in designing and fabricating digital or analog circuits. In literature, the DC analysis of the CMOS can be found [5], therefore it will not be described in the following topic. While working with analog circuits, small-signal models are usually discussed. At some particular bias point, these models explain the linear function of transistor. The small-signal model given in this chapter is taken from [5]. This model includes intrinsic capacitances, and gives information about the desired extrinsic components.

Though in power amplifiers, the device can intersect the boundaries between different frequency ranges, because the transistors work under large voltage difference.
This chapter will account the basic working of MOS device, and will also discuss the restrictions of different CMOS technologies.

2.2 Device Explanation:

2.2.1 Composition of MOS:

The working of an n-channel MOS, represented as NMOS, will be discussed in the section below. The operation of PMOS (p-channel MOS) is similar to that of NMOS. The basic structure of NMOS is given in Figure 2.1. In the substrate, two heavily n-doped regions are present. These areas are called drain (D) and source (S). An insulating sheet of silicon dioxide (SiO_2) is located between the gate (G) and substrate. The device is placed in p-substrate and is known as bulk or body (B). To maintain the source drain junction diodes reverse biased, the device is usually fixed to the minimum potential in the system.

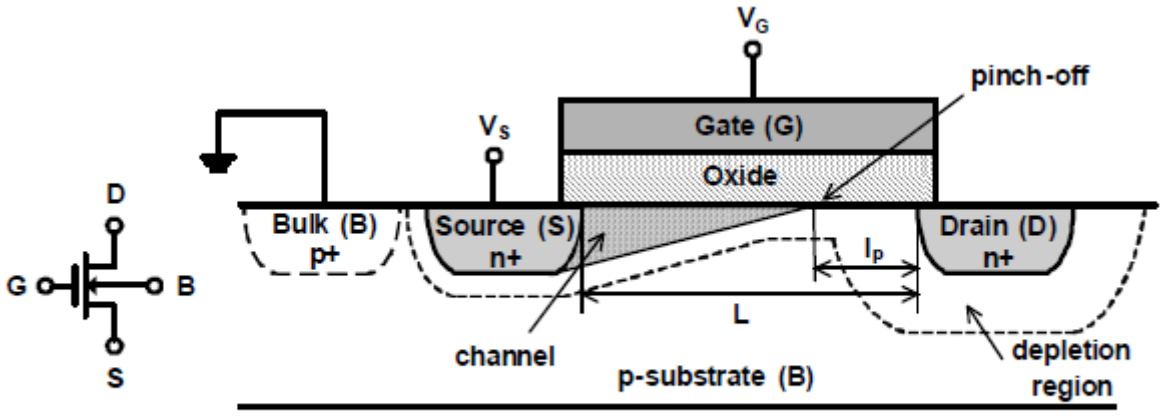


Figure 2.1 Schematic and cross section view of an NMOS transistor

Channel L is situated between the drain and source, and below the gate, whereas the channel between drain and source is present at the four ports under specific biasing situations. The perpendicular expansion of source and drain terminals is represented as width W. Channel and Gate are parted by a thick layer named T_{OX}. Its thickness is usually between 1.0 – 5.0nm.

2.2.2 Small signal input model:

2.2.2.1 Basic Model:

The intrinsic model of a MOS transistor is given in Figure 2.2a. This is a small-signal representation, which is achieved when a small signal difference is supplied at the device terminals. After that, variations in the charges and device current values are obtained. Very minute differences of the bias voltages are directed at the device terminals in steps, one by one, and resultant impacts on drain current are noted down. These small effects can be represented by the equation 2.1. It must be kept in mind that intrinsic modelling neither accounts for the extension of drain and source, nor the capacitance between the gate, source and drain. This is shown in Figure 2.3.

$$i_{ds} \approx g_m v_{gs} + g_{mb} v_{bs} + g_{sd} v_{ds} \tag{2.1}$$

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{BS},V_{DS}}, \qquad g_{mb} = \left.\frac{\partial I_{DS}}{\partial V_{BS}}\right|_{V_{GS},V_{DS}}, \qquad g_{sd} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS},V_{BS}} \tag{2.2}$$

The derivatives are replaced by trans-conductances in equation 2.1. These trans-conductances are shown in equation 2.2. In this equation, g_m shows the gate trans-conductance, which is mostly known as only trans-conductance. g_{sd} and g_{mb} denotes the source-drain conductance and substrate trans-conductance respectively. The working of transistor in different regions is determined by the type of biasing performed for transistor. As a result, the calculations of parameters are dependent on the region in which transistor runs.

Let us consider that the transistor runs in saturation region. In such case, the trans-conductances and source-drain conductance can be found using the equations from 2.3 – 2.5. Figure 2.2a shows a small-signal model, which is obtained by combining the intrinsic capacitances of the device and resultant trans-conductances. Here, the output conductance is swapped by a resistor [5]. Though, it can be deduced that the substrate conductance g_{mb} only appears when there is some potential difference between the source and the substrate.

$$g_m \approx \frac{2I_{DS}}{V_{GS} - V_{th}} \approx \sqrt{\frac{2\mu C_{ox} W I_{DS}}{L}} \tag{2.3}$$

$$g_{sd} \approx \frac{\mu C_{ox} W}{2L}(V_{GS} - V_{th})^2 \lambda \approx \lambda I_{DS} \tag{2.4}$$

$$g_{mb} \approx \frac{g_m \gamma}{2\sqrt{\varphi_0 + V_{SB}}} \tag{2.5}$$

The output conductance decreases with an increase in the voltage difference between drain and source V_{DS} [5]. But if we increase the value of V_{DS} beyond, the depletion region that is linked with drain will increase more into the substrate, which will have a direct influence on the depletion region of source. To avoid this issue, the value of V_{DS} is decreased, that gives the lower threshold voltage. This behavior is known as drain induced barrier lowering DIBL [6]. It neutralizes the effect on the output impedance, because of channel-length modulation.

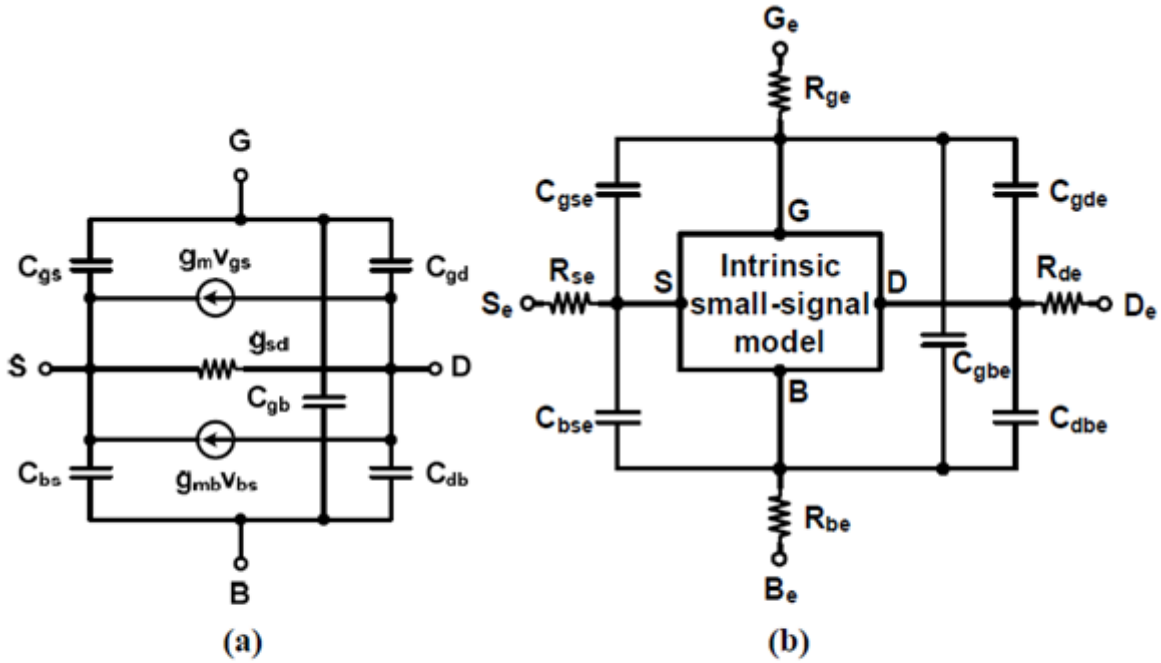


Figure 2.2 (a) Intrinsic small-signal model of MOS transistor [1]
(b) Small-signal model with extrinsic elements added

These facts and events are essential while designing analog circuits because the output conductance and intrinsic gain of the transistor are directly related. This phenomenon has an influence on the output impedance of the device because in a standard power amplifier, the voltage fluctuations are pretty large. Similarly, these prospects are also practical for the intrinsic capacitors of the device, and they must be remembered in transistor model to acquire better outputs.

2.2.2.2 Extrinsic Components

The extrinsic capacitances are inserted in parallel to the intrinsic small-signal model. This is shown in Figure 2.2b. These capacitances are present among all the terminals, such as fringing capacitance C_{fringe}, overlay capacitance C_{ov}, capacitance associated with the extension of source and drain, denoted by C_{bottom} and sidewall capacitances $C_{sidewall}$. These are represented in Figure 2.3. The value of capacitance between drain and source is quite small, so it can be ignored.

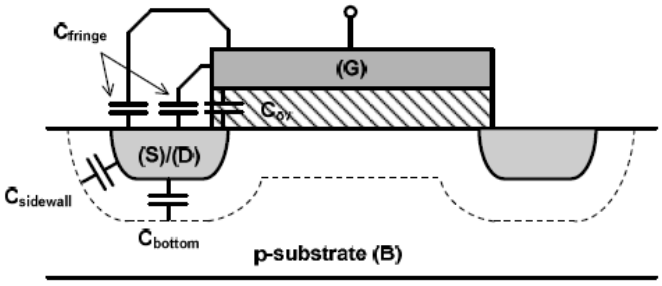


Figure 2.3 Extrinsic capacitances in the MOS transistor

2.2.3 Simulation for Electromagnetic parasite:

Apart from transistor model, there are some parasitic and parameters, which are not linked directly to the MOS device. For example, when a transistor is employed for a power amplifier, then the value of current passing through the device can go up to hundreds of mill amperes or even it can appear in amperes. As a result, the MOS device, along with the links and network surrounding the transistor has to endure the large values of currents. At the drain and source junction, many metal layers are piled on one other in order to solve the current density restrictions of the metal traces. As a result, electron migration will decrease [7]. The resistive voltage drop will also reduce around the inter-links and there will be more capacitive coupling among the drain, gate and source. This is given in Figure 2.4a. As we know that in transistor model, all metallic layers are not counted in. Therefore, extra capacitances and some other dielectric losses should be added to the present model of the device. Layouts parasitic are usually characterized by either pi or tee equivalent circuit designs [5].

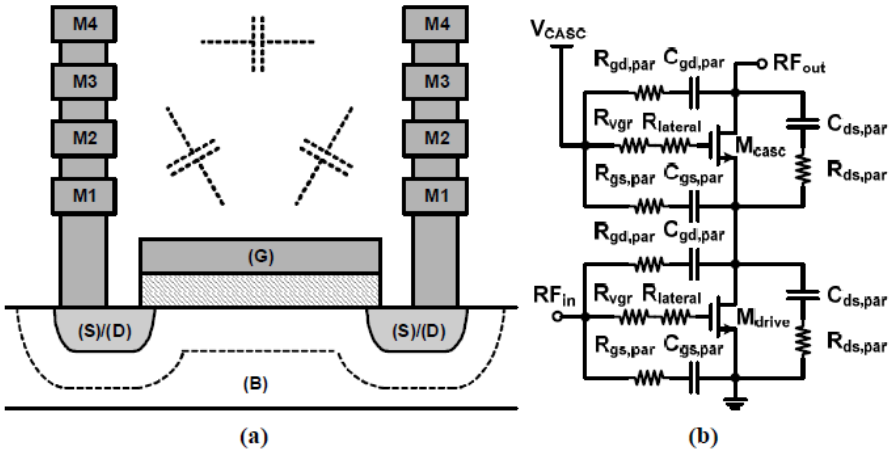


Figure 2.4 (a) Parasitic capacitances between gate, drain and source

(b) Model of cascode stage with parasitic including the vertical gate resistance

From some reference papers [5] and [6], we observe a cascade amplifier stage. This is given in Figure 2.4b. Its related layout parasitic is shown in Figure 2.4a. The parasitic connections were estimated with serial connections of resistances and capacitances between the drain, gate and source at the simulation frequency, instead of introducing π or T equivalent circuits between every two nodes in the simulation representation of the amplifier. Hence, in place of six components, just two components are employed i.e. one is resistive component and the other one is a reactive component. The values of these components are approximated by electromagnetic simulations. Two different formulas, using Z parameters are given, which require the approach used for directing signals between two terminals. These are given in equation 2.6 and 2.7. First equation is utilized for differential signals, while equation 2.7 is used for calculating the input impedance at port 1 [8]. Likewise, signal traces involved the series resistance and series inductance. Parasitic capacitance presented to the substrate is also included [9].

$$Z_{dd} = Z_{11} - Z_{12} - Z_{21} + Z_{22} \tag{2.6}$$

$$Z_{se} = Z_{11} - Z_{12}Z_{21}/Z_{22} \tag{2.7}$$

Parasitic inductances should also be taken into account in order to enhance the model of cascade stage [10]. If we suppose that the expected parasitic inductances have exact values, then this means that the single-ended impedance is very precise because the signal is provided at just one terminal. The errors in the calculated current between the estimated network and a pi or tee equivalent circuit is maintained less than 20% in the differential signal case, when the amplitudes of the differential signals and the phases are altered. The parasitic impedance is added in parallel to the small input impedance. However, the errors due to photo-lithographic effects may go beyond 20% in taking out RC from design to the fabrication [11].

2.2.4 Impedance across the GATE terminal:

A number of resistive components must be included at the drain, gate, source and substrate in order to obtain a thorough model of device. In this way, the power gain, input impedance and output impedance and phase delay between the current and gate voltage V_G can also be found correctly. The value of resistance for the drain and source usually rely on the resistivity in the respective regions and the way these regions are attached. Substrate resistance can be given

by using a resistor of nearly 10GHz frequency [12] and for greater frequencies, by a parallel RC circuit [13]. To decrease the ground resistance, guard rings are mostly employed.

While further discussing about gate resistance, we will study about the gate's structure. It is constructed mainly by the silicided poly-silicon, whose resistance is nearly 10 ohms per square [14], denoted by R_{sq}. Its lateral resistance $R_{g,lateral}$ is calculated using equation 2.8. The value of α becomes one third if the gate is connected at one side. It becomes one twelfth when the gate is present at both sides [14].

$$R_{g,lateral} = \alpha \frac{W}{L} R_{sq} \tag{2.8}$$

$$R_{g,vertical} = \frac{r_c}{WL} \tag{2.9}$$

A contact resistance exists in the MOS transistor gate between the silicide and the poly-silicon. It is denoted by $R_{g,vertical}$ and is shown in Figure 2.5a. Usually it is not discussed in transistor models. Suppose that the contact resistivity is given by r_C, then the supplementary contact resistance is calculated using equation 2.9. This supplementary contact resistance can have a large value as that of found in equation 2.8. Therefore, it is considered a main feature for devices with gate lengths smaller than 350nm. Especially at higher frequencies, it becomes vital to account the resistance factors, to get the exact results of transistors. The sum of these two equations 2.8 and 2.9 is usually shown by a single resistor. To decrease the gate resistance, silicised gates or multiple contacts are used. It can also be lowered by separating the device into many parallel devices.

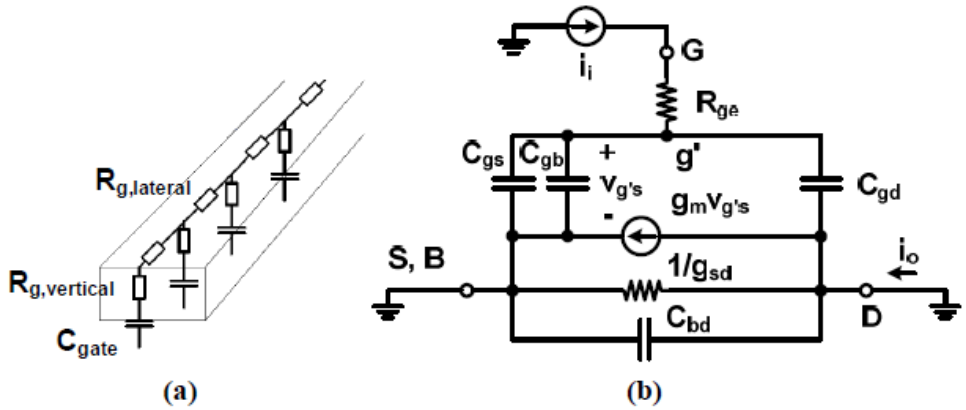


Figure 2.5 (a) Vertical gate resistance

(b) Circuit to estimate

At the present time, CMOS technologies have improved further. In newly developed 45nm CMOS technologies, a metal gate is employed instead of silicided poly-silicon gate [15]-[16]. Gates with thicker layer of oxides can be manufactured using high-k metal gate technology. It still shows better electrical properties. Some better results have been found in literature, e.g. an explanation of gate leakage lessened up to 25X has been shown in [16]. The increase in gate leakage power has turned out to be a large segment in total power utilization in microprocessors [17], therefore, this factor i.e. development in lessened gate leakage is a very significant factor.

Next, the figure of merits (FoM) of the device will be discussed. When we talk about FoM, the two most general FoMs of the transistor devices are the maximum oscillation frequency f_{max} and transition frequency f_T. When a DC current is given to the drain and a ground source [5], then the frequency at which the small-signal current gain is equal to unity is known as transition frequency f_T. The small value of current through C_{gd} is ignored while calculating transition frequency. By the means of circuit in Figure 2.5b, an approximation of f_T is formulated, given in equation 2.11. C_g is the whole capacitance present at the gate to ground, as given in equation 2.10. Intrinsic and extrinsic capacitances both are counted in C_g.

$$C_g = C_{gs} + C_{gb} + C_{gd} \tag{2.10}$$

$$f_T = \frac{1}{2\pi}\frac{i_0}{i_i}\Big|_{vds=0} = \frac{1}{2\pi}\frac{g_m}{C_g} = \frac{1}{2\pi}\frac{g_m}{C_{gs} + C_{gb} + C_{gd}} \tag{2.11}$$

Maximum oscillation frequency f_{max} is also known as unity power gain frequency. To calculate f_{max}, the device is considered to be matched conjugately at both input and output terminals. In this way, unilateral power gain is measured [5]. Tt is defined as that frequency at which power gain reduces to unity.

Equation 2.12 gives the relationship between f_{max} and f_T.

$$\omega_{max} \approx \frac{\omega_T}{\sqrt{4R'_{ge}\left(g_{sd} + \omega_T C_{gd}\right)}};\ R_{se} \ll R_{ge} \tag{2.12}$$

From this equation, we can see that the effective gate resistance R'_{ge} can reduce the effectiveness of the transistor. Yet, f_{max} is a parameter of small-signal model, a conjugate-matched output is assumed, that is probably not the situation in the amplifier's output stage [18] and can nearly be used in the driver stages where the signal levels are smaller. The gate resistance can be decreased by using any of the layout methods given before. Also, impedance matching practices are largely found in literature.

Chapter 3

Theory of RF Power Amplifier

3.1 Basics of Power Amplifier

Amplification of a signal means to increase or boost up signal power of certain radio frequency. There are certain stages/modules of a RF Power amplifier and each of these stages have specific job to do in order to make the Power amplifier work perfectly. The following are the main modules of an RF Power amplifier:

3.1.1 DC Biasing

- Fixed base biasing of transistor
- Collector feedback biasing of transistor
- Dual feedback biasing of transistor
- Emitter feedback transistor biasing
- Transistor biasing using Voltage divider

3.1.2 Amplifier Gain

3.1.3 Power Added Efficiency

3.1.4 Linearity

3.2 Classes in Amplifiers

3.2.1 Class A

3.2.2 Class B

3.2.3 Class AB

3.2.4 Class C

3.2.5 Class D

3.2.6 Class E

3.2.7 Class F

3.1.1 DC Biasing

Transistor Biasing is the process in which an accurate DC voltage and current is provided to the transistor so that a low power AC input signal can be amplified correctly by the transistor. Figure 3.1 shows a simple DC biasing of a transistor.

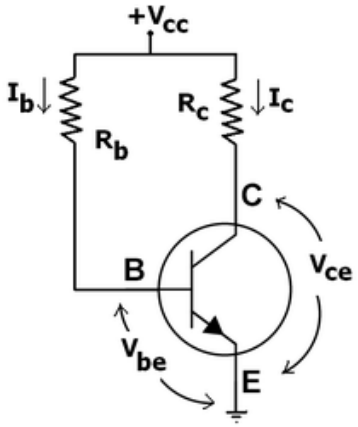


Figure 3.1 Basic DC Biasing of a transistor

Usually a transistor has three regions of operation i.e. Cutoff Region, Active Region and Saturation region. The transistor will function in any of these three regions depending upon the biasing value of its base current, collector voltage and collector current and therefore a transistor will operate as a linear amplifier only if proper DC biasing is provided.
For an Amplifier, the transistor has to function within the active region of operation and to establish the correct biasing values, proper selection of bias resistors are required in order to provide correct voltage and current to the base and collector of the transistor. Functioning of a transistor between the extreme points of a load line is referred to as "Quiescent Operating Point" or Q-point.

The proper biasing of any transistor can be achieved by the process of Base Bias.
The task of "DC biasing level" is to set the Q-point of a transistor correctly by keeping the Collector current (I_C) constant without the presence of any input signal. The DC operation point is set by the value of the biasing resistors which are connected to the transistor terminals and the DC supply voltage termed V_{CC} [19].
In setting up the DC biasing, proper selection of coupling and bypass capacitors are required so that one transistor stage will not affect the working of the next transistor stage.

Base Biasing of a Common Emitter Amplifier

There are two forms of transistor biasing which is *Beta Dependent and Beta Independent* and the biasing voltage of any transistor is largely dependent on the transistor beta value, (β). Since the beta value of any transistor may not be the same for another transistor, so biasing of one transistor may not work on another transistor.

Following are some of the forms of Base Biasing of a transistor using a single Power supply V_{CC}.

1. Fixed base biasing of a transistor

Figure 3.2 shows a simple form of "fixed base biasing of a transistor" in which two biasing resistors are used in order to control the biasing voltage for base and collector of the transistor. Here the transistor base resistor is used to provide a fixed base current I_B to the base of transistor as long as the supply voltage V_{CC} remains constant.

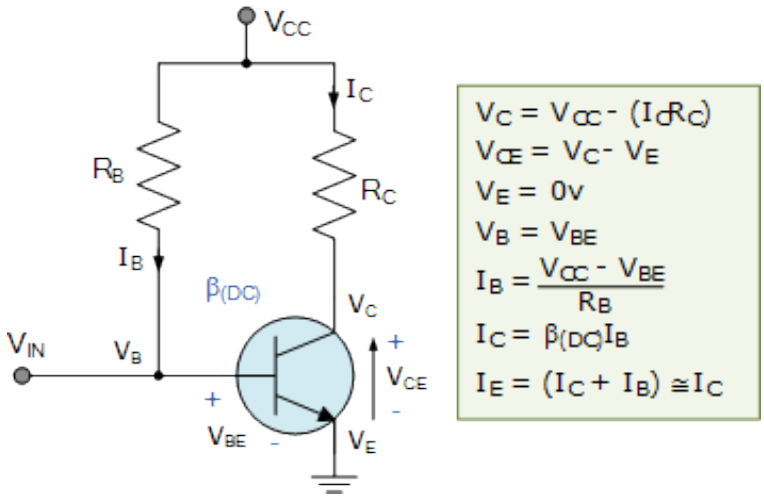


Figure 3.2 Fixed Base biasing

This arrangement of fixed base biasing is beta β dependent so two transistors of different beta β values will receive different value of current and voltage at its base and collector.

This method of biasing using a single resistor cannot keep the voltage and current stable during the operation of transistor and can vary exceedingly. Also the change in temperature of transistor can affect the operating point unpropitious [19].

2. Collector Feedback Biasing of a Transistor

Figure 3.3 shows the self biasing Collector feedback configuration for a transistor. In this configuration only two resistors are required to provide the correct DC voltage and current to the transistor terminals [19]. This type of biasing is also beta dependent biasing method. In figure 3.3, the base resistor R_B is deriving current from the Collector voltage V_C which

ensures that the transistor will works always in the active region regardless of the value of beta and this provides good stability.

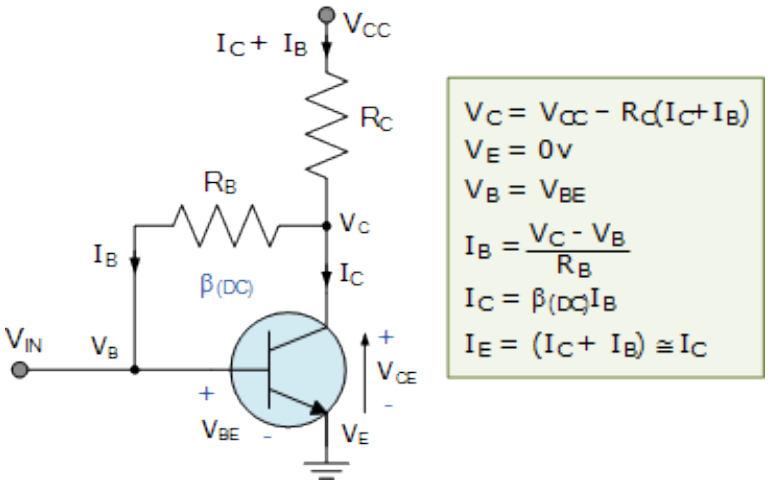


Figure 3.3 Collector Feedback biasing

In this configuration, the base resistor R_B is connected to the collector terminal of the transistor instead of being connected directly to the voltage rail V_{CC}. Now if the current in the collector terminal rises, the collector voltage will fall accordingly, this will result in reduction of the base current and therefore the collector current will reduce automatically to keep the transistor Q-point stable. This method of biasing the transistor is creating a negative feedback from the collector terminal to the base terminal through the resistor R_B.

The voltage drop across the load resistor R_L provides the biasing voltage. If the current across the load resistor increases then voltage drop will also increase which will result in reduced voltage drop across the collector voltage and correspondingly the base current I_B will decrease which in turn lead the I_C current back to normal.

Since there is a continuous feedback from the collector to the base of the transistor to keep the transistor stable so this kind of feedback bias network is good for most amplifier designs for stable amplification.

3. Dual feedback Biasing of a transistor

The biasing in figure 3.4 is called the Dual feedback biasing of a transistor. In this configuration another resistor R_{B2} is connected to the base of the transistor and grounded in order to provide even more stability than the previous version of it.

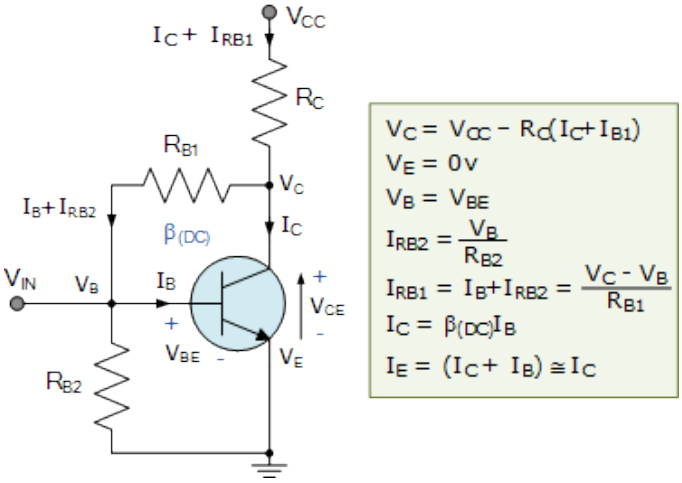


Figure 3.4 Dual Feedback biasing

The value of the resistor R_B is set at such a value so the base current will be equal to nearly 10% of the total collector current [20].

This type of biasing configuration provides feedback network and automatic basing at the same time.

4. Emitter feedback Transistor Biasing

The Emitter feedback biasing is another form of configuration where a more stable biasing of transistor is achieved by taking feedback from the collector as well as from the emitter terminal of the transistor [21]. It is shown in figure 3.5 below.

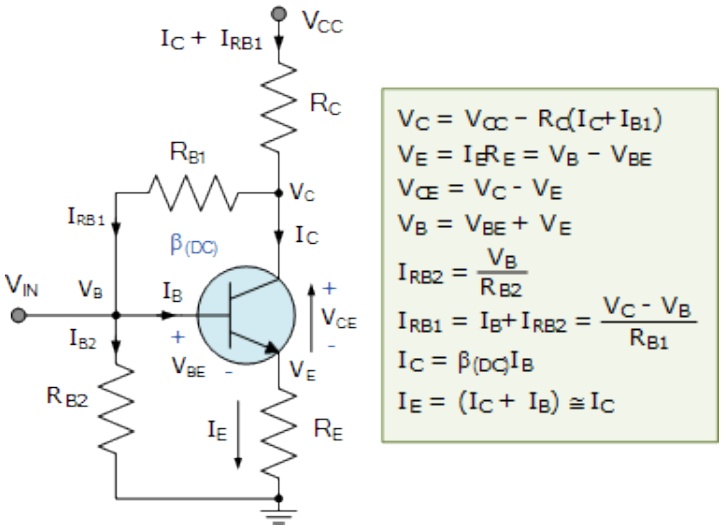


Figure 3.5 Emitter Feedback biasing

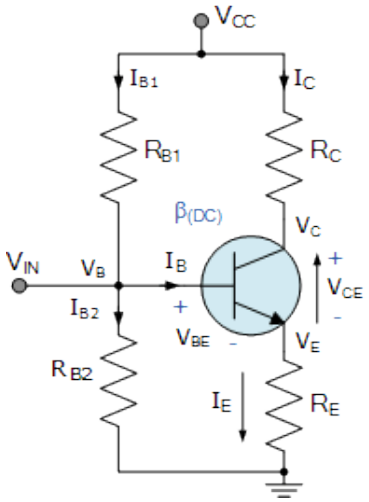
The disadvantage of this biasing configuration is reduced output gain of the transistor because of the base resistor R_B since the voltage across the collector controls the current through R_B producing what is known as the "degenerative feedback".

The biasing resistors are calculated such that the voltage drop across resistor R_E remains 10% of supply voltage V_{CC} and the current across base resistor R_B is 10% of total collector current.

This biasing configuration is best for low power supplies.

5. Transistor Biasing using Voltage Divider

In voltage divider transistor biasing there are 4 resistors used as shown in figure 3.6. The two resistors R_{B1} and R_{B2} are settled in a voltage divider fashion and the base terminal of transistor is connected to the center point of these two resistor network.



$$V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$$
$$V_E = I_E R_E = V_B - V_{BE}$$
$$V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$$
$$V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right)V_{CC}$$
$$I_{B2} = \frac{V_B}{R_{B2}}$$
$$I_{B1} = I_B + I_{B2} = \frac{V_C - V_B}{R_{B1}}$$
$$I_B = \frac{V_B}{R_B + (1+\beta)R_E}$$
$$I_C = \beta_{(DC)} I_B$$
$$I_E = I_C + I_B = \frac{V_E}{R_E}$$

Figure 3.6 Voltage divider Biasing

This configuration of biasing network is widely used for biasing of transistors in many Amplifiers [21]. This biasing technique is independent of changes in beta value as the voltage across base, emitter and collector terminal are dependent on V_{CC}.

The values of the two resistors R_{B1} and R_{B2} are calculated using the voltage divider formula. Since the voltage drop across R_{B2} is much less as compared to R_{B1}, so the base voltage will always be equal to the voltage across R_{B2}.

The base resistor current R_{B2} is usually set at 10 times the value for base current, and this will result in having stable biasing and independence from changes in beta.

3.1.2 Amplifier Gain

The ability of any Amplifier's amplifying ability is measured in terms of output to input ratio. In engineering terms it is called Gain. The output to input ratio could be of Voltage, current or Power. Usually the Gain is measured in dB and in terms of S-Parameters it is defined by S_{21} as shown in figure 3.7

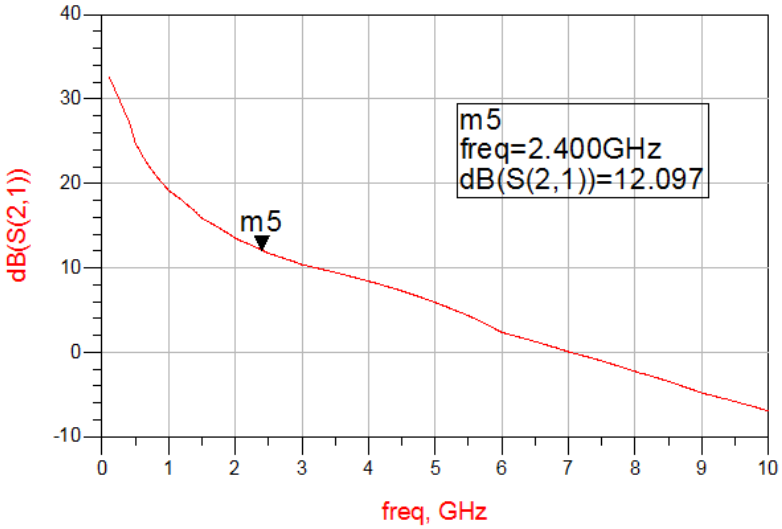


Figure 3.7 Plot of a Power amplifier Gain

Generally the Amplifier increases the amplitude of the input signal by taking energy from the DC source and adding it to the signal [22]. The active circuits have gain greater than 1 means zero dB while the passive circuits will have gain less than one.

The gain of any amplifier is divided into two parts, the gain which is provided by the transistor and the gain achieved by the matching circuits. The transistors which are used for the amplification purpose have their own gain defined by the manufacturer in the datasheet. The maximum gain of the amplifier is achieved if there is perfect impedance matching between the DUT (Device under test) and the source and load [23].

The Gain also depends on the voltage supplied to the device. If the DC biasing of transistor is providing stable voltage then the gain will maintain its peak value. For transistors which are unstable in the frequency of operation, a resistor is usually used for the stability of transistor but it reduces the Amplifier Gain as the value of resistor increases [24].

3.1.3 Power Added Efficiency

Power added efficiency can be defined as the efficiency of circuit to convert the total input power (DC input + RF input) into total RF output power. Mathematically it is defined as:

$$PAE = [(P_{OUT} - P_{IN}) / (P_{DC} + P_{IN})] \times 100\%$$

Power Added Efficiency can never exceed 100%. The PAE graph is shown in figure 3.8.

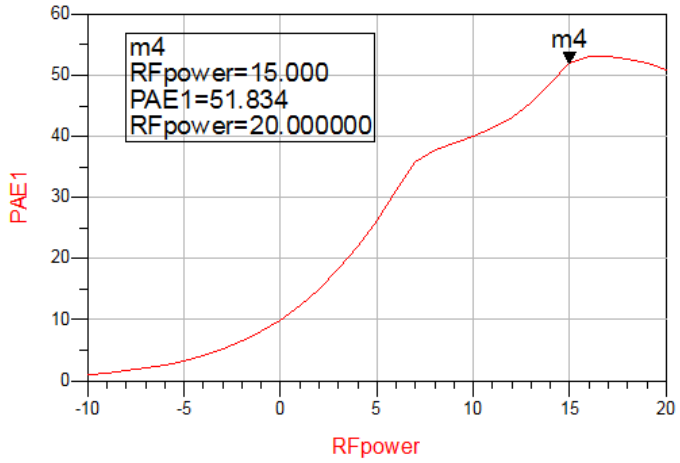


Figure 3.8 Plot of a Power amplifier Power added Efficiency

The X-Axis of the graph shows the input RF-power that is provided to the Power amplifier and the Y-Axis shows the Power Added Efficiency in percentage. As can be seen from this graph that the input RF power ranges from -10dBmto 20dBm. The maximum PAE of 51.8% is achieved at input power of 15dBm which is the P1dB and at 6dB back off point i.e. at 9dBm input power the efficiency becomes 38.8%.

There are different techniques which have been implemented in order to increase the Power added efficiency. The input supply voltage should be kept nearly at the optimum drain voltage of the transistor in order to get the maximum efficiency out of the amplifier. The techniques which can be used to improve the Power added efficiency can be Adaptive biasing techniques, Harmonic suppression techniques, implementation of cascade topology, optimum input output matching circuits etc. Out of many these are some of most recently used techniques which have been implemented in different Power amplifier designs.

Class	Theoretical Efficiency	Experimental Efficiency
Class-A	50% - 60%	35% - 38%
Class-AB	60% - 70%	40% - 45%
Class-B	70% - 79%	45% - 55%
Class-C	80% - 90%	55% - 60%
Class-E	90% - 98%	60% - 69%
Class-F	98% - 100%	70% - 80%

Table 3.1 Comparison of different Amplifiers with their Ideal and Practical Efficiency

In table 3.1, the comparison of different amplifier classes and their efficiencies are shown. It can be seen that the class A amplifier have 50% ideal and 35% practical efficiency. The amplifier efficiency increases as we move from class A to F, for class C the efficiency can vary from 78.5% up to 100% in Ideal case while for practical amplifiers the efficiency is 55%. Finally for class E and F amplifiers the ideal efficiency is 100% while in practical case it is 62% and 80% respectively.

3.1.4 Linearity

Linearity of an amplifier refers to produce a signal which is an accurate copy of the input signal provided to it but the output signal will have an increased power level. The factors which usually affect the linearity of an amplifier are impedance of the load, voltage that is supplied to the amplifier V_{CC}, the gate driving current, and the maximum output power capabilities of the amplifier [25].

Class	Linearity
Class-A	Best
Class-AB	Best
Class-B	Average
Class-C	Worse
Class-E	Worse
Class-F	Worse

Table 3.2 Amplifier Classes and their Linearity behavior

In table 3.2, the comparison of amplifier classes is shown for their linearity. Class A amplifiers are pretty good in their linear behavior but as we move down from class A to class F it can be seen that the linearity becomes moderate for class B and reaches to poor performance for class F amplifiers.

The linearity and efficiency of amplifiers are two opposite factors and in designing of an amplifier there is always a tradeoff between these two characteristics. If an amplifier has a linear characteristic then its efficiency will be either poor or moderate [26]. Similarly for amplifiers with good efficiency, their linearity would suffer as it would be poor.

3.2 Classes in Amplifiers

Amplifiers are divided into different classes depending upon their behavior and way of operation. The main characteristics of any amplifier are Gain, total output power, S-parameters, Linearity, and efficiency and there is always barter between them.

Typically for loads whose impedance is 4 Ohms or 8 Ohms, the power amplifier should have enough power to drive such low impedance speaker and must provide high current to such loads. These amplifiers are usually found as the final stage of any amplification system.

Basically, amplifier classes are structured in such a way in order to distinguish between them according to the configuration of circuit design, and operation method. Thus amplifier classes are the appellation for differentiating different types of amplifiers based on their characteristics.

Amplifiers can be classified as linear with low efficiency and non linear with high efficiency output. These classes are mainly categorized into two groups. The first group consists of classes A, B, AB and C which are controlled in an old fashion by simply providing voltage to the gate of transistor so that the Q-point lies between the Saturation and cutoff region.

The second group consists of classes D, E and F and these amplifiers uses switching method in order to drive the gate of transistor with the help of circuits like pulse width modulation (PWM) and this keeps the transistor to maintain its Q-point between the ON and OFF state [27]. A more detailed structure of classes of amplifier is now explained:

3.2.1 Class A

The Amplifiers of this class are famous for their linear characteristics as compared to other classes. They have very low signal distortion intensity and are considered the best due to this nature.

Basically the class A amplifiers mostly use a single transistor and it can be a BJT, FET or a MOSFET which is connected such that the input is provided to the base of the transistor, the emitter is grounded and the collector is used to get the output signal. In this class, the transistor is continuously being provided DC source voltage into its collector-source terminals even if the base terminal is open, which means that the transistor is always kept within the active region of operation and it always stays switched ON which is the main drawback of this class.

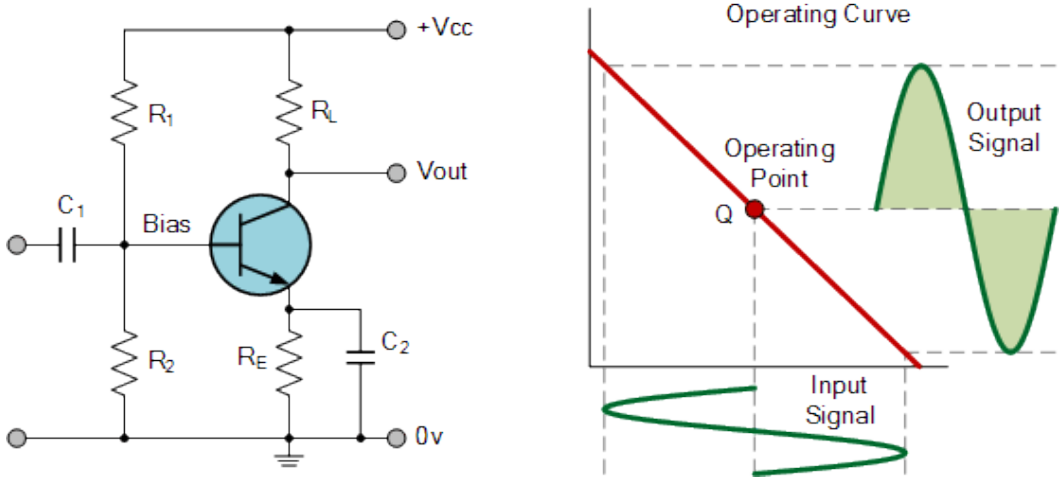


Figure 3.9 A basic Class A Amplifier Schematic

In figure 3.9 a simple schematic of a Class A amplifier is shown at the left side and its characteristic curve is shown at the right side. The class A amplifiers achieve their high linearity and maximum output gain by keeping the amplifier always in an ON state. It also provides a full 360 degree of output waveform as can be seen in future 12.

As mentioned earlier that the class A amplifier operates in active region of operation so the transistor biasing for its gate (or base) and collector should be properly chosen to guaranty low distortion at the output stage. But since the transistor is kept always in the ON state, the transistor shows a continuous loss of power in the form of heat [27].

Because of this continuous power losses in the form of heat, the class A amplifier has a very low efficiency which is nearly 30% and this makes it unsuitable for amplifiers with high output power. Also since this amplifier has to provide high output current at the collector terminal, the power supply for this amplifier should be designed properly so that the DC supply should be ripple free and with low noise. For such disadvantages, other types of amplifiers are designed for getting better output and efficiency.

3.2.2 Class B

Due to the low efficiency and heat losses in Class A amplifiers, the class B amplifier was designed. In a class B amplifier there are two transistors used. These transistors can either be BJTs, FETs or MOSFETs and each of the two transistors has to work only for one half of the waveform, meaning that each transistor will act in a PUSH-PULL topology and only for half of the total waveform [28].

The Efficiency in class B amplifiers is much greater as compared to class A amplifiers, but the negative side of this amplifier is that its linearity is lower as compared to class A amplifiers.

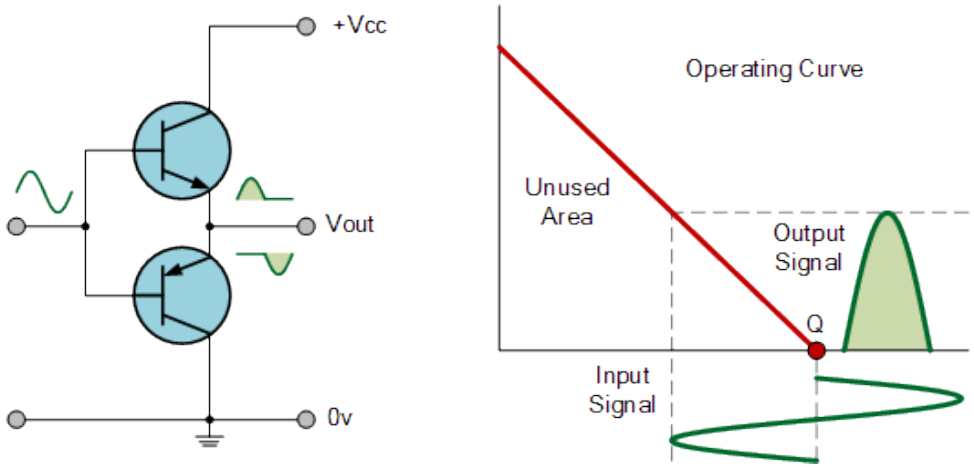


Figure 3.10 Basic configuration of Class B Amplifier

Figure 3.10 shows the basic configuration of class B amplifiers and its operating curve. The circuit works as follows, when the positive half of signal is applied at the input terminal then the transistor with positively base biased starts to conduct while the negatively base biased transistor stays in OFF stage. In the 2nd half cycle the transistor with positively base biased turns OFF while the transistor with negatively base biased starts to conducts. Hence each of the transistors turns ON for only half cycle.

As we saw that each of the two transistor works only for half cycle or 180 degrees and their output will also be half of total waveform, then there is a combiner at the output stage which combines these two half waveforms in order to give a complete waveform [28].

Since we know that the base emitter junction of a BJT will start to conduct properly only when its voltage drop is higher than 0.7 volts. In case of Class B amplifiers, if the input voltage is equal to or less than 0.7 volts than the base-emitter junction will not conduct properly and the output waveform will be distorted and this makes a class B amplifier unsuitable for some audio amplifiers. This kind of distortion produced is known as Crossover Distortion and to overwhelm this problem Class AB amplifier were designed.

3.2.3 Class AB

The class AB amplifier is an amalgamation of class A and Class B amplifiers. As it was discussion in Class B amplifiers that emitter base junction voltages below 0.7 volts produces Crossover distortion and to remove this problem Class AB amplifiers are introduced. These

amplifiers are very famous for audio amplifier designs. Class AB amplifier is a modified form of Class B amplifier in the sense that in class AB amplifier both the transistors works at the same time to obliterate the problem of Crossover distortion [29].

In Class AB amplifier, the two transistors biasing voltage is kept very small so that it can be biased at point very close to its cut-off point. So for more than a half cycle the transistor will be turned ON for any input signal.

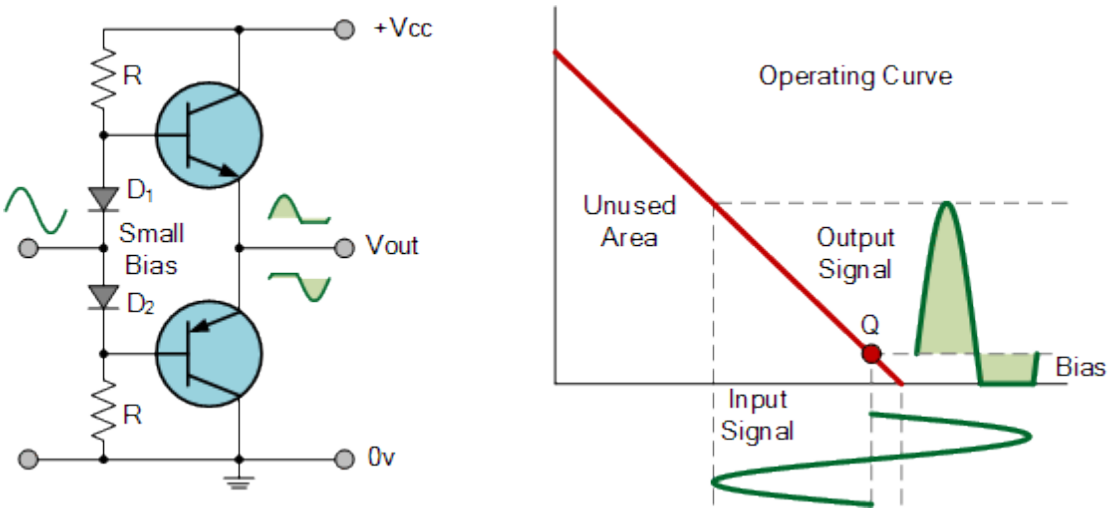


Figure 3.11 Circuit Configuration of Class AB Amplifier

Figure 14 shows the basic schematic of a class AB amplifier. There are two diodes are two resistors which are connected in series in the emitter base junction of the transistors. Using these resistors and diodes the biasing voltage of these transistors are reduced in order to annihilate the crossover distortion [29]. So the Class AB amplifier provides the combined advantage of efficiency and linearity of both Class A and Class B amplifiers.

3.2.4 Class C

Talking about amplifier efficiency the class C amplifier is the most efficient amplifier as compare to Class A, B and AB amplifiers. As we discussed earlier that these three classes of amplifiers has a linear output signal and phase compared to its input signal.

The Class C amplifier on the other hand is biased in such a way that for more than a half input signal the current at the output is zero [30].

With such biasing technique the Class C amplifiers provides output efficiency of nearly 80% but the price paid for such a high efficiency is the high distortion of output signal. Therefore this Class is mostly not used for audio amplifiers.

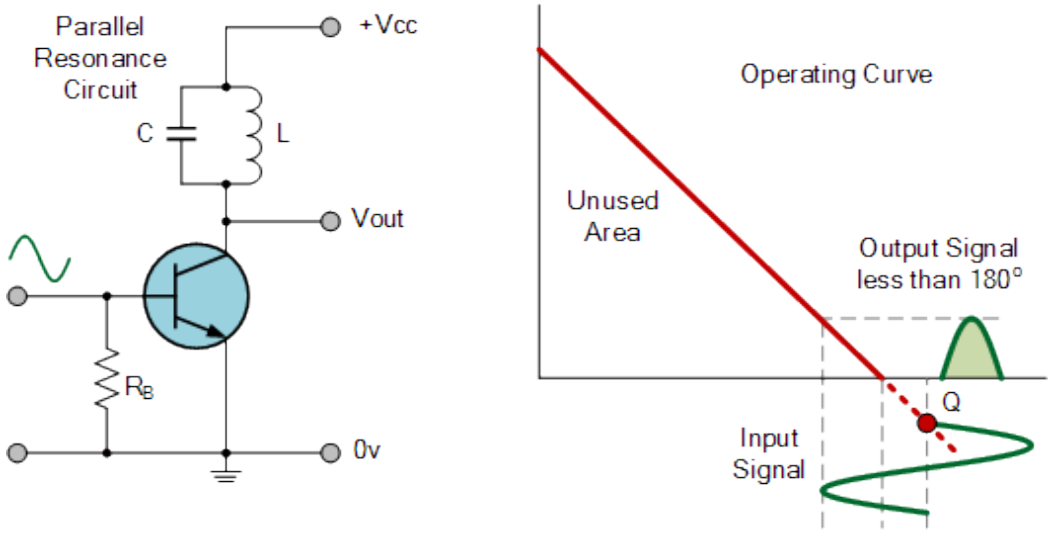


Figure 3.12 Schematic configuration of Class C Amplifier

Class C amplifier is shown in figure 3.12. This class is mostly used in the design of oscillators and high frequency amplifiers [30].

3.2.5 Class D

The Class D amplifier is a Pulse width modulation (PWM) or switching amplifier and is mostly used for the design of audio amplifiers. In this amplifier, the device under test (DUT) can be a BJT, FET or MOSFET and it works as a simple switch instead of linear gain device. The input analog signal which is to be amplified is first converted into a train of ON-OFF pulses so that it can be fed to the gate of transistor and it will then turn ON and OFF depending upon the state of input pulse signal. Usually a simple pulse width modulation (PWM) is used in order to change the input signal from analog to ON-OFF pulses. After the signal is converted, it is fed into the device where it receives amplitude gain and then at the output side the amplified signal is again transformed from pulses to analog signal with the help of low pass filters which consists of capacitors and inductors [31]. This amplifier can provide efficiency of 90-95%.

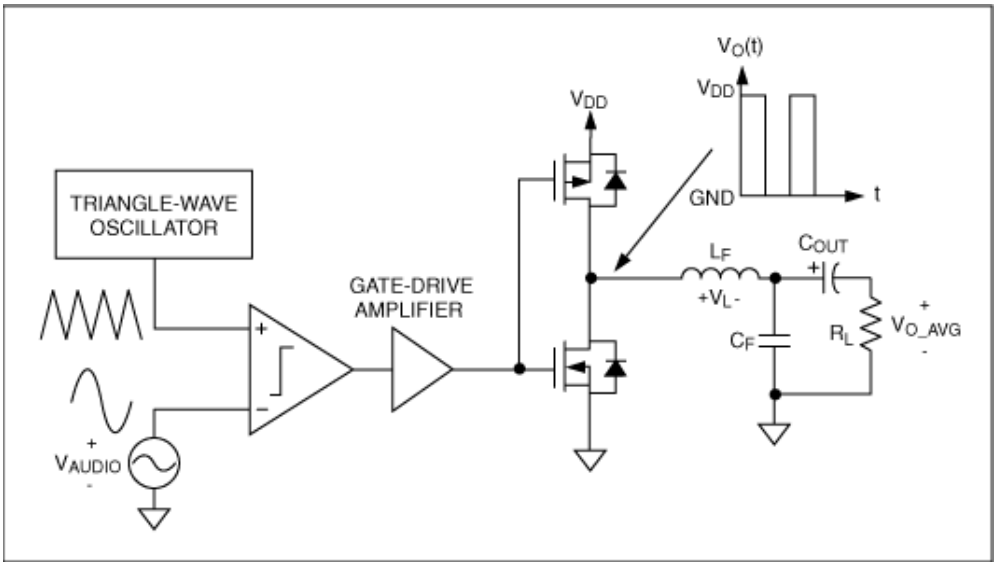


Figure 3.13 Internal diagram of Class D Amplifier

Figure 16 shows the basic block diagram of a Class D amplifier. The schematic is known as a half bridge Class D amplifier. For the compensation of imbalance in gate voltage a feedback network is also employed in this circuit which helps to recover the low voltage problems [31][32]. The class D amplifier can be used for the design of audio amplifiers as well as power amplifiers.

3.2.6 Class E

The Class E amplifier is designed in order to remove the problems faced in Class A, B, AB, C and D amplifiers. This amplifier is also a switching amplifier where the input signal at gate of transistor is in the form of pulses while at the output side a low pass filter is used to change the amplified pulses back to analog signal. The major Problem in Radio Frequency (RF) amplifiers is the switching losses in these devices and to eliminate such losses a technique is used to switch the device only when there is no voltage across the DUT [32][33]. Another problem is the different capacitances that are present within the amplifier which affects the efficiency and gain of amplifier. Three capacitances can be seen at work within a Class E amplifier, these are input capacitance, output capacitance and the capacitance within the DUT (from gate to drain terminal). The capacitance within the device can be reduced by making the resonant circuit more inductive and also by careful switching of DUT so it will be switched ON only when the capacitor at the output side is completely discharged. Short circuit resistors can be used at the output side of the amplifier to help discharge these

capacitors and such resistors are known as bleeder resistors but the only problem which lies with such resistors is that they reduce the total output gain of the amplifier [33].

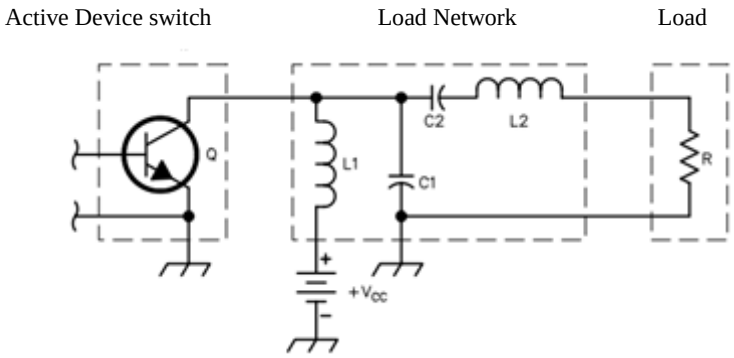


Figure 3.14 (a) Basic configuration of Class E Amplifier

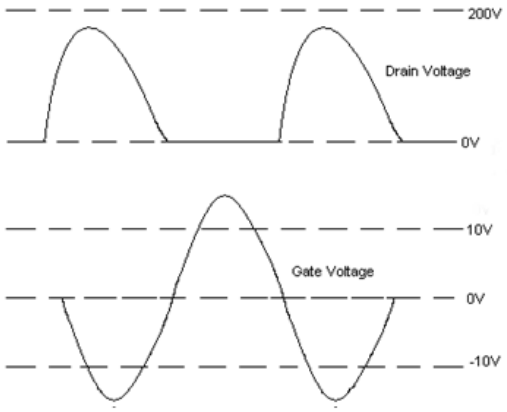


Figure 3.14 (b) Voltage across the gate and drain of transistor

Figure 3.14 (a) show basic configuration of a Class E amplifier and Figure 3.14 (b) show the respective gate and drain voltages. From the graph it can be seen that for the gate voltages from -10V to +10V the drain voltage can vary between 0V and 200V.

The components which are shown in the circuit diagram are carefully tuned so that the capacitance within the transistor (gate to drain) and the shunt capacitor which is connected at the drain of transistor is completely discharged before the turning ON of transistor which will ensure that a drain to source voltage can only be seen when there is voltage at the gate terminal [33].

The capacitance at the input terminal can be reduced by either employing a driver circuit at the gate terminal of transistor or by using an inductive circuit which will make the input reactance overall inductive.

The output capacitance is also reduced in the similar manner where an inductor or a step down transformer is used. Class E amplifiers can provide very high efficiency and moderate linearity and most of the RF amplifiers are designed using a Class E scenario.

3.2.7 Class F

Class F amplifiers are considered as one of the most efficient amplifiers. These amplifiers deploy such output filters which help to reduce the harmonics at the output side of device and this helps to shape the output waveform which will result in reducing the total power dissipation by the device and it would lead to increased efficiency of the amplifier.
Figure 3.15 (a) show the general diagram of Class F amplifier where as Figure 3.15 (b) show the voltage and current waveforms across its output terminals.

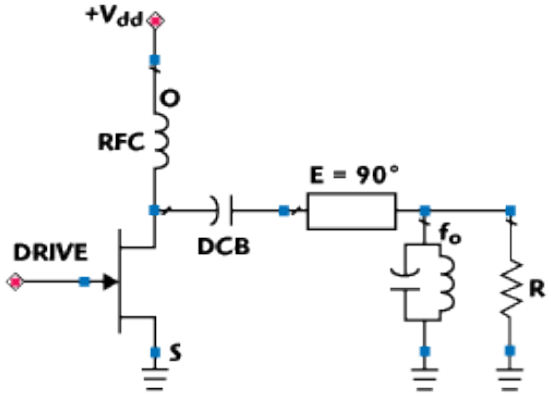


Figure 3.15 (a) A simple Class F amplifier

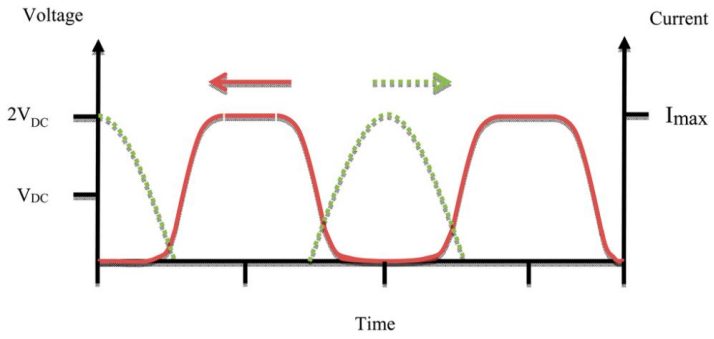


Figure 3.15 (b) Voltage and Current waveforms at the output terminal of Class F amplifier

From the figure it can be seen that the input voltage at the gate terminal is a square waveform while its current graph is a half- rectified sine wave. In ideal case the current and voltage do not overlap as can be seen from this graph. This kind of ideal amplifier provides 100% efficiency. For getting maximum efficiency, the bias point of the device should be set at the cut-off region for switching of transistor. From the Fourier analysis we know that a square voltage waveform represents only the fundamental and odd harmonics of frequency whereas the current waveform of half rectified shows only the fundamental and even harmonics of frequency. Therefore the load at the output terminal should present open circuit for odd harmonics and short circuit for even harmonics. [33].

Tuning circuits which are known as the tank circuits are mostly employed for this operation which is used to represent both open and short circuit load. In the above figure 3.15, the capacitor C1 and inductor L1 is used to present the short circuited load for the even harmonics while the quarter wave line is used to represent the open circuited load for odd harmonics. [32 - 33]

This class of amplifier is very efficient in terms of Power added efficiency (PAE) but presents very poor linearity and thus can be used for the design of Radio Frequency amplifiers however an audio amplifier cannot be designed with a Class F amplifier as it will present poor linear output with respect to its input.

Chapter 4

Design of Integrated Power Amplifier

4.1 Selection of Device

For the design of a Power amplifier the first step is the selection of the device. This selection depends on many important factors which need to be considered first before selecting a transistor. The factors may include the frequency of operation, output power gain, supply voltage V_{CC} etc. This selection also defines the throughput of our Power amplifier and its overall efficiency. In our proposed Power amplifier, the frequency of operation is 2.4 GHz and output power gain is expected to be at least 14 dB so one of the perfect candidates for the device is ATF-53189 which can operate from 50 MHz up to 6 GHz and the typical output power gain of this device is 15 dB at 2.4 GHz without the use of impedance matching circuits.

4.2 Design specifications

Frequency	:	2.4 GHz
Gain	:	16 dB for single stage and 27dB for two stage Power amplifier
Power Added Efficiency	:	40% for both single and two stage Power amplifier.
Device	:	ATF-53189
Substrate	:	Taconic with dielectric constant of 3.2

4.3 DC Biasing

The first step in the design of any power amplifier is the implementation of DC biasing circuit. Every transistor has its own optimized value of voltage and current where the transistor provides maximum gain and works efficiently. This value of voltage and current can be taken from the data sheet of transistor. In the proposed Power amplifier the transistor used is ATF 53189 which is Pseudomorphic HEMT in SOT 89 Package. Its working frequency range is 50 MHz to 6 GHz. For our proposed Power amplifier of 2.4 GHz, at optimum DC biasing which is 4v and 135mA, the transistor typically provides output Gain of 15dB. A voltage divider circuit is designed in ADS for the DC biasing of our proposed Power amplifier which is shown in figure 4.1 below.

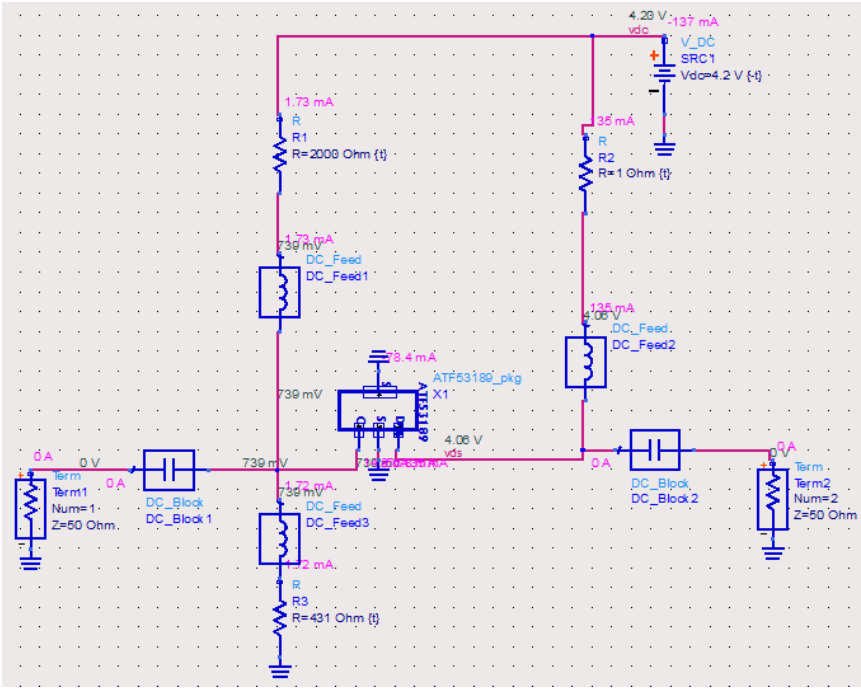


Figure 4.1 DC biasing circuit of the proposed Power amplifier

In figure 4.1 three resistors R_1, R_2 and R_3 are used for the design of DC biasing circuit. The values are set such that it will provide drain voltage of 4v and 135mA current as required for the optimized operation of the Power amplifier.

4.4 Stability Test

Table 4.1 shows the S-Parameters of the transistor ATF-53189. Column 1 shows the frequency range of this transistor and the S-parameters for those frequencies. Since this Power amplifier is to be designed on 2.4 GHz frequency the exact values of S-parameters are to be taken from the simulated design in ADS software which is performed in section below.

ATF-53189 Typical Scattering and Noise Parameters at 25°C, V_{DS} = 4.0V, I_{DS} = 135 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.916	-47.6	32.6	42.775	152.6	-37.7	0.013	66.7	0.458	-40.7	35.2
0.2	0.897	-83.9	30.9	35.086	133.4	-33.2	0.022	49.5	0.43	-73.3	32.0
0.3	0.885	-109.5	29.1	28.4	119.5	-31.4	0.027	37.8	0.407	-96.8	30.2
0.4	0.878	-127.5	27.4	23.322	109.2	-30.8	0.029	29.9	0.39	-113.4	29.1
0.5	0.859	-151.3	24.8	17.286	98.2	-31.4	0.027	21.3	0.399	-148.1	28.1
0.6	0.857	-159.9	23.3	14.647	93.1	-31.1	0.028	18.6	0.401	-155	27.2
0.7	0.855	-166.5	22.1	12.703	88.7	-31.1	0.028	16.9	0.402	-160.1	26.6
0.8	0.854	-171.9	21.0	11.225	84.9	-30.8	0.029	15.6	0.4	-164.3	25.9
0.9	0.852	-176.6	20.1	10.065	81.5	-30.8	0.029	14.6	0.398	-167.7	25.4
1.0	0.854	179.1	19.2	9.101	78.2	-30.8	0.029	13.9	0.396	-170.6	25.0

ATF-53189 Typical Scattering and Noise Parameters at 25°C, V_{DS} = 4.0V, I_{DS} = 135 mA

Freq.	S_{11}			S_{21}			S_{12}		S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
1.5	0.851	162.1	15.8	6.197	63.9	-29.9	0.032	11.3	0.386	178	22.9
2.0	0.85	147.7	13.5	4.726	50.7	-29.4	0.034	9	0.374	169	21.4
2.5	0.846	133.9	11.7	3.851	37.7	-28.4	0.038	5.7	0.364	160.4	19.3
3.0	0.844	119.8	10.4	3.301	24.6	-28.0	0.04	0.8	0.362	152.4	17.0
3.5	0.854	110	9.4	2.968	13.9	-27.7	0.041	-4	0.382	143.7	16.2
4.0	0.863	100.2	8.4	2.636	3.1	-27.5	0.042	-8.7	0.401	135	15.3
5.0	0.883	80.5	5.9	1.972	-18.5	-26.9	0.045	-18.1	0.441	117.6	13.3
6.0	0.902	60.8	2.3	1.308	-40	-26.6	0.047	-27.6	0.48	100.2	10.3
7.0	0.939	44.1	0.0	1.005	-60	-27.1	0.044	-38.6	0.542	87.3	10.3
8.0	0.956	31.8	-2.3	0.769	-78.3	-27.7	0.041	-49.6	0.605	72.8	9.8
9.0	0.94	23.2	-4.8	0.573	-95	-29.1	0.035	-62.1	0.668	58.1	6.6
10.0	0.948	13.6	-7.0	0.448	-110.5	-30.8	0.029	-80	0.721	45.6	5.9
11.0	0.942	2.6	-8.9	0.36	-127.7	-34.0	0.02	-118.6	0.757	35.2	4.6
12.0	0.92	-4.2	-10.5	0.297	-141.8	-38.4	0.012	-173.3	0.784	24.8	2.1
13.0	0.959	-15.4	-12.4	0.239	-161.9	-34.9	0.018	105	0.794	15.1	3.5
14.0	0.951	-20	-14.5	0.188	-172.9	-35.4	0.017	74	0.812	7.7	0.4
15.0	0.942	-21.1	-15.7	0.164	178.7	-35.4	0.017	84.5	0.847	1.4	-0.6
16.0	0.956	-24.2	-16.5	0.149	167.8	-34.0	0.02	82.4	0.853	-2.9	0.0
17.0	0.958	-31.8	-16.2	0.155	154.1	-31.4	0.027	87.3	0.866	-7.8	1.2
18.0	0.92	-43.5	-15.9	0.161	136.9	-28.4	0.038	78.5	0.848	-14.7	-2.1

Table 4.1 S-parameters of transistor ATF-53189

For the design of any amplifier it has to be sure that the transistor is stable in the frequency range for which it is to be designed. The stability test assures that the transistor is stable and is not oscillating as for different values of DC biasing and impedance matching circuits the amplifier might oscillate and become unstable. As stated in Rolette stability factor, the value of K > 1 and Δ < 1 for the transistor to be stable as defined in the equation (1) below.

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{11}||S_{12}|} \qquad (1)$$

where, $\Delta = S_{11}S_{22} - S_{12}S_{21}$

For the stability test of the proposed Power amplifier, a simple stability test is taken in ADS as shown in Figure 4.2 where a built-in stability factor block is used. The values of S-Parameters are set from 2.3 GHz to 2.6 GHz and step size is set to 0.01 GHz.

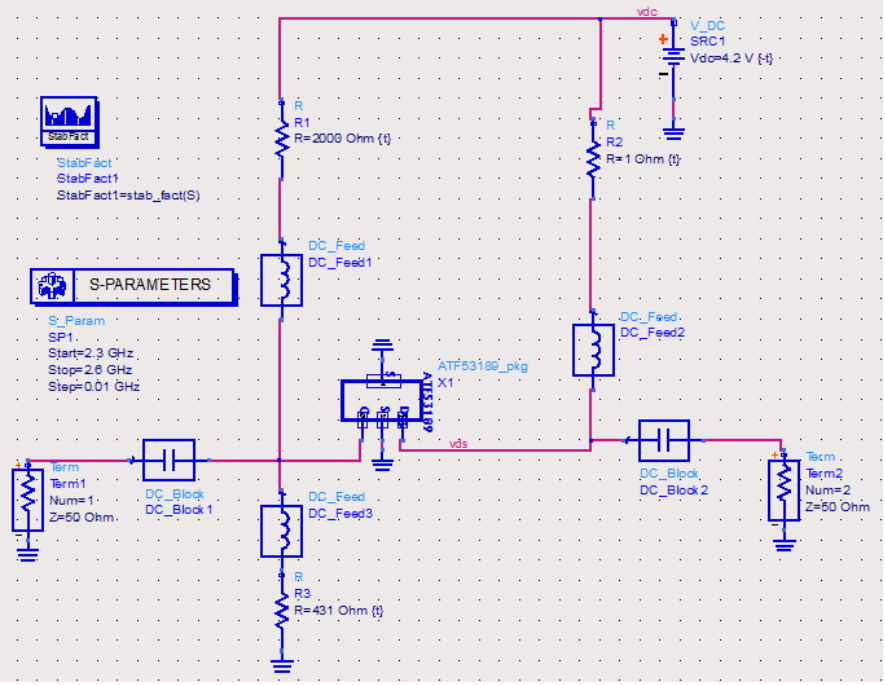


Figure 4.2 Stability test circuit for 2.4 GHz Power amplifier

Test results show that the value of stability factor K is 1.151 for 2.45 GHz which assures that the transistor is stable. Figure 4.3 shows the value of stability factor K.

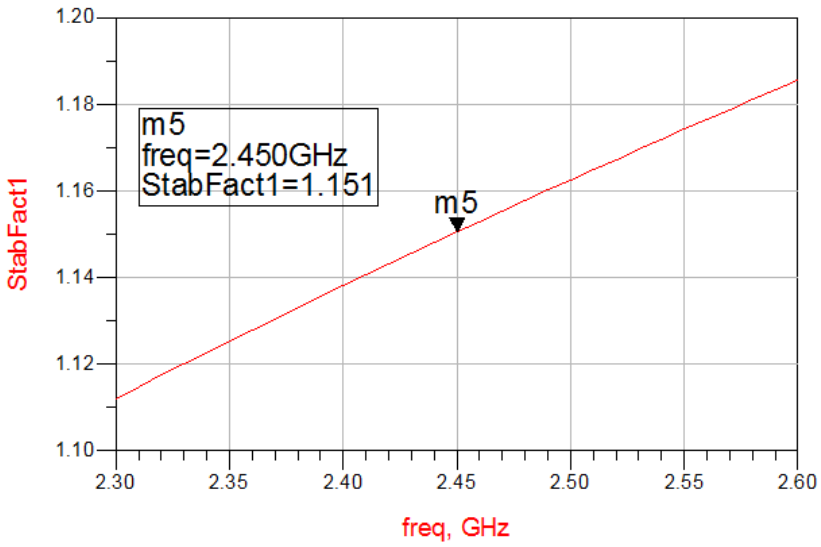


Figure 4.3 Stability test result for the proposed power amplifier

4.5 Input and Output impedance matching circuits

4.5.1 Matching Techniques

In any Radio frequency Amplifier, the input and output impedance of the device should be matched with the source and load respectively. The maximum power transfer is only possible if this impedance is perfectly matched. Each transistor has its own input and output impedance and these values are usually known from their datasheets. In terms of matching networks, the S- parameters are considered for finding if the input and output is perfectly matched. For two ports network there will be 4.

Types of matching circuits

Basically there are three main types of matching circuits:

- Transformer Matching
- LC Matching
- Transmission Line Matching

4.5.1.1 Transformer Matching

For the impedance matching the first technique is the transformer matching. In this technique a transformer is designed having some primary and secondary turn ratios. These turns can be on the PCB board itself using the transmission lines or can also be on any bobbin with specified core. Since the Radio frequency ranges in MHz so the core used should be of Ferrite material as the Iron core works only in low frequency ranges.

Impedance Matching using transformer designing provides a wideband impedance matching but there are limitations in restricted range of impedance to be matched due to limited turn ratios.

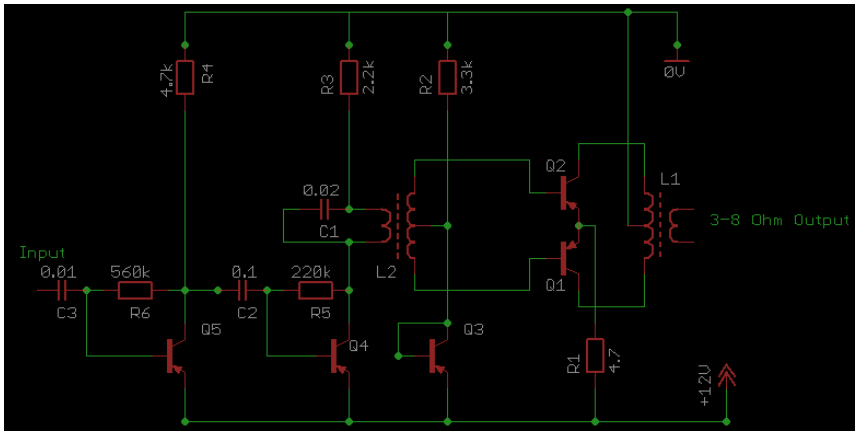


Figure 4.4 Transformer matching for wideband impedance matching

Here in figure 4.4, a simple amplifier is shown with two transformers L1 and L2. The L2 is the input matching transformer and the L1 is the output matching transformer. Both of these transformers are center tapped and each using ferrite core. Their turn ratio is selected such that for achieving maximum power transfer from input to the device and then from the device to the output.

4.5.1.2 LC Matching

In LC matching technique, lumped components are used in order to match the device impedance with the source and load. The two components which are used for matching the impedance are Inductor and capacitor. The LC matching provides a narrow bandwidth match and such matching network is practically used in the frequency range from 30MHz to 300MHz. This type of matching provides easy tuning of impedance even after fabrication.

Since the Lumped components allow tuning the impedance on circuit board, the manufacturers use these components to determine the impedance of the device. They use variable inductors and capacitors to find the maximum output power and lowest return losses for the device and the perfect match can then determine the impedance of the device.
The LC Matching can further be divided into two networks which are:

- PI Matching Network
- Tee Matching Network
- L- Matching Network

4.5.1.2.1 PI Matching Network

The PI Matching network is mostly used to match high impedance devices to 50 Ohms and vice versa. In figure 4.5 three schemes of PI network is shown with a signal source having impedance R_G and a load with impedance R_L.

In figure 4.5(a) a low pass PI network is designed where an inductor is placed in series between two parallel capacitors. The second figure 4.5(b) shows a high pass PI network where a capacitor is placed in series between two parallel inductors. Another way of designing a PI network can be by placing two inductors in series, two capacitors in parallel to ground and virtual impedance between them as shown in figure 4.5(c).

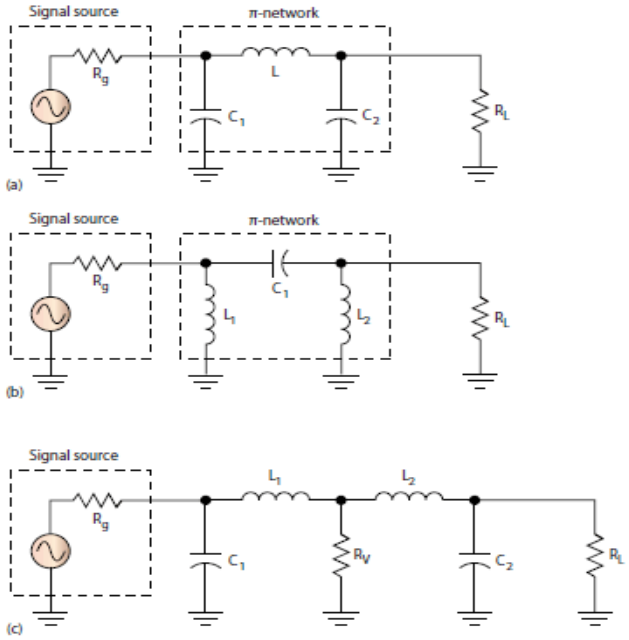


Figure 4.5 PI impedance matching network

4.5.1.2.2 Tee Matching Network

Two types of Tee Matching network is shown in figure 4.6(a) and 4.6(b). The first figure 4.6(a) is a high pass tee matching network where two capacitors are placed in series and an inductor grounded between them.

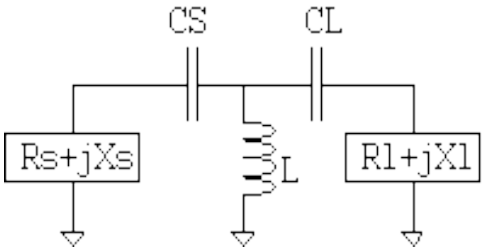


Figure 4.6(a) Tee matching network using two Capacitors and one Inductor

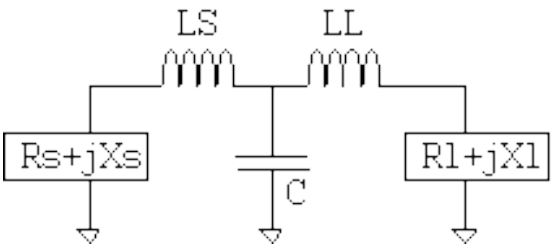


Figure 4.6(b) Tee Matching network using two Inductors and one capacitor

The second figure 4.6(b) is a low pass Tee matching network where two inductors are placed in series and a capacitor grounded between them. Since the sole purpose of these matching networks is to match the source and load impedance with the device used, the selection of either of these matching networks depends on the frequency of operation.

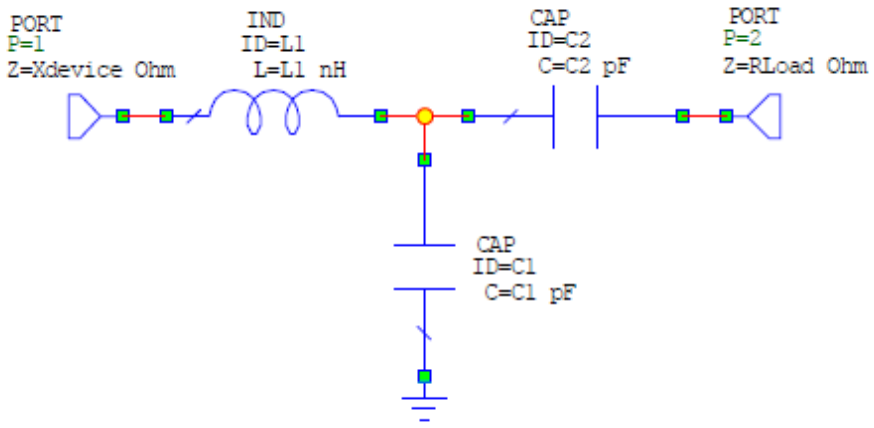


Figure 4.6(c) A simple Tee Matching Network

A band pass Tee matching network is shown figure 4.6(c). In this matching network two capacitors and an inductor is used and this matching network provides a band pass characteristic. The capacitors used can be tunable or fixed depending upon the requirement of circuit.

4.5.1.2.3 L – Matching Network

The fourth type of LC matching network is a band pass L-Matching network. The device manufacturers use this matching network as a test circuit. It contains a DC Block capacitor which allows the DC supply voltage to pass through it which is to be provided to the DUT (device under test) and prevent it from going towards the source or load. Usually the two capacitors are tunable which allows the circuit designer to match the impedance even after the fabrication process.

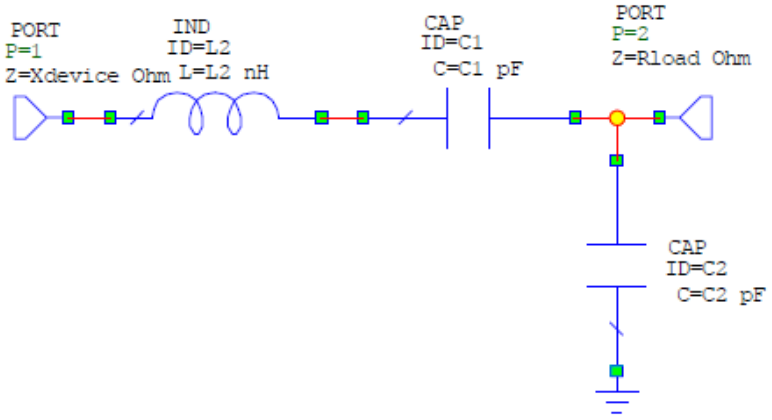


Figure 4.7 LC Band pass Impedance matching Network

4.5.1.3 Transmission Line Matching

The Transmission Line Matching uses transmission lines and stubs for impedance matching of DUT (device under test) with source and load. This type of matching network provides a wider bandwidth of impedance match as compared to LC matching network and can be used for frequency ranges above 150MHz. The downside of Transmission Line matching is that it is difficult to tune the matching network once it is fabricated.

The stubs used can be either a short circuit stub or an open circuit stub. Usually a short circuit stub is not used until compulsory because it reduces the output gain.

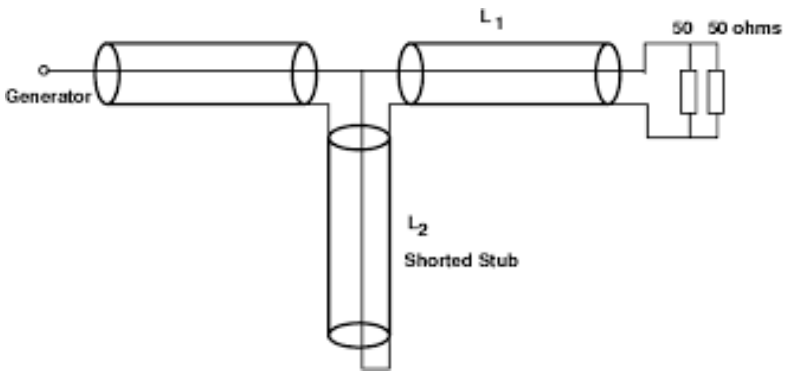


Figure 4.8 A Basic Transmission line Impedance Matching

Figure 4.8 shows a simple transmission line matching network together with a shorted stub. The transmission lines can be used either to match the impedance or just for allowing the two

components to be soldered on the circuit board. In figure 4.8 the transmission line near the generator is placed so that the input port can easily be soldered with the matching network without disturbing the matched impedance between the source and DUT (device under test). The transmission line L_1 and shorted stub L_2 are for the matching purpose.

Two important parameters of the transmission lines are the Length 'L' and width 'W'. The width defines the impedance of the transmission line while the length describes its angle. Both of these parameters highly depend upon the material, its height and the dielectric constant of the Printed circuit board and can vary widely for different PCB's. Mostly for Power amplifiers PCB with a height below 1mm and dielectric constant above value 3 is preferred for a good impedance match.

4.6 Design of Input and Output Impedance matching circuits on ADS Software

The next step in the design of a Power amplifier is the design of Input and output impedance matching circuits which help to match the impedance of transistor with the impedance of input and output ports of amplifier (which is usually 50 Ω). The S_{11} and S_{22} are used to define the source and load reflection coefficient (tau) $Γ_s$ and $Γ_L$. Figure 4.9 shows the schematic of s-parameter testing circuit.

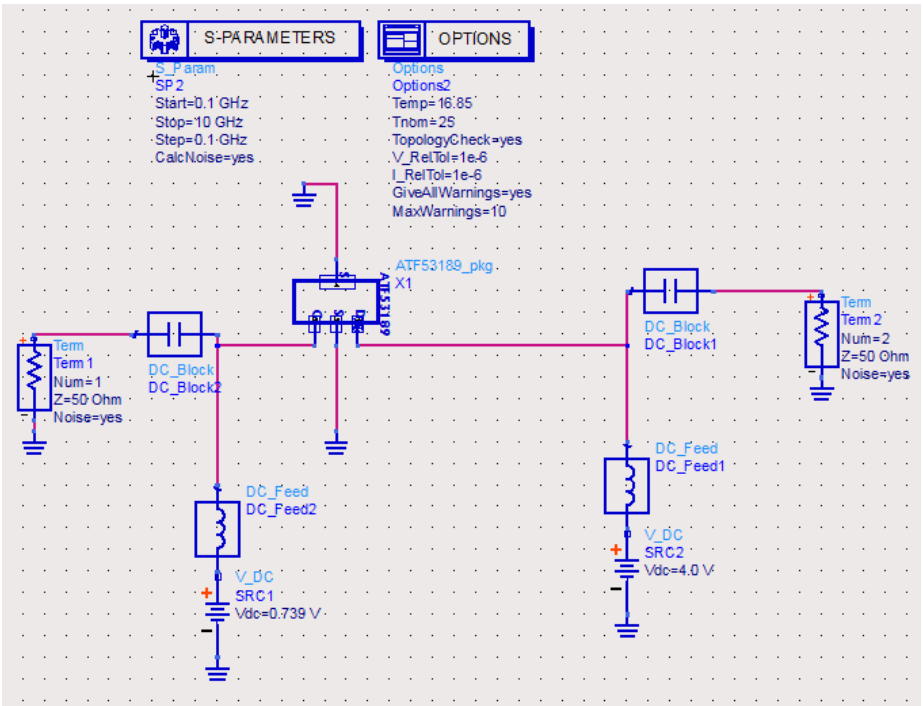


Figure 4.9 S-parameter testing circuit

This circuit is used to plot the S-parameters for our transistor ATF 53189 from the frequency range 0.1 GHz to 10 GHz and the plot is shown in shown in Figure 5.5. This plot shows that for 2.4 GHz frequency the value of S_{11} is 0.840/135.688 while the S_{22} is 0.499/145.145.

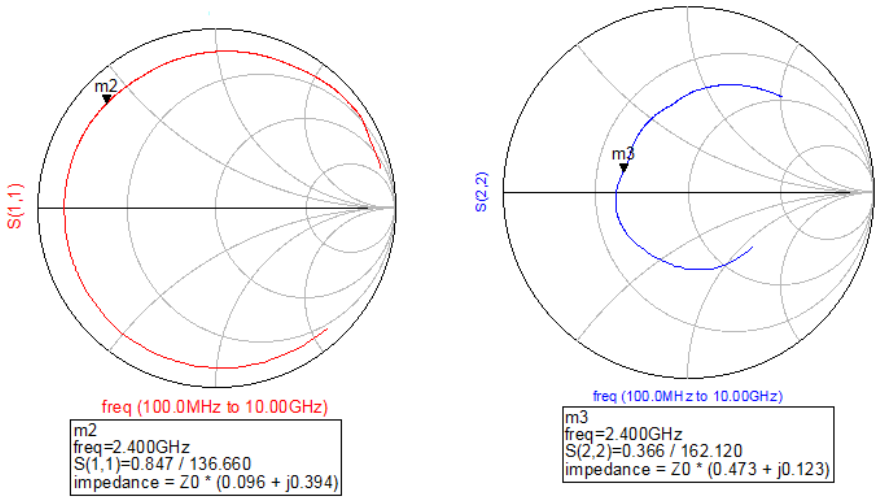


Figure 4.10 S_{11} and S_{22} values for 2.4 GHz frequency

These values of S-parameters are used to match the impedance across Gate and drain of transistor with the source and load of Power amplifier. The Smith chart tool in ADS helps to design the input and output impedance matching circuit by simply putting the values of S_{11} and $S2_{22}$ in this tool and match the impedance with 50Ω.

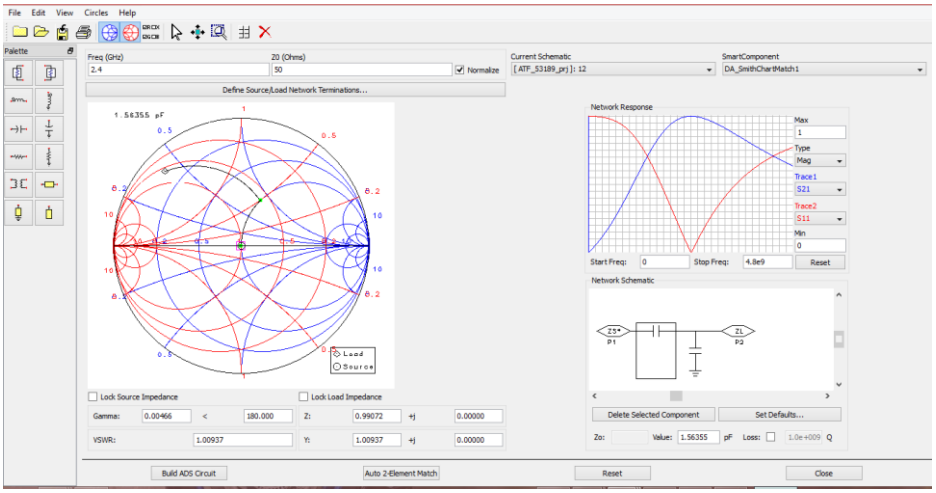


Figure 4.11 Smith chart tool for the design of impedance matching circuit

As can be seen in Figure 4.11 the values of S_{11} and S_{22} are put in the Smith chart tool which will define the proper values of Lumped components which will then be used in the power amplifier circuit for the impedance matching.

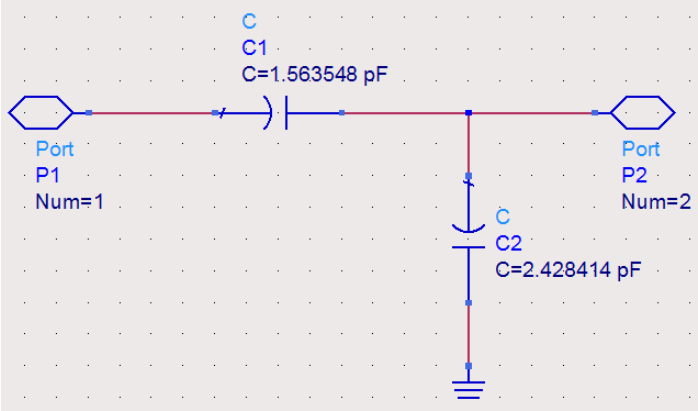


Figure 4.12 Input Impedance matching circuit

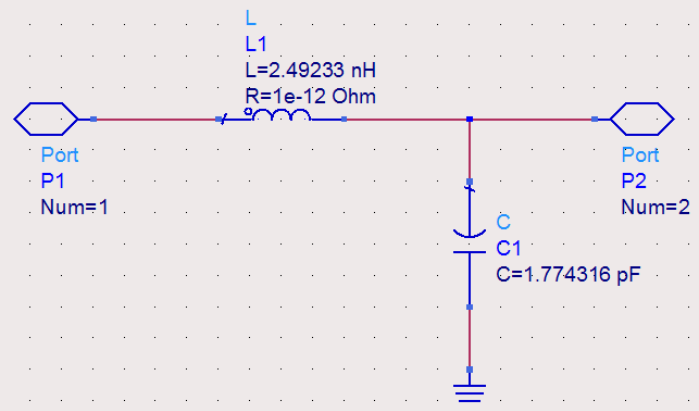


Figure 4.13 Output impedance matching circuit

Figure 4.12 and Figure 4.13 shows the input and output impedance matching circuit where the lumped components are used. These circuits will help in matching the input and output reflection coefficient (Tau) which in turn will increase the overall Gain of the Power amplifier.

4.7 Power amplifier circuit with input and output matching circuits

The power amplifier with input and output impedance matching circuit is shown in Figure 4.14. Biasing voltage V_{CC} is set to 4.2 volts while the three resistors R_1, R_2 and R_3 are calibrated previously in the biasing section. Two coupling capacitors C_1 and C_2 are used to

allow the AC signal to pass from AC source towards the transistor but to prevent any DC signal from entering the AC source and load. Three RF chokes L_1, L_2 and L_3 are used to allow the DC signal to enter the transistor but to block the AC signal from moving towards the DC source.

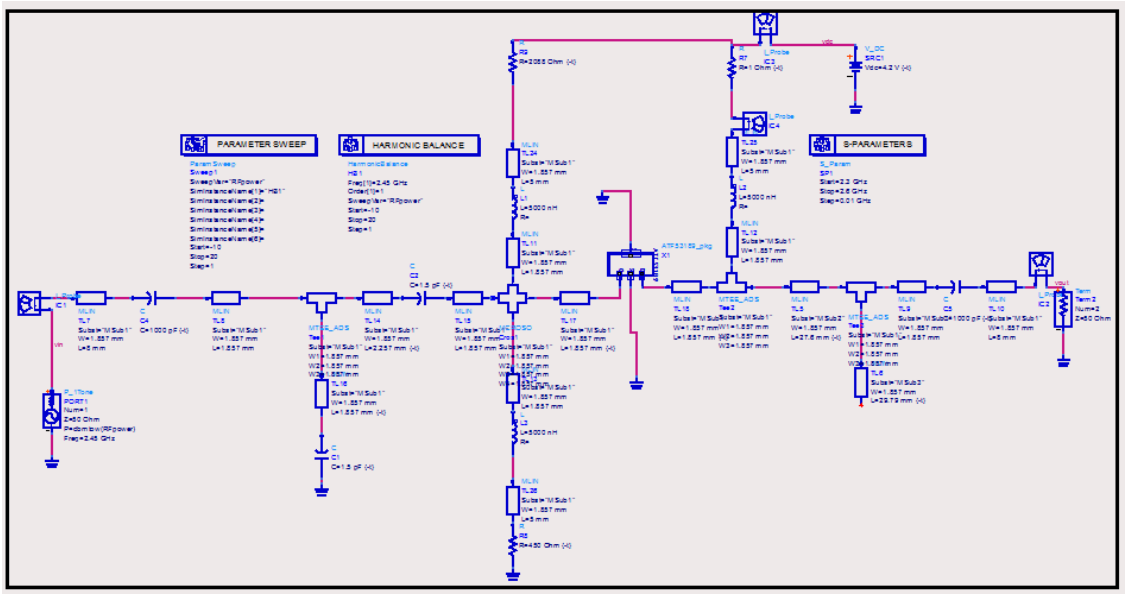


Figure 4.14 Schematic diagram of Power amplifier with input and output impedance matching circuit

After simulation the results are taken and it is shown in figure 4.15 where the gain S_{21} and PAE (power added efficiency) graph is plotted. From the given plot it can be seen that the gain of power amplifier is 18dBm while the PAE comes out to be 45%. Now to further increase the efficiency of this Power amplifier a technique is used which is the harmonic suppression circuit which will help to suppress the harmonic frequencies and reduce the power losses at those frequencies. This technique is discussed in the next section.

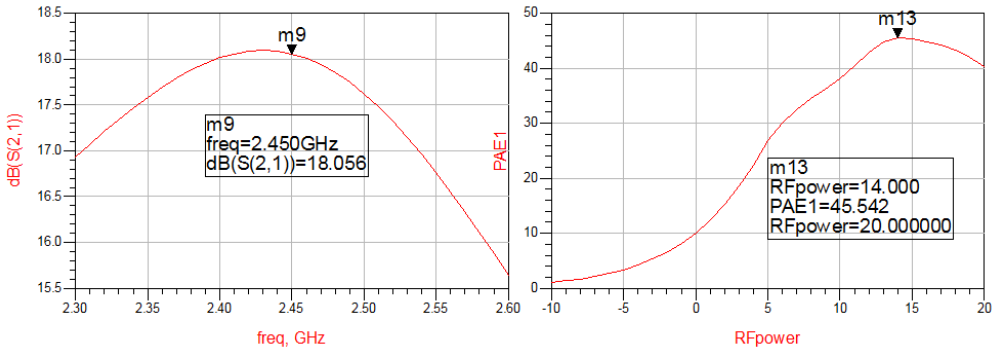


Figure 4.15 Plot of S_{21} and PAE for the proposed Power amplifier

4.8 Gain and Efficiency Enhancement Techniques

There are a lot of research and work done in order to improve and gain and efficiency of Power amplifiers. These techniques can be used on different classes of amplifiers depending upon the requirements. Three techniques will be discussed now which helps to improve and enhance the gain and efficiency of a Power amplifier.

4.8.1 Harmonic Suppression Technique

The harmonic suppression technique is used to increase the efficiency of a power amplifier. This technique helps to reduce the power which is being lost in the harmonic frequencies of the fundamental frequency. There are many methods which are used for the implementation of harmonic suppression [38] [39] [40] [41]. One of which is using a capacitor and inductor in series. This is the simplest way of designing a simple but efficient harmonic suppressor. A capacitor and an inductor together in cascade fashion is placed after the input impedance matching network at the gate of transistor. This kind of suppressor simply helps to filter out the unwanted harmonic frequencies and allows the desired fundamental frequency to pass towards the gate of transistor for amplification process [36].

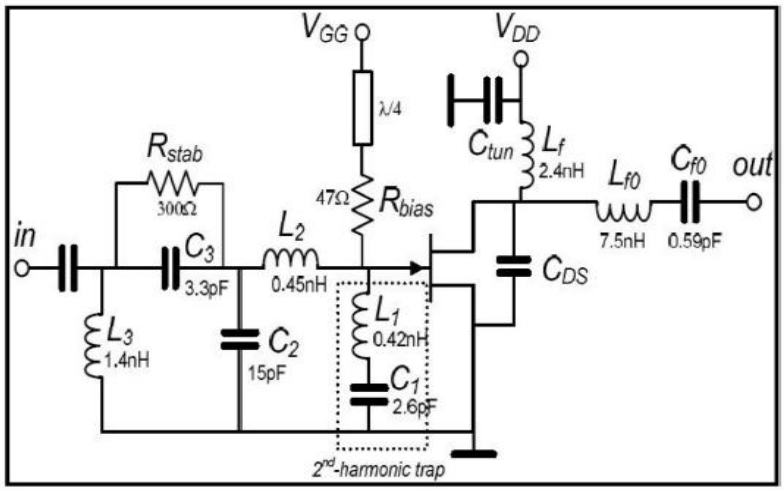


Figure 4.16 Basic schematic diagram of a harmonic trap circuit

In Figure 4.16 a simple harmonic trap circuit is shown which is used to suppress the unwanted harmonic frequencies. This is a Class-E topology so the gate of transistor needs switching square wave cycles in order to amplify the input signal. This harmonic trap circuit helps to filter the unwanted harmonic frequencies and allow only the fundamental frequency.

It also helps in shaping the input waveform to a square wave which will help in switching the gate of transistor by the input RF signal.

As can be noted from the Figure 4.16 the harmonic trap circuit is placed at 90 degrees to the input matching circuit and this technique helps to prevent the trap circuit from magnetic coupling. It also helps to reduce the bond wire inductance [37].

To get the maximum efficiency more than one harmonic suppressors could be implemented which will assure that only the fundamental frequency is allowed to pass towards the gate of transistor and this will eventually help in the enhancement of efficiency of Power amplifier. Figure 4.17 show another method in which two harmonic suppression circuits are placed at the input side of power amplifier. There are 2 capacitors and 2 inductors used in series which are tuned to the harmonic frequencies which are needed to be blocked and removed. When the input signal is applied at port 1 so after passing through the matching circuit the input RF signal reaches the harmonic suppression circuits which are tuned only for the harmonic frequencies which should be removed. So those frequencies which are harmonic to the fundamental frequency (2.4GHz in this case) are grounded through these harmonic suppression circuits as they appear open to them while the fundamental frequency is allowed to be passed towards the gate of transistor for amplification process.

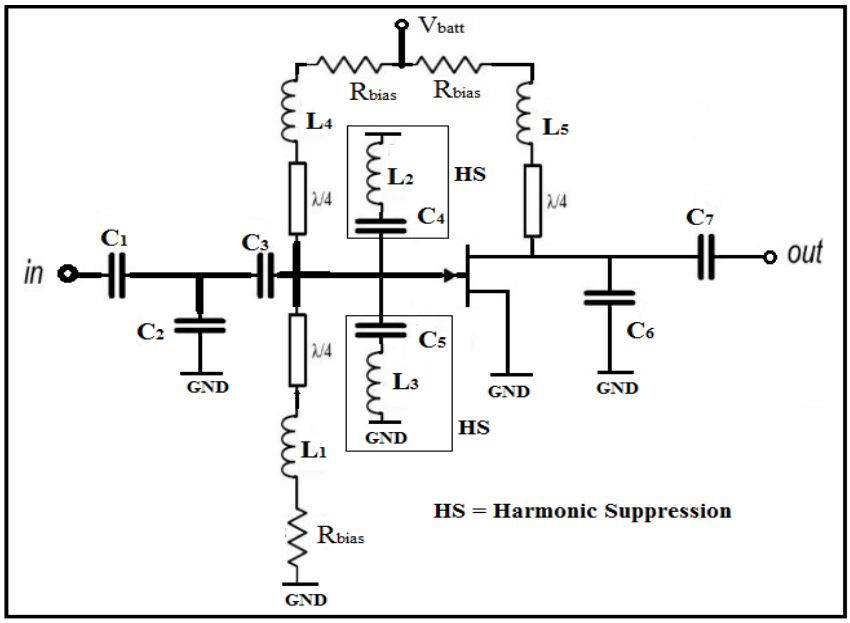


Figure 4.17 Implementation of 2-harmonic suppression circuits at the input side of Power amplifier

The harmonic suppression circuit can greatly affect the overall efficiency of any power amplifier. Depending upon the number of circuits used and its topology the increase in efficiency enhancement could range from (3% up to 30%). Other advantage of a harmonic suppression circuit is increase in gain of amplifier.

4.8.2 Cascade Topology Gain enhancement

Gain is one of the most important parameter of any power amplifier which defines its output power. For the design of any power amplifier a transistor usually provides the gain to the input signal by using the DC supply voltage. There is always a limit of any transistor up to which it can provide the maximum gain and for that the amplifier should be designed very precisely. Even more gain can be taken from a power amplifier by optimizing the input and output matching circuits. Without the use of input and output matching networks half of the gain is mostly lost due to impedance mismatch between the source, load and transistor itself and with mismatching standing waves are also produced which do not allow most of the input RF signal to enter the transistor for amplification. By properly optimizing the input and output impedance matching circuits the input RF signal could reach the transistor without producing standing waves.

A cascade topology helps to enhance the Gain of a power amplifier. Figure (4.18) shows a simple implementation of a cascade topology using two transistors M_1 and M_2.

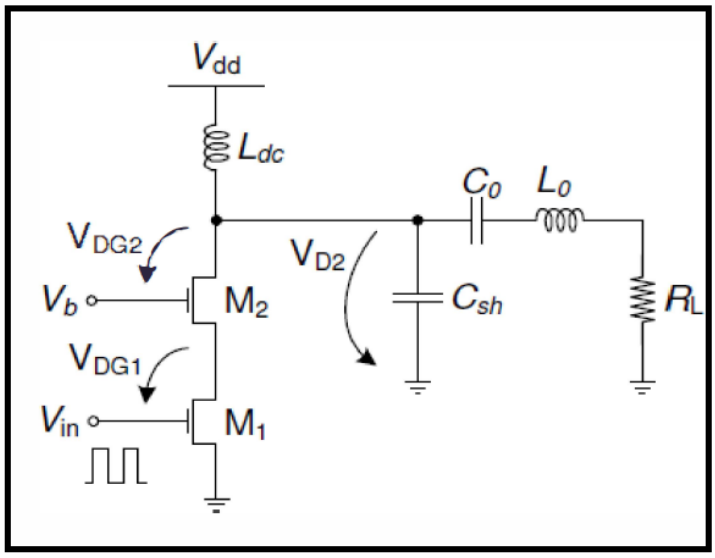


Figure 4.18 Circuit diagram of cascade topology gain enhancement technique

A cascade topology Class-E amplifier is shown in Figure 4.18. There are two transistors M_1 and M_2 connected in series and the input RF signal is provided to the gate of transistor M_1. This transistor simply acts as a switch and the input RF signal pulses helps to turn the transistor ON and OFF. Now for the signal to be transmitted from the drain of M_1 towards the source of M_2 the gate should also be provided enough voltage which is V_b. The reliability of this amplifier increases with the voltage swing within the drain-gate loop. The advantage of this cascade implementation is that Miller effect is decreased which helps in isolation and improvement of stability [42]. This topology also helps in optimization and tuning of linearity and noise removal independent of other parameters [43][44][45]. Furthermore since the transistor M_2 is not connected to the gate and drain terminal of the amplifier as compared with the M_1 transistor so improved isolation and stability is achieved. Assuming that both the transistors M_1 and M_2 have the same trans-conductance, the gain of the transistor M_1 would be almost unity since its input resistance is small.

4.8.3 Adaptive biasing Efficiency enhancement

Figure 4.19 shows the basic schematic of a 2-stage power amplifier which is divided into two main parts, the first is the power amplifier and the second is the adaptive bias circuit. The power amplifier stage is further divided into two stages which are driver stage and power stage.

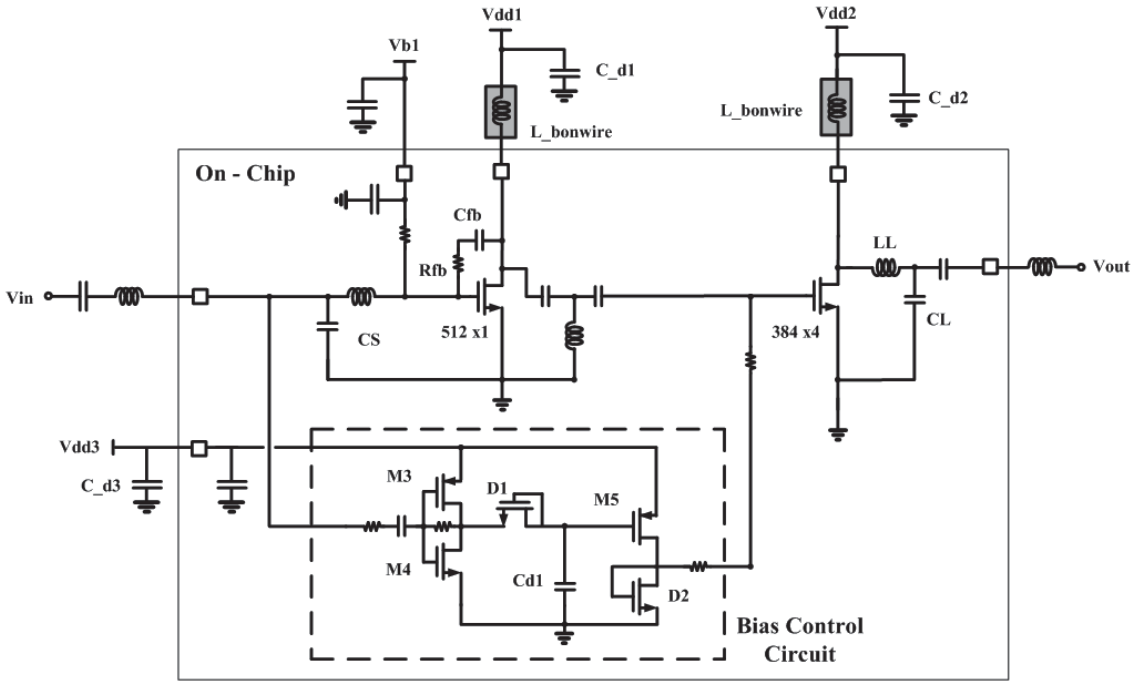


Figure 4.19 Basic schematic of adaptively biased 2-stage power amplifier

Usually a capacitor and a resistor is used in the feedback network which helps to improve the linearity of amplifier. Input and output impedance matching circuits are used to receive maximum gain from the amplifier. In the bias control circuit first the input signal is amplified by a self biased amplifier and then it fed to the power detector which controls the overall function of the bias control circuit. There are two transistors in the bias control circuit which are PMOS and NMOS transistors. At the output side of adaptive biasing circuit a PMOS transistor is used to provide DC power to the bias control circuit and also amplify the signal taken from the power stage of power amplifier. This helps to improve the nonlinearity behavior of main power amplifier built using NMOS transistors.

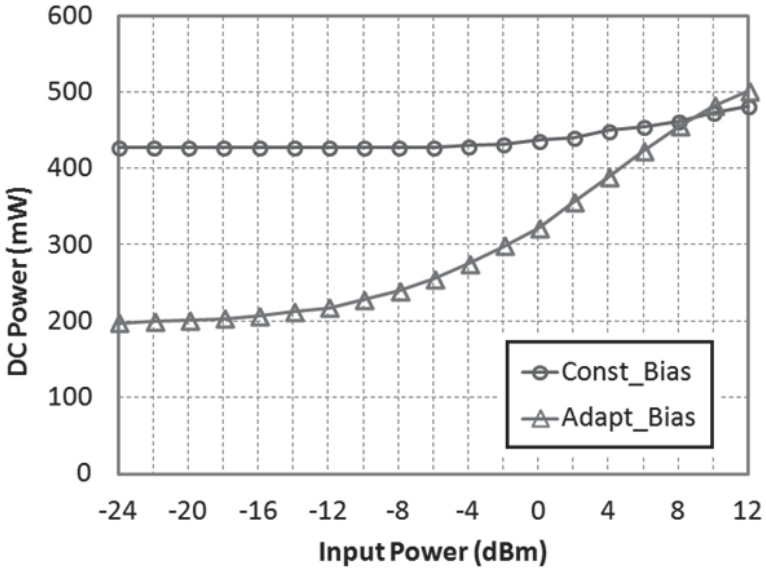


Figure 4.20 Comparison between a constant bias and Adaptive bias Power amplifier

An adaptive bias control circuit can really reduce the power consumption and help to improve the efficiency of a Power amplifier. Figure 4.20 shows the comparison of power consumption between power amplifiers with and without the adaptive bias circuits. As can be seen from the graph that the power consumption of a Power amplifier with adaptive bias circuit is almost half as compared to the other one [34]. This reduction in power consumption of Power amplifiers can extend the battery lifetime in power amplifiers of mobile devices. At low input RF power the battery usage is pretty low and since most of the time the input RF signal in any mobile device is low so this will help to improve the battery backup time [35].

4.9 Circuit simulation of the Proposed Power Amplifier

The simulation of proposed single stage power amplifier is presented in figure 4.22 below. A single transistor ATF-53189 is used in this design where the biasing voltage is set to 4v and 135mA, the input matching circuit is designed using capacitors C1 and C2 while the output matching circuit is designed using stub matching. The V_{CC} is set to be 4.2volts to provide the desired drain voltage and current to the transistor. After simulation the components are tuned to get the desired results and are shown in the simulated results section.

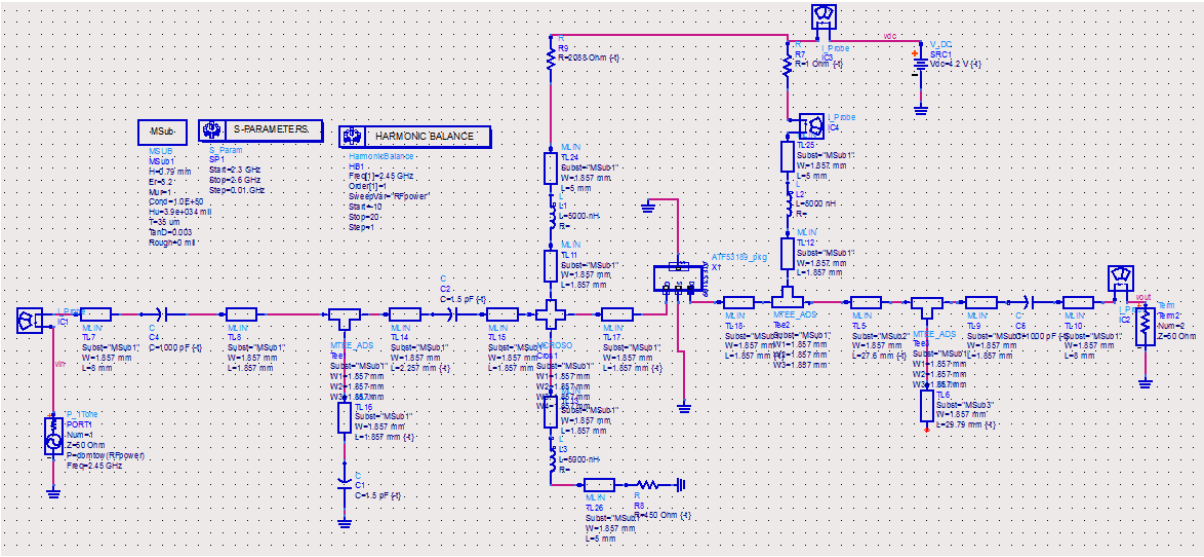


Figure 4.21 Schematic circuit of the proposed Power Amplifier

4.10 Implementation of Harmonic Suppression circuit and Co-simulation of the Proposed Amplifier

Figure 4.21 shows the complete Co-simulation diagram of the Proposed Power amplifier which includes the Biasing circuit, input-output impedance matching circuits and harmonic suppression circuits. Three resistors R_1, R_2 and R_3 are used to provide biasing voltage of 4 volts and 135mA current, these biasing values are taken from the data sheet of transistor ATF-53189 which is the optimum value for maximum gain from the amplifier. Capacitors C_1, C_2 and C_3 are being used for impedance matching together with transmission line. Two capacitors C4, C5 and two inductors L1 and L2 are used for designing the harmonic suppression circuit which is filtering out the unwanted harmonic frequencies. Supply Voltage V_{CC} of 4.2 volts is provided.

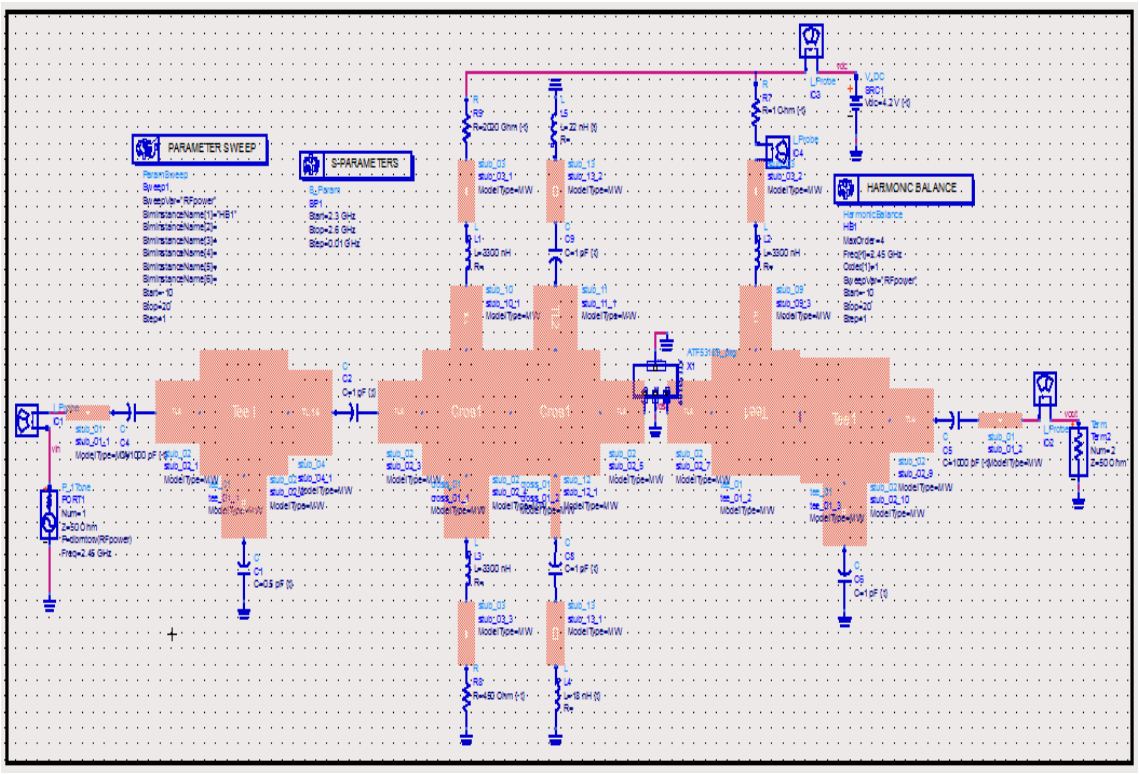


Figure 4.22 Co-simulation of the Proposed Amplifier with Harmonic Suppression circuit

4.11 Simulation design of the proposed two stages Power Amplifier

In the proposed 2-stage Power Amplifier the single stage Power amplifier is connected in cascade fashion as shown in Figure 4.22. The design of 2-stage Power amplifier is the same as was for the single stage, the only difference is the impedance matching circuit which is added between the two amplifiers while cascading. Resistors R7, R8 and R9 are the biasing resistors for the 1st stage while resistors R10, R11 and R12 are for 2nd stage of the 2-stage Power amplifier. Capacitor C2 and transmission line TL2 are the input impedance matching circuits while capacitor C14 and C11 are the output matching circuits. The impedance matching within the 1st stage and 2nd stage of the amplifier is achieved with the help of capacitor C17 and transmission line TL1. The capacitor C17 also helps to prevent any interference of 1st stage biasing voltage with the 2nd stage biasing circuit. Capacitors C4 and C11 are the coupling capacitors while inductors L1-L3 and L6-L8 are DC pass inductors to stop the AC signal from going towards DC power supply. Unwanted harmonics are filtered by inductors L4, L5, L9, L10 and capacitors C8, C9, C15 and C16. The Supply voltage V_{CC} is kept 4.2 volts as was for single stage power amplifier but its current consumption would be twice than single stage as there are two Power amplifiers cascaded. This power amplifier

design was targeted towards better output gain while compensating for little loss in efficiency.

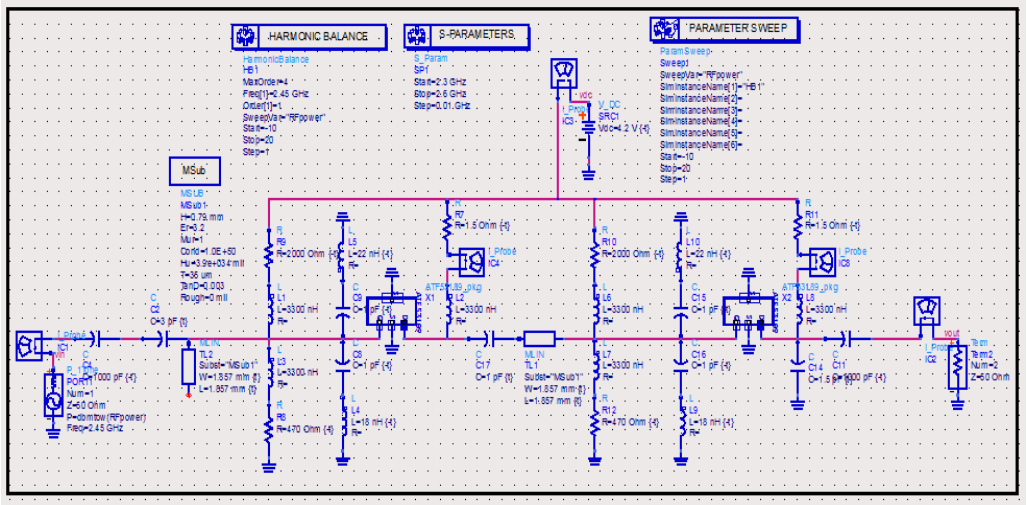


Figure 4.23 Simulation design of 2-stage Power amplifier

4.12 Co-simulation design of two stages Power Amplifier

The co-simulation of proposed two stages Power amplifier is shown in figure 4.24 below using two transistors ATF-53189 in cascaded fashion.

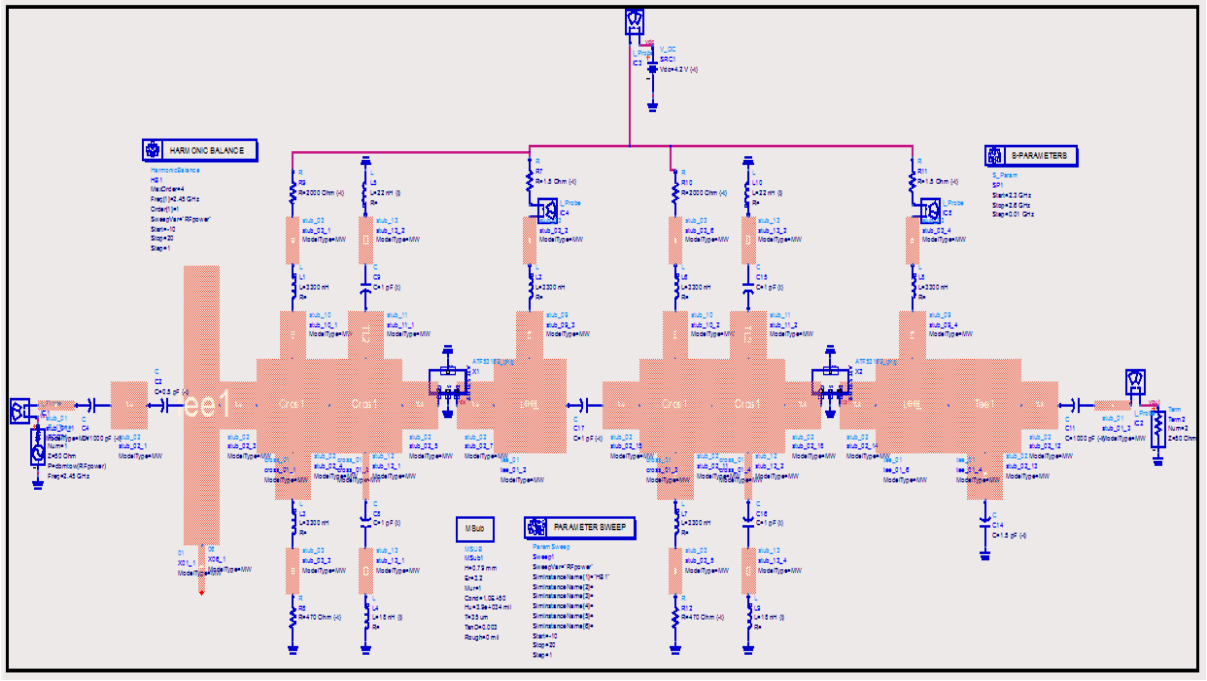


Figure 4.24 Co-Simulation of Proposed two-stage Power Amplifier

For optimizing and tuning the two-stage Power amplifier first the schematic diagram is moved for co-simulation which is shown in Figure 4.23 and then it is simulated to get the Optimized results, next step is the tuning where different components are selected for tuning and while changing the values of lumped components results are improved. In our design the input-output matching circuits and DC blocking inductors are tuned to get maximum Gain from this 2-stage Power amplifier.

4.14 Fabricated Design

The Single stage and 2-stage Power amplifiers are fabricated on Taconic PCB with dielectric constant value of 3.2 and thickness of 0.79mm as shown in figures 4.26 and 4.27 respectively.

The single stage Power amplifier has the dimensions of 4.6cm x 3.4cm. A single transistor ATF-53189 is located at the centre of the circuit. The capacitors used have the dimensions according to the standard of 0805, while the inductors are according to the standard of 1206. The Grounding of transistor is directly done using thin wires with the lower side of the PCB as it affects the Gain of the amplifier.

In case of two stage Power amplifier, the dimensions are 5.9cm x 3.6cm. Two transistors are placed in cascade fashion, the capacitors and inductors are according to the standards as previously mentioned.

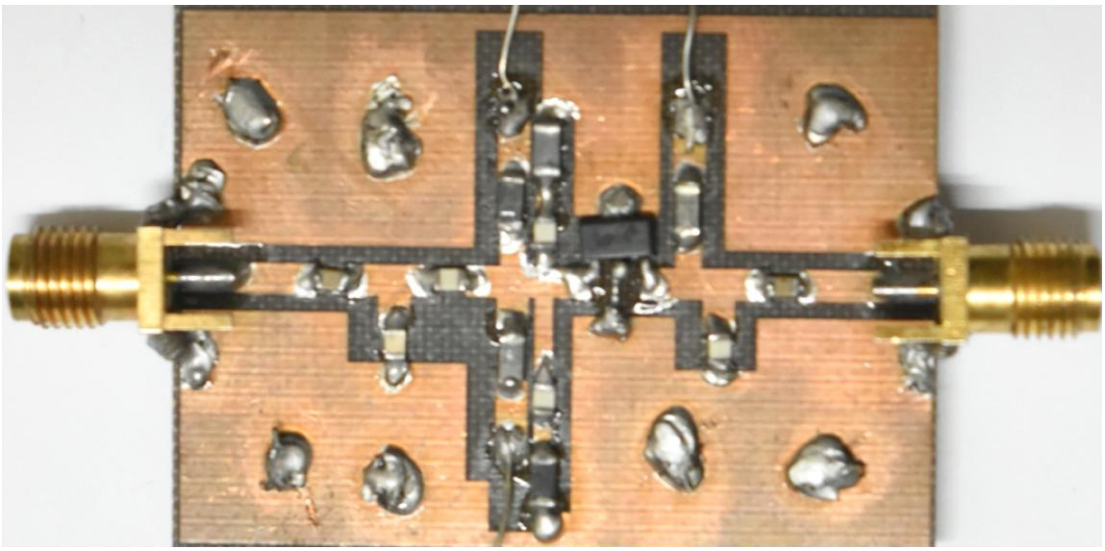


Figure 4.25 Fabricated design of Single stage Power Amplifier
Dimensions = 4.6 cm x 3.4 cm

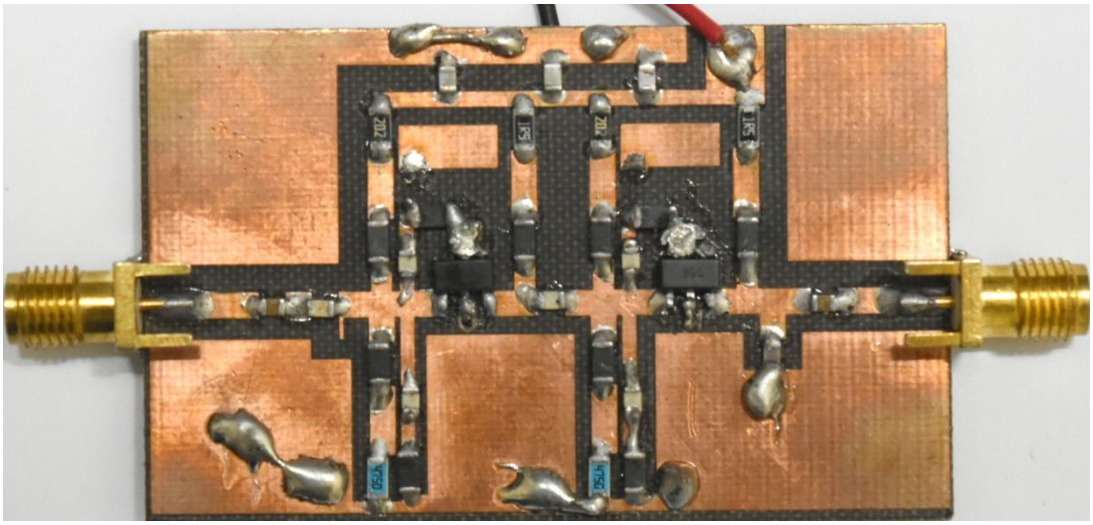


Figure 4.26 Fabricated Design of Proposed 2-stages Power Amplifier
Dimensions = 5.9 cm x 3.6 cm

Chapter 5

Design of CMOS Power Amplifier

5.1 Introduction

Designing PAs is often considered a very special field distinctive from other RF block designs because of the lack of well characterized models for large signal operations and high voltage and current stress. Thus, designers often rely more on their experience than simulation results when they characterize PAs. Moreover, guaranteeing a reliable operation is as important as achieving good performances such as high output power, high efficiency, and high linearity. In addition to these design difficulties of general PAs, a CMOS PAs are even harder to design. While CMOS technology is welcomed because of its cost-effective material and great versatility, as mentioned in Chapter I, the commercialization of CMOS PAs has not been easily achieved due to the intrinsic drawbacks of standard CMOS processes from RF perspectives: a low-quality factor (Q), the lossy substrate of passive structures, low breakdown voltage, and low transconductance of active devices. Thus, many efforts, including the development of high power generation techniques, linearity enhancement techniques, and efficiency enhancement techniques, have focused on overcoming the drawbacks of CMOS technology for PA designs. Thus, Section 5.2, introduces the structure and the difficulties of designing PAs. Section 5.3 follows with a discussion of the challenges of CMOS technology in the design of PAs. In response to the challenges outlined in the previous sections, Section 5.4 introduces several state-of-art performance enhancement techniques for CMOS PAs.

5.2 General Issues in Designing RF Power Amplifiers

As shown in Figure 5.1, a PA consists of four important blocks: an active block that consists of power cells and three passive blocks that comprise bias feeding for the DC current, power combiners, and impedance transformers. Since the passive blocks usually contain inductive characteristics, they can be combined functionally.

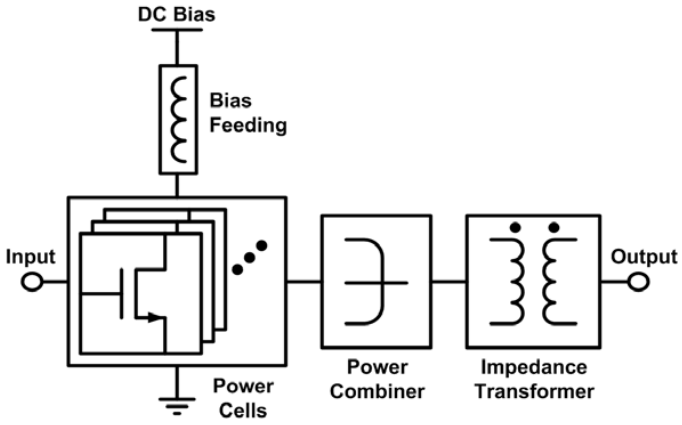


Figure 5.1 **Block diagram of the PA output network**

In the bias feeding for the DC current, minimizing the voltage drop is a key factor to keeping the drain voltage as high as possible. PAs typically consume high current, around a few amperes, so even a small series resistance of the bias feeding line can severely deteriorate efficiency. Fully-integrated PAs, the bias feeding line can be implemented in two ways. One is to use bond wires, well known for their high Q [2] of around 40 to 50 for cellular bands; however, they are subject to inductance variations. The other is to use an integrated inductor that consumes a large area and normally has low Q of less than 30, a best guess by the author.

An impedance transformer is also a key block to determining the amount of power to be transferred from the power device to the load. Even though it draws a large current from the power cells for high output power, the transformed load impedance at the input of the output network turns out to be as small as a few ohms [16]. Since the parasitic resistance of the output network, caused by resistive loss, the skin effect, and the proximity effect [17], occurs together with the transformed load impedance, a portion of power is consumed during this parasitic resistance. Hence, a high Q impedance transformer is preferred if power loss is to be minimized.

Last, when the required output power is higher than the power that a single PA can provide, a power combiner that guarantees output power specifications becomes essential. Since typical power combiners lead to an increase in power loss as the structure becomes more and more complex, the misuse of power combining consumes a large die area and even degrades performance. Therefore, this method of meeting power requirements should be a last resort.

In the design of PAs, a lossy output network is detrimental to achieving high output power, efficiency, and linearity, all crucial characteristics of PAs for wireless applications; thus, output networks require special attention. Output networks have been successfully

implemented using conventional techniques such as high-Q off-chip components [18, 19] and integrated patterns onto low-loss substrates (e.g., low-temperature co-fired ceramics) (LTCC) [20]. Nonetheless, such a modular design requires additional cost. Furthermore, because PAs are extremely sensitive to output networks, the use of semiconductor processes is preferred as they have better tolerance and repeatability [6].

5.3 Challenges of CMOS Technology for RF Power Amplifiers

The challenges mentioned in this section originate from the devices and process characteristics of CMOS field effect transistors (FETs). While such devices are used for other purposes such as digital and small signal RF circuits, if the aim is to design PAs, these characteristics pose serious challenges to PA designers. Before developing performance enhanced PAs, designers must possess a thorough understanding of the issues that will lead to better designs.

5.3.1 Lossy Substrate and Thin Top Metal of Bulk CMOS

As mentioned in Section 5.2, power loss caused by passive structures in a PA layout must be minimized. Figure 5.2 shows the loss mechanism of inductive structures in bulk silicon (Si) CMOS technologies. On top of a low resistance substrate, dielectric layers are stacked vertically and metal traces are formed within the dielectric layers. When current conduction flows through the metal traces that have series resistance and inductance with parasitic capacitance with neighboring traces, ohmic loss by the resistance affects the quality factor of the metal traces. At the same time, the induced magnetic field penetrates the dielectric and substrate layers. Since most materials, except certain magnetic materials rarely used in semiconductor processes, have the permeability constant value of unity, the magnetic field naturally makes a closed loop not bothered by any layers in the figure. The field can cause eddy current flow for a low resistive substrate. The substrate conduction current can also flow through the parasitic capacitance in-between the metal traces and the substrate, leading to additional loss. Thus, maximizing the quality factor by reducing eddy currents [21] and minimizing parasitic capacitance [8] are the main design goals of an inductive passive component in CMOS.

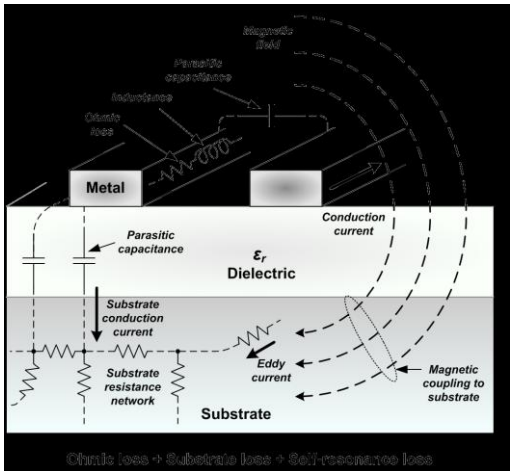


Figure 5.2 **Loss mechanisms of inductive structures in CMOS technologies**

The quality factor of an inductive structure is defined as [22]

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}} \tag{5.1}$$

$$= \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one ocsillation cycle}} \tag{5.2}$$

As represented in Equations (5.1) and (5.2), the definition can be further categorized according to three primary mechanisms: the ratio of magnetic energy storage capacity to energy loss (the ohmic loss in the series resistance), substrate loss dissipated in the silicon substrate, and the self-resonance factor by the parasitic capacitance [6, 22] in Figure 5.2. In a more analytical description, a single-ended spiral inductor can be modeled as illustrated in Figure 5.3(a), in which $RRss$ and $LLss$ represent the series resistance and inductance, respectively. $CCss$ is the interwinding parasitic capacitance, and $CCoooo$is the oxide capacitance on top of the substrate resistance and capacitance, $RRSSSS$ and $CCSSSS$, respectively.

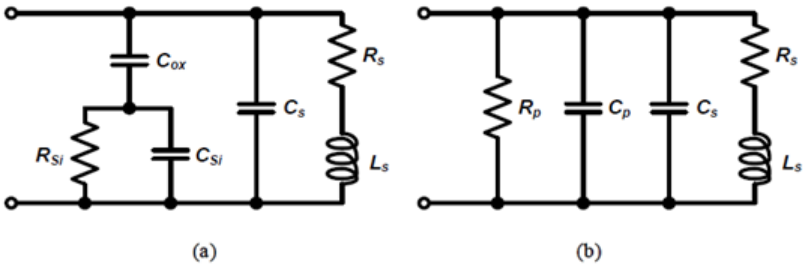


Figure 5.3 **Lumped model of a spiral inductor on silicon: (a) physical model and (b) simplified equivalent model**

In the simplified equivalent model in Figure 5.3(b), $RRpp$ and $CCpp$ can be derived as

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{Si}} + \frac{R_{Si}(C_{ox} + C_{Si})^2}{C_{ox}^2} \quad (5.3)$$

$$C_p = C_{ox} \cdot \frac{1 + \omega^2 (C_{ox} + C_{Si}) C_{Si} R_{Si}^2}{1 + \omega^2 (C_{ox} + C_{Si})^2 R_{Si}^2} \quad (5.4)$$

The quality factor of the inductor can be derived again as follows [22]:

$$Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + \left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right] R_s} \cdot \left[1 - \frac{R_s^2 (C_s + C_p)}{L_s} - \omega^2 L_s (C_s + C_p)\right] \quad (5.5)$$

Ohmic loss factor · substrate loss factor · self-resonance factor (5.6)

Ohmic loss stems from the quality of the metal, reflected in its conductance, width, and thickness. The design parameters that control the quality factor of an inductor are the width and the thickness for $RRss$, and the distance from the substrate to the metal layer. The reason for the series resistance is twofold: the DC metal resistance for low frequency and the skin effect for high frequency [8]. The physical cause of the skin effect is the eddy current induced by a magnetic field. While an AC current flows through the inductor trace, the eddy current redistributes the total current, and most charges are spelled from the center of the metal traces, increasing the series resistance of the inductor. This is called “skin depth” with the following relation,

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \quad (5.7)$$

$$R_{skin} = \sqrt{\frac{\omega\rho\mu}{2}} \quad (5.8)$$

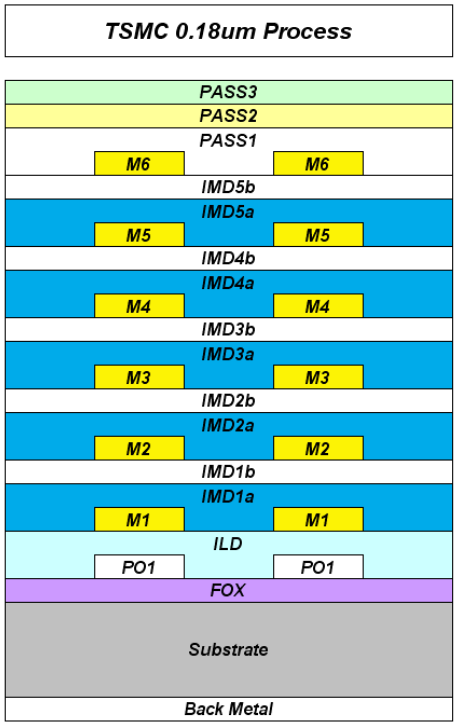
where $\delta\delta$ (m) is the skin depth, $\rho\rho$ (C/m3) is charge density, and $\mu\mu$(H/m) is the permeability. To reduce the ohmic loss by the skin effect, the thickness, the width, and the conductivity of the metal traces should be controlled so that it has low series resistance. In a spiral structure, the currents of neighboring metal traces in an equivalent phase expel each other, rendering the current distribution more complex. This phenomenon is referred to as the “proximity effect,” which is also caused by magnetic flux through the metal traces.

The substrate of CMOS technologies also has finite resistance causing dissipation by the substrate resistance. The parasitic capacitance causes the current through the metal trace of the inductor to leak out along the electric field. To suppress parasitic capacitance, the distance from the substrate to the metal traces should be sufficiently far, but in CMOS technologies, the distance is not controllable. Although techniques such as patterned ground shielding (PGS) can be used to reduce substrate loss, they come at the cost of low self-resonance frequency. Often, PGS is believed to reduce the magnetic coupling to the substrate resistance, but it has little effect [8, 22]. If the substrate resistance were either infinite or zero, no substrate loss would occur and a high quality factor could be expected [8].

While a purely magnetic component can store only magnetic energy, parasitic capacitances store electric energy, and when two energies are equal, self-resonance occurs. This is the point in which the magnetic energy of the inductor is converted to purely electric energy, so the behavior of the inductor resembles a capacitor. To avoid such an effect, the substrate under an inductor or transformer layout is blocked from doping or limited to light doping.

In dedicated RF processes such as the GaAs HBT process, substrate resistivity is higher than 10,000 Ohm·cm (=0.01 S/m); that is, it is virtually an insulator, and the loss in the substrate is low because substrate leakage and the eddy current are suppressed [21]. However, standard CMOS processes are built on a bulk silicon substrate, which has a low substrate resistivity, or high substrate conductivity, of less than 10 Ohm·cm (10 S/m).

Figure 5.4 provides an example of standard CMOS layer information. In this example, 1 poly 6 metal layers are shown, and the substrate has a conductivity of 12.5 S/m (8 Ohm·cm) and the top metal thickness is 2.34 μm. The quality factor has a direct relationship to the metal thickness. A thin top metal that is less than 3 μm provides only a low quality factor far less than 10 for passive designs. If an on-chip inductor is used for matching, this low quality inductor can cause power loss.



TSMC 0.18um Layer

Dielectric Layer	Dielectric Thickness	Er	Conductivity	tan
	um		S/m	
PASS3	0.6	7.9		0.03
PASS2	0.15	4.2		0.03
PASS1	2.5	4.2		0.03
IMD5b	0.35	4.2		0.03
IMD5a	1.18	3.7		0.03
IMD4b	0.2	4.2		0.03
IMD4a	1.18	3.7		0.03
IMD3b	0.2	4.2		0.03
IMD3a	1.18	3.7		0.03
IMD2b	0.2	4.2		0.03
IMD2a	1.18	3.7		0.03
IMD1b	0.2	4.2		0.03
IMD1a	1.18	3.7		0.03
ILD	0.75	4		0.03
FOX	0.35	3.9		0.03
Substrate	250 (10mil)	11.9	12.5	0.03

Metal Layer	Metal Thickness	Conductivity
	um	S/m
M6	2.34	2.40E+07
M5	0.53	2.40E+07
M4	0.53	2.40E+07
M3	0.53	2.40E+07
M2	0.53	2.40E+07
M1	0.53	2.40E+07
PO1	0.2	
BM	10	PEC

Figure 5.4 **Layer information of a standard CMOS process**

To contain the magnetic field above the substrate, various methods have been developed. The most popular is to add a PGS on the M1 layer or on the PO1 layer in Figure 5.4 with slots perpendicular to the direction of the eddy current, but with increased parasitic coupling to the substrate [21]. However, the misuse of this technique often leads to an inferior quality factor. The loss mechanism of inductive structures in CMOS technologies is summarized in Table 5.1, which also lists some simple approaches overcoming the loss mechanisms.

Loss Factor	Cause	Techniques
Ohmic loss	• DC resistance • Skin effect • Proximity effect	• High conductivity metal traces • Thick and wide metal traces
Substrate loss	• Capacitive coupling • Magnetic coupling	• High substrate resistance • Long distance from substrate to metal traces
Self-resonance loss	• Parasitic capacitance	• Low parasitic layout • Long distance from substrate to metal traces

Table 5.1 **Loss mechanism of inductive structures in CMOS technologies**

If a PA is integrated into a transceiver, the large signal coupling to the substrate can corrupt the operation of neighboring transistors, illustrated in Figure 5.5. The large signal swing at the drain of the center transistor is coupled through the junction capacitance of the drain-body diode to the substrate, and the resistor-diode (or capacitance) network is undesirably modulated. Substrate coupling affects sensitive blocks, especially the low-noise amplifier (LNA), which is very susceptible to noise. Toward the ultimate goal of designing a fully-integrated transceiver, isolation techniques should be properly applied between the PA and other blocks. From a circuit perspective, differential topologies can consume an AC current swing within the circuit itself and minimize the injection of stray electrons and holes into the substrate. The other way is to make guard-rings a more intuitive and direct method of cutting off the leakage itself, but at the cost of a large signal routing area.

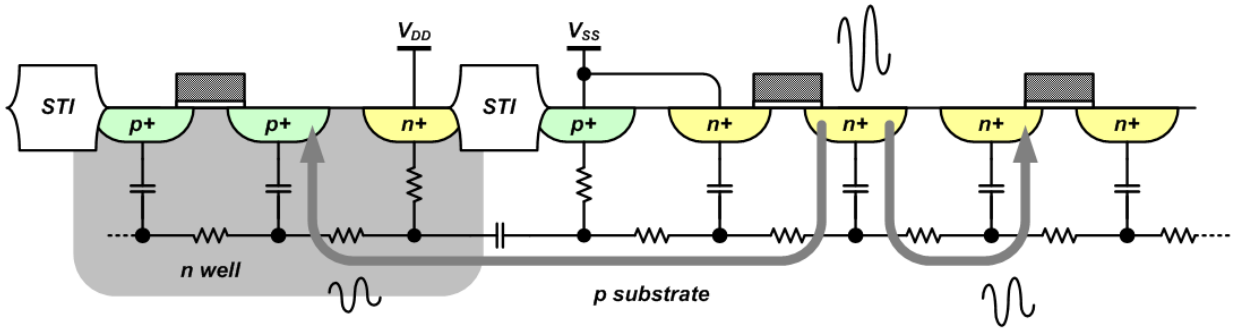


Figure 5.5 **Substrate coupling of a CMOS process**

5.3.2 Reliability of Bulk CMOS

Since PAs deal with a large output power, the reliable operation range is often violated in the design of CMOS PAs. CMOS devices in PAs are under high stress, causing a breakdown of devices in extreme cases. The breakdown mechanism of field effect transistors (FETs) can be categorized as shown in Table 5.2 [23]. Among them, hot carrier effects and oxide breakdown are destructive while junction breakdown and punch-through effects are recoverable when stress conditions are removed. The breakdown mechanisms caused by a large signal swing between the drain and the source or between the drain and the gate are junction breakdown and oxide breakdown, respectively. Although junction breakdown is recoverable, oxide breakdown permanently damages transistors. Thus, preventive measures must be taken in PA designs. Whereas GaAs hetero-junction bipolar transistors (HBTs), which constitutes a dedicated RF process, have high breakdown voltage sustaining up to 20 V, CMOS transistors endure only up to twice the supply voltage [2], which barely meets the supply voltage of cellular terminals

Breakdown	Cause	Effect	Damage
Junction (Avalanche) Breakdown	• Increase in the drain-source voltage cause excess voltage for the drain-substrate pn-junction • The drain to body diode is operated in the reverse breakdown area • Impact ionization	Abrupt increase in the drain current	Not inherently destructive
Punch-trough	• Punch-through of the drain depletion region to the source depletion region	Gradual increase in the drain current	Not inherently destructive
Hot Carriers	• Injection of electrons and holes into the oxide region with sufficient horizontal or vertical electric fields • Increase in the gate current and carrier trapping	Turn-On of transistor with trun-OFF conditions	Destructive
Oxide breakdown	• Strong vertical electric field due to excessive gate voltages	Gate leakage current	Destructive

Table 5.2 **Breakdown mechanism of FETs**

Several efforts have been made to overcome the low breakdown voltage of the CMOS process. One way is to make a thicker gate oxide that bolsters the high gate bias voltage. However, this approach requires process revision and is cost prohibitive. Thus, simple circuit techniques are preferable in a standard CMOS process. For instance, the vertical stacking of devices can reduce the burden on each transistor as long as the number of stacks is large enough to distribute the voltage stress [18].

In addition to the voltage stress of transistors, PAs also suffer from high current driving. A large current swing through passive structures can cause a gradual increase in metal resistance in a long-term operation and the Joule heating effect in a short-term operation ending in the melting of metal lines. These problems call for some guidelines that will guarantee a reliable operation. While the rule of thumb value, 1 mA/μm, is often suggested, a more rigorous criterion that affords such a guarantee should be used for each process.

5.3.3 Low Transconductance of Bulk CMOS

The current for forward bias and the transconductance of a CMOS device can be expressed [23] as

$$I = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2, \tag{5.9}$$

$$g_m = \mu C_{ox}\frac{W}{L}(V_{GS} - V_t), \tag{5.10}$$

respectively, in which all symbols follow the conventional MOSFET parameters of [23]. Then, the ratio of the transconductance to the current is expressed as

$$\frac{g_m}{I} = \frac{2}{V_{GS} - V_t}, \tag{5.11}$$

while the transconductance of a bipolar junction transistor (BJT) shows a relation of

$$\frac{g_m}{I} = \frac{q}{kT}. \tag{5.12}$$

For example, by simply comparing the ratios of both the MOSFET and the BJT at room temperature, the BJTs have a higher value of $qq/\ kkkk$~ 1/26 mV, while a typical MOSFET shows 2/($VVGGGG-VVtt$) ~ 1/50 mV with $VVGGGG$= 600 mV and $VVtt$ = 500 mV. In other words, BJTs usually have a higher transconductance ratio per given current through the output by one order of magnitude.

Thus, obtaining both a high gain and a high output current in the CMOS process requires large power cells and strong driving power from previous stages. However, neither way is desirable in a PA design, and PAs that use BJTs are generally considered more efficient at output power generation.

5.3.4 Nonlinearity of Bulk CMOS

In the design of a linear PA using a standard CMOS process, the first step is to understand the limitations of the given process. Figure 5.6 shows the equivalent circuit model of a standard RF NMOS transistor. In addition to the transconductance provided by the MOS transistor (based on the BSIM3 model with turned-off junction diodes), other resistances, capacitances, and junction diodes can represent the RF behavior of the transistor. Such ever-present parasitic capacitances and junction diodes distort the AC signal applied to terminals and cause distortion, imposing serious constraints on their anticipated performance [2]. If such

distortions are not efficiently suppressed at the device or circuit level, then the PA designed using such a device can cause nonlinear circuit operation.

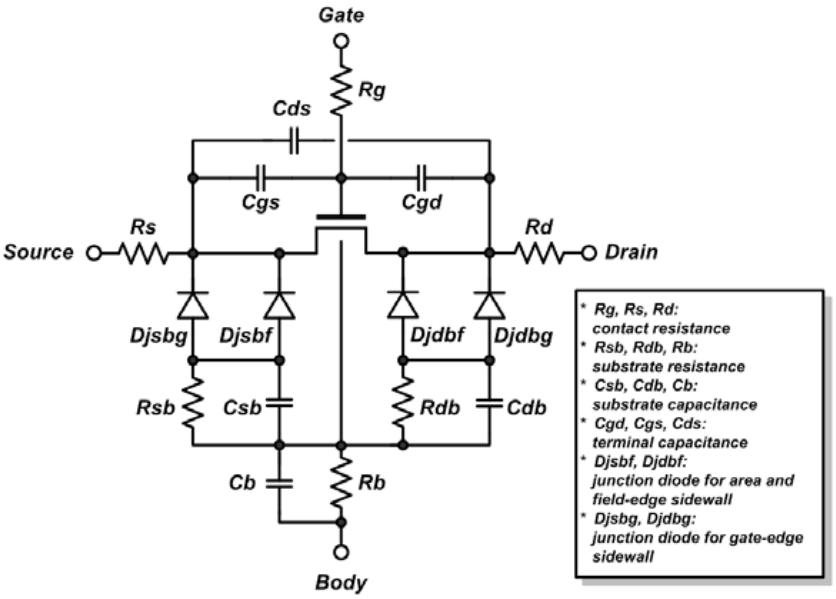


Figure 5.6 **Equivalent circuit model for RF NMOS transistor**

Researchers have devoted their efforts analyzing the effects of the components on linearity and the factors responsible for nonlinearity [24]. It is claimed that the factors responsible for the nonlinearity of a device are gate-source capacitance, gate-source transconductance, gate-drain transconductance, and drain-body junction diodes, listed in order of most to least dominant.[25, 26]. However, analyses, which are limited to a small-signal range and ignore the large-signal swing in PA operation, have led to disagreement, requiring further investigation that leads to the generalization of the ideas.

In summary, CMOS processes have inherent problems such as poor reliability and linearity, and poor passive and active performances in RF CMOS PA designs. Thus, before undertaking the next step of developing proper measures for handling the large-signal operation of PAs, we must first understand the challenges that such a task entails.

5.4 Techniques for CMOS RF Power Amplifiers

As introduced in Section 5.3, CMOS devices have low power capability compared to compound semiconductor devices. Due to the low Q of on-chip inductors in CMOS processes, off-chip matching networks have been the dominant methods for completing the PA functions. One breakthrough in the effort to achieve the integration of an entire PA came in the form of the design of an efficient power-combining method using transformers in series

[16, 27]. Although this design represented proof of the feasibility of achieving high output power from CMOS processes, because of its bulky size and instability, further effort is required to gain the same output power capability using alternative methods [28]. Since the initial efforts focused only on power capability, the linearity performance was poor, marring the progress toward linear applications. Only through the broadening of the understanding of CMOS nonlinearities can any approach that eliminates nonlinear factors in CMOS devices be established. Upon until now, however, only a few noticeable findings have been reported [24, 26, 29]. Despite such efforts, system concepts are also being applied to implement a PA in which linearity or efficiency enhancement is realized using more complex signal manipulation [30-33].

5.4.1 Output Power-Combining Techniques

In wireless applications, output power usually reaches watt levels. For example, most PA products for GSM applications generate more than two watts. Hence, CMOS processes, known for low power-driving capabilities, necessitate an additional function, i.e. a power combiner, that combines several unit power cells that generate the required output power. Figure 5.7 depicts several popular power-combining techniques. The LC matching and combining network is popular but not suitable for IC integration due to its bulky size and narrowband characteristics. The Wilkinson combiner is also a popular method, especially for high frequency or off-chip implementation, but its bulky quarter-wave transmission lines thwart implementation efforts in cellular applications. Compared to the above techniques, the transformer provides differential combining in a compact form factor with a broadband advantage.

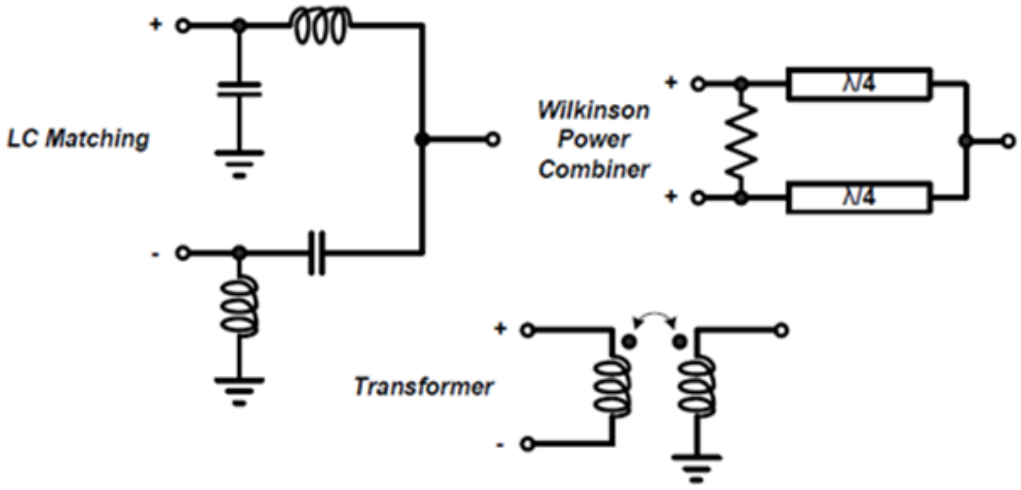


Figure 5.7 **Conventional power – combining techniques**

Thus, with the use of transformer-type output networks, several successful efforts have been reported for both power combining and impedance transformation. Some reported techniques, such as distributed active transformers (DATs) [16, 27], shown in Figure 5.8, or their variations [28, 34, 35], and figure-eight structures [36] are good examples of series-combining transformer (SCT); and recently introduced voltage-boosting parallel-primary transformers [37, 38] are examples of parallel-combining transformer (PCT).

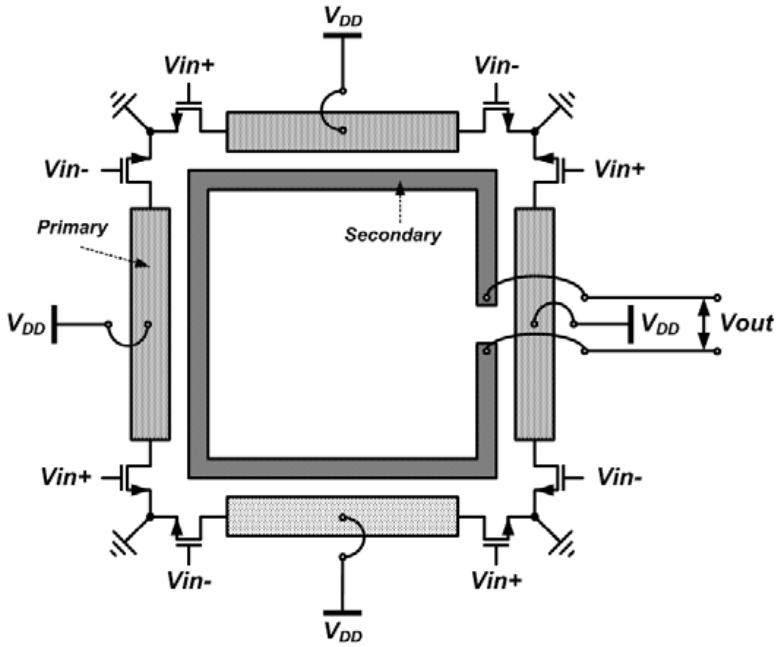


Figure 5.8 **Diagram of a DAT PA**

5.4.2 Linearity Enhancement Techniques

To address the linearity of a PA, one must consider both the fundamental cause of nonlinearity and the nonlinear behavior of the PA topics of interest. Pertaining to the causes of nonlinearity, transconductance and gate-source capacitance are considered the key factors that determine linearity among the many conductance and capacitive components [24, 29]. For capacitive components, the absolute amount of capacitance itself is not a problem, but the amount of transition resulting from a large-signal swing is the actual cause of nonlinearity. The neutralization of a capacitance transition can be attained by adding a transistor with an opposite characteristic in parallel with the main transistor. In Figure 5.9, the main transistor generating output power is an NMOS transistor MN, and PMOS MP is in parallel with it, described in Equation (5.11). Then, the input signal swing does not suffer from the transition of input capacitance, and the linearity of the PA can be improved [29]. In this figure, the termination of a second harmonic is also shown to suppress the return of a second harmonic to the gate of the transistor, thus averting the third-order inter-modulation [24].

When the behavior of a PA is known in advance and the nonlinearity behavior of the PA can be mimicked using other components, the distortion can be suppressed. The pre-distortion of a PA in which the compression of gain and phase are adequately matched with the pre-distorter generating a very linear output signals is shown in Figure 5.10.

For meeting the specifications of high data-rate communications, linearity enhancement is one of the most important design aspects. Therefore, more efforts are required to guarantee good linearity with increases in PAR.

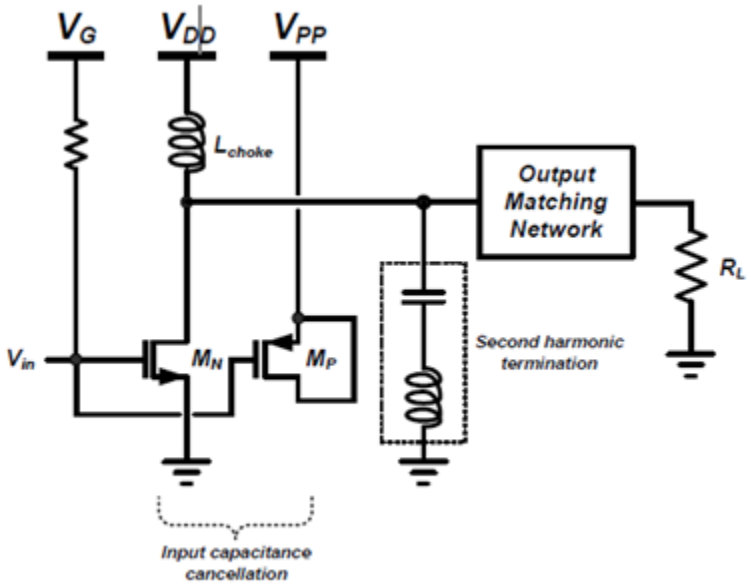


Figure 5.9 **Input capacitance cancellation techniques**

$$C_{in}(V_{in}) = C_{g,M_N} + C_{g,M_P} \qquad \textbf{(5.13)}$$

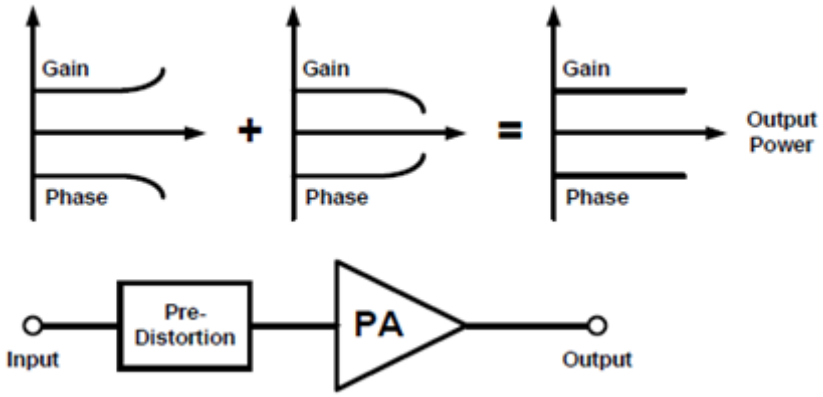


Figure 5.10 **Pre-distortion of a PA**

5.4.3 Efficiency Enhancement Techniques

Since the early era of radio signaling a century ago, concepts for system PAs such as the Doherty PA [31], the Kahn PA [32], and the Chireix PA [33] have been developed. Such techniques have been well established and adopted successfully in base stations. However, even for GaAs HBT PA modules, realizing such techniques in a small form factor poses a formidable challenge, so only a few relatively unsuccessful examples have been reported. However, these techniques require the application of efficiency enhancement techniques to CMOS PAs, posing even greater challenges due to their poor passive performance. Therefore, their performance is far from that demanded in commercial production [39-41].

Among such techniques, the polar transmitter, illustration in Figure 5.11, became very popular recently with the aid of digital signal processing. From the baseband system, an amplitude modulated signal, (tt), and quadrature phase signals, $PPi(tt)$ and $PPqq(tt)$, are generated. The PA has the input of phase modulation but with a constant envelope, but the amplitude modulation through the operation amplifier and PMOS keeps the operation point of the PA in the saturation mode with a constant envelope that maximizes efficiency. The output of the PA can be represented as Equation (5.14).

$$v(t) = A(t) \cdot \cos\left(\omega_c t + \sqrt{P_i(t)^2 + P_q(t)^2}\right) \qquad \textbf{(5.14)}$$

Unfortunately, the polar transmitter system suffers from a mismatch of amplitude and phase loss by the PMOS, and the complicated operation requirements. Therefore, the trade-off between efficiency enhancement and circuit complexity should be carefully considered in advance.

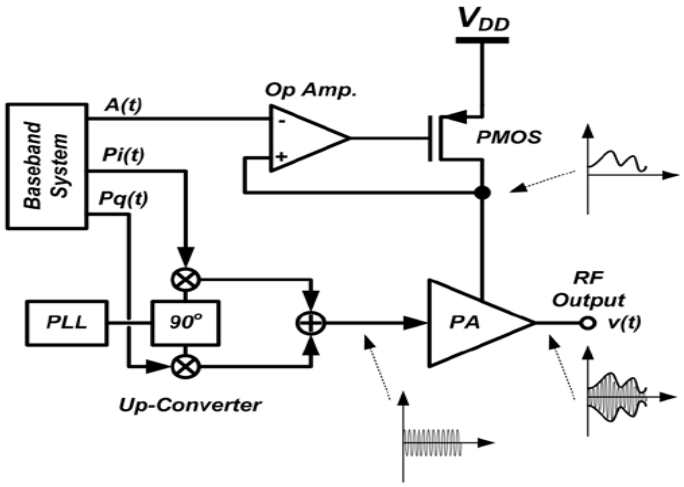


Figure 5.11 **Polar transmitter system**

5.5 CMOS Design of Proposed Power Amplifier

Proposed design of CMOS Power amplifier is shown in Figure 5.12 below. The CMOS_IC consists of 5 pins where Pin 1 and 2 are the input and output ports for RF signal respectively, Pin 3 is used for V_{CC} input and pins 4 and 5 are the ground pins. Two coupling capacitors C_4 and C_5 are placed at the input and output of CMOS IC whereas Resistor R_1 is placed for current limiting. The designed input and output impedance matching circuits together with the harmonic suppression circuits are inside the CMOS_IC. V_{CC} voltage of 4.2 is provided at pin 3 and capacitor C_6 is used for filtering of unwanted noise.

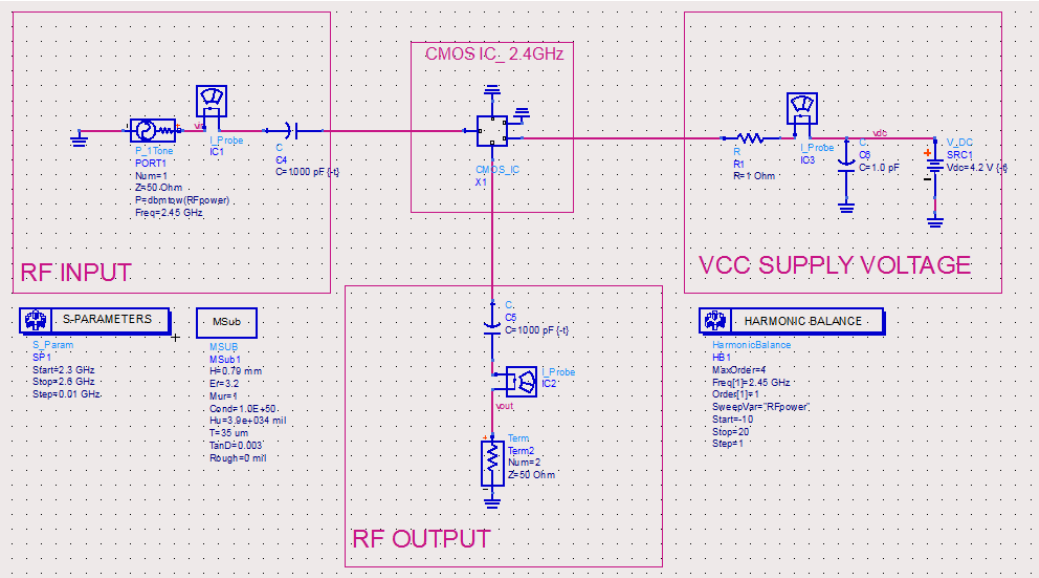


Figure 5.12 **CMOS design of Proposed P.A**

The designed CMOS Power amplifier is simulated and tuned for different values of coupling capacitors which helps to improve the output gain and Power added efficiency. The input and output ports are matched to 50Ω impedance to keep up the standard design. The grounding of pins 4 and 5 are properly done with the lower side of the PCB in order to connect the RF AC ground with the DC ground. The simulation parameters are set from 2.3 GHz to 2.6 GHz and step size of 0.01 GHz. The CMOS IC together with these external lumped components is to be placed on Taconic PCB with dielectric constant of 3.2 and thickness of 0.79mm.

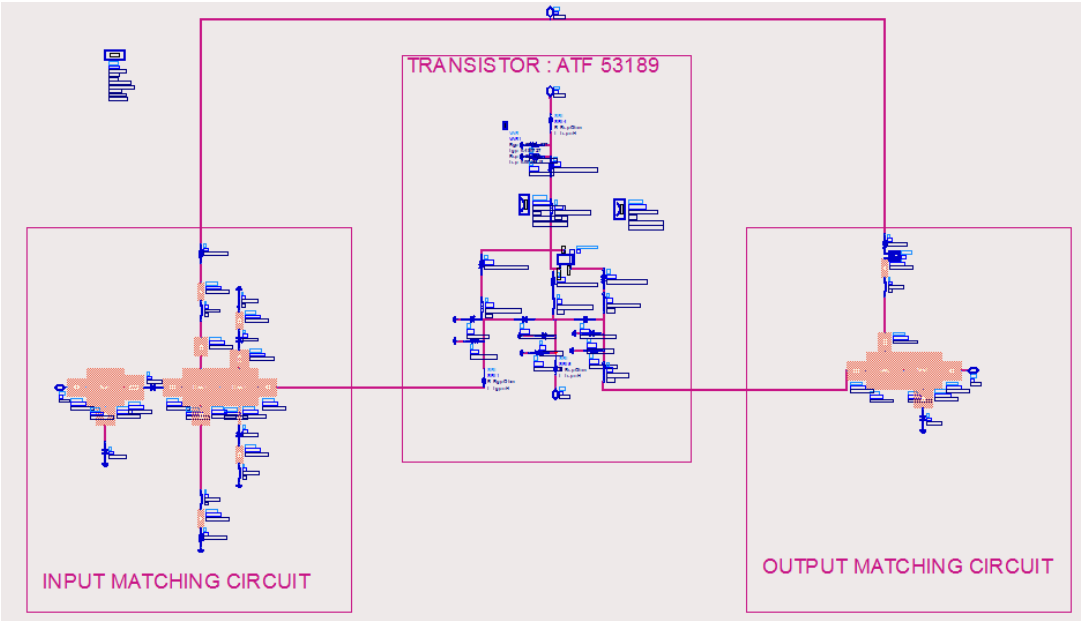


Figure 5.13 **Internal diagram of the designed CMOS IC**

The internal diagram of the designed CMOS Power amplifier is shown in figure 5.13 where the input and output matching circuits together with the biasing circuit and transistor ATF-53189 is shown. In this diagram the transistor ATF-53189 is lumped with other tuned components which are already present in the ATF-53189. In figure 5.13 the highlighted ATF-53189 is placed with the optimized lumped components and the biasing resistors are also connected within this transistor. The RF input port of this transistor is joined with the designed input impedance matching circuit and the RF output port is connected with the output impedance matching circuit. Both the input and output impedance matching circuits are the co-simulated versions which assure that this final design will have very close results to the fabricated one. Finally the RF input – output ports are introduced together with the V_{CC} and GND pins.

Chapter 6

Simulated and Measured Results

6. Simulated Results:

6.1.1 Simulation results of Single stage Power Amplifier

Figure 6.1 Show the simulated results of proposed single stage power amplifier. Using a single transistor the designed power amplifier is providing output gain of 18 dB and the Power added efficiency is 45.5%. The power amplifier is stable for the whole bandwidth of WIFI and Bluetooth applications. The S-Parameters are as follows: S_{11} is -18.7 dB, S_{12} is -23.4 dB, S_{21} is 18 dB and S_{22} is -21.5 dB.

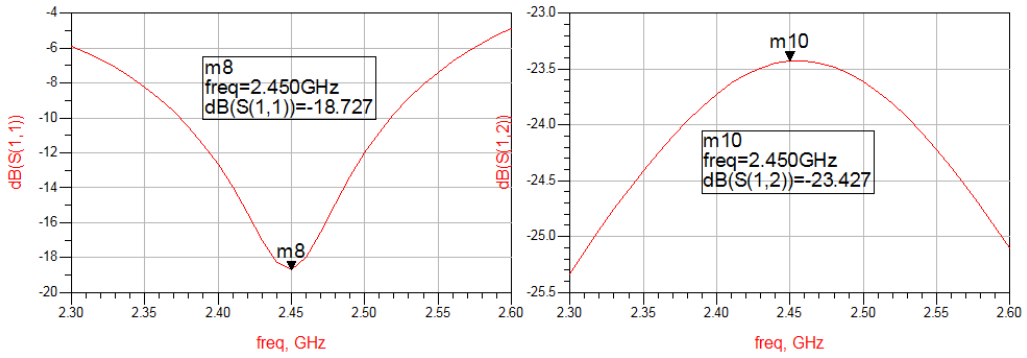


Figure 6.1(a) S_{11} & S_{22} VS frequency of single stage Power amplifier

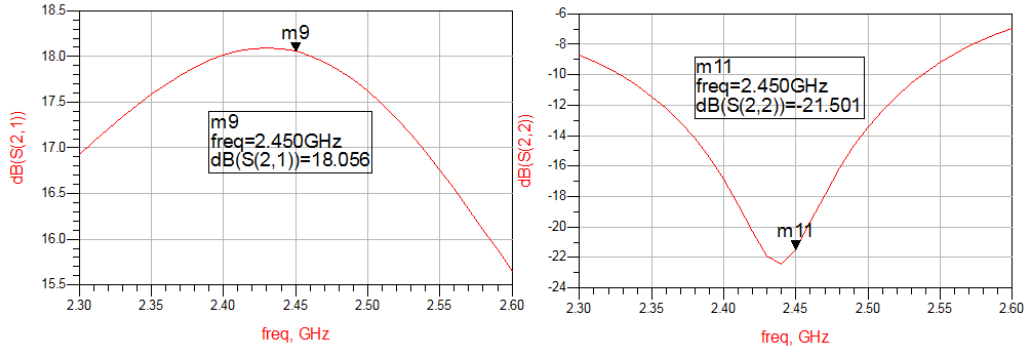


Figure 6.1(b) S_{21} & S_{22} VS frequency of single stage Power amplifier

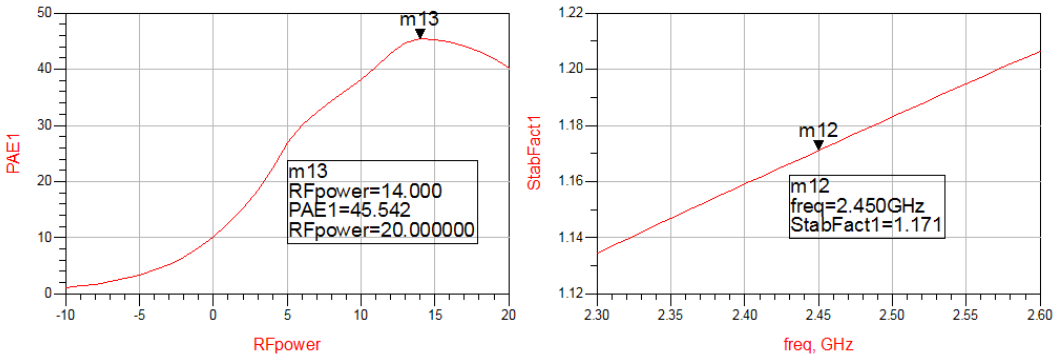


Figure 6.1(c) Power Added Efficiency and Stability VS frequency of single stage Power amplifier

In Figure 6.1 (c) the maximum value of Power added efficiency is 45.5% which is achieved at an input power of 14 dB. At about 6 dB back off power the Power added efficiency falls to 40%.

6.1.2 Co-simulation results of single stage Power Amplifier

In Figure 6.2 test results show that by added the harmonic suppression circuit the Power added efficiency has increased from 45.5% to 53%. The maximum output gain S_{21} comes out to be 17.5dBm, S_{11} is -20.4dBm, S_{12} is -23.6dBm and S_{22} is –12.13dBm. These are the optimized results after co-simulation where input-output matching circuit components and AC filtering inductors are tuned to get maximum Gain and Power added Efficiency (PAE). The output gain of this amplifier is almost linear from 2.3 GHz to 2.45 GHz and then it slowly decreases.

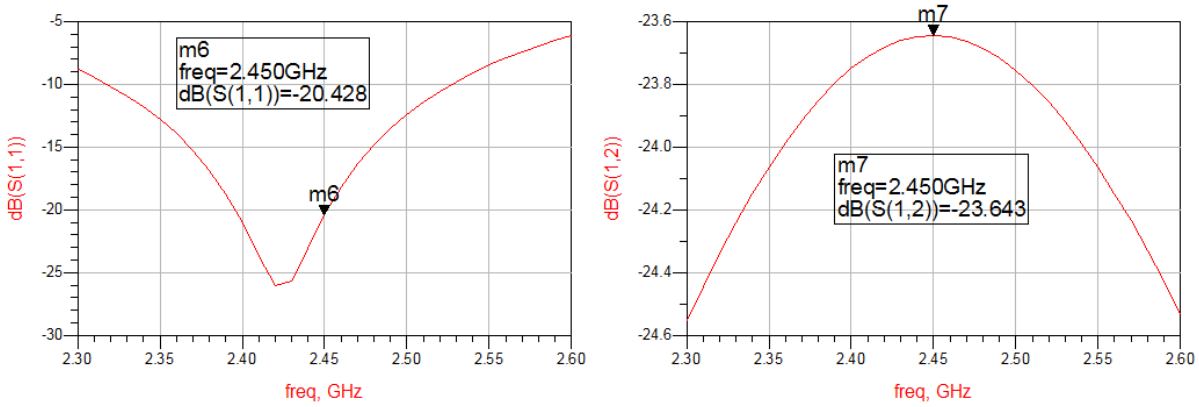


Figure 6.2(a) S_{11} & S_{22} VS frequency of single stage Power Amplifier

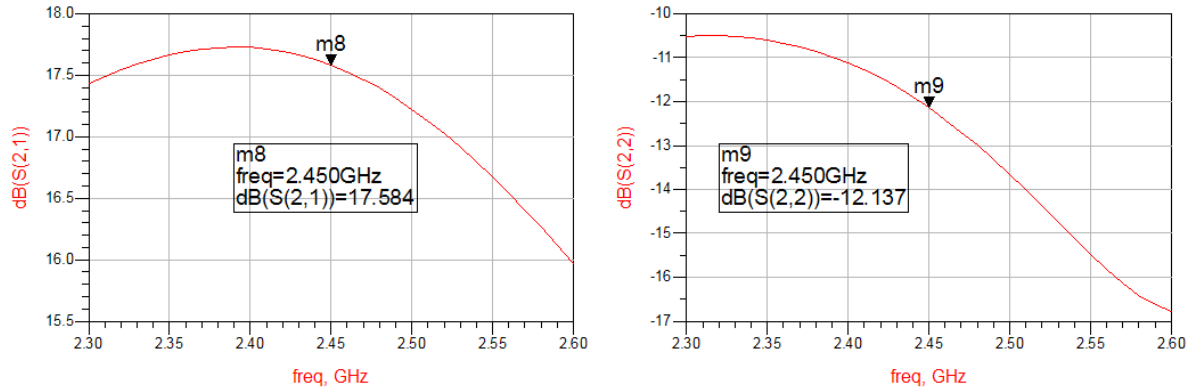


Figure 6.2(b) S_{21} & S_{22} VS frequency for Co-simulation of single stage amplifier

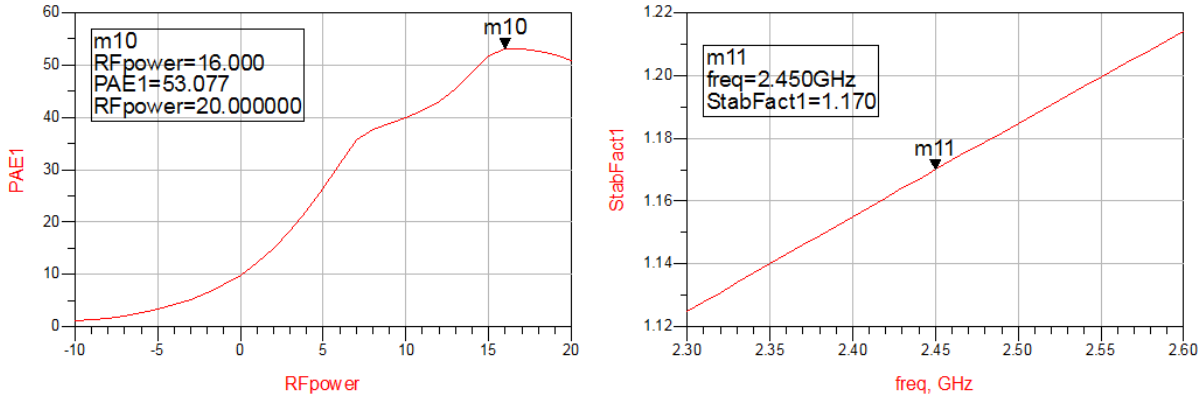


Figure 6.2 (c) Power Added Efficiency and Stability VS frequency for Co-simulation of single stage Power amplifier

The Power added efficiency is Figure 6.2 (c) shows that after co-simulation and tuning this parameter value become 53% at an input power of 16 dB and at 6 dB back off Power it drops to 41.3%.

Thus these values show that the final co-simulated schematic can be processed for fabrication and testing.

6.1.3 Simulated Results of two stage Power Amplifier (Schematic Results)

From Figure 6.3, the output gain parameter S_{21} comes out to be 26.45dBm while the Power added efficiency is 31.6%. Since these are the simulation results and further improvement in output Gain and Power added efficiency can be achieved by tuning and optimization of the circuit which is done in co-simulation circuit below.

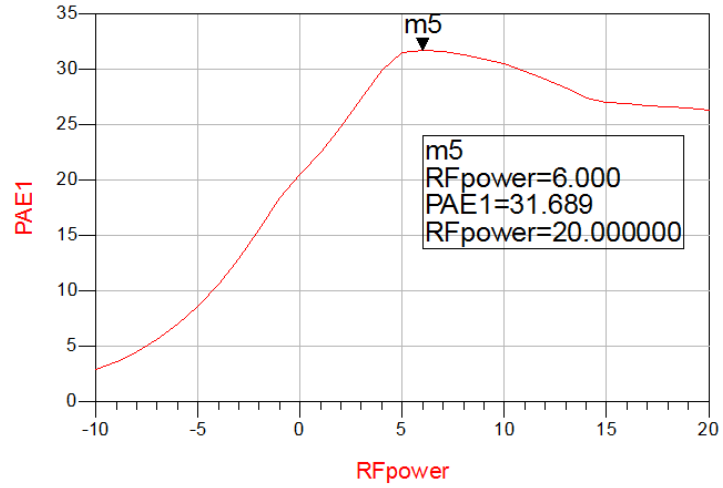


Figure 6.3(a) Power Added Efficiency VS Input RF power of simulated two stages Power amplifier

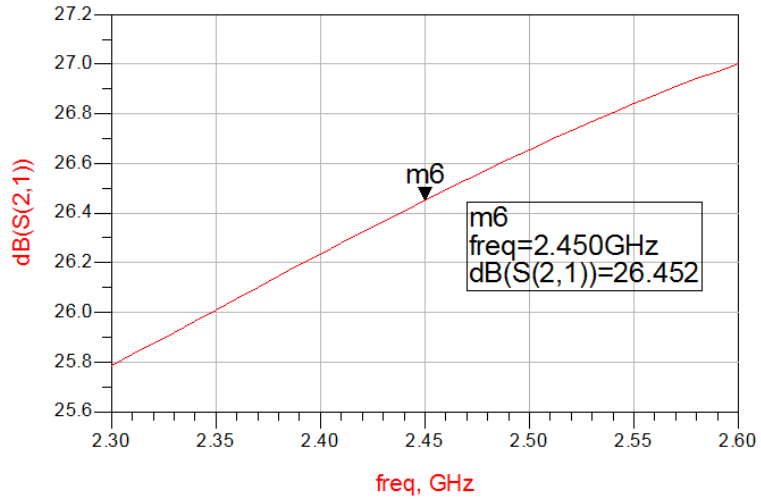


Figure 6.3(b) S_{21} VS Frequency of simulated two stages Power Amplifier

6.1.4 Simulation results of two stage Power Amplifier (Co-Simulation Results)

From Figure 6.4 the Plot for S-parameters and Power Added Efficiency are shown. It is clear that the optimizing and tuning of Schematic in co-simulation has increased the Gain of Power amplifier and now it has improved up to 34.6dBm which is more than twice as was for single stage Power amplifier. The Power Added Efficiency came out to be 55.4%, stability factor K is 2.5 which show that the power amplifier is stable for the design frequency 2.45 GHz. The other S-parameters are as follows: S_{11} is -32.3dB, S_{12} is -48.3dB, S_{21} is 34.6dB and S_{22} is -28.8dB.

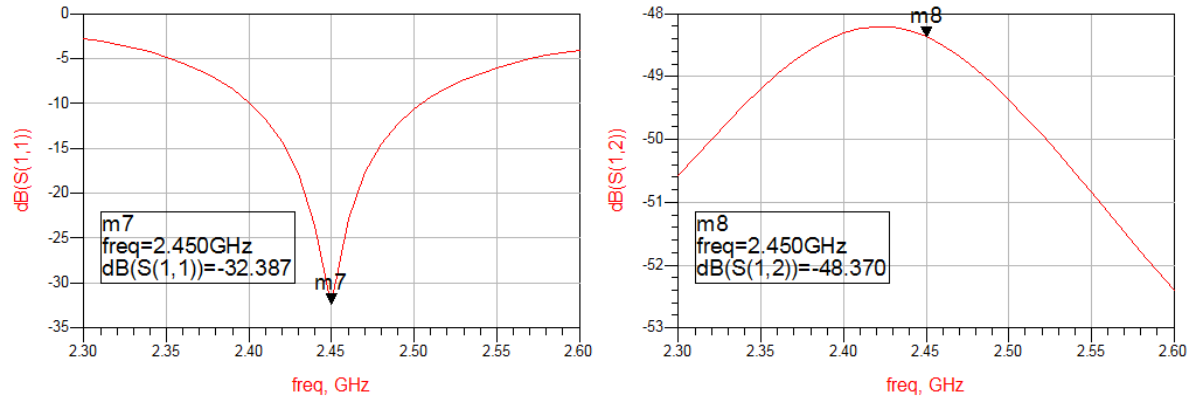


Figure 6.4(a) S_{11} & S_{12} VS frequency of Co-simulated two stages Power amplifier

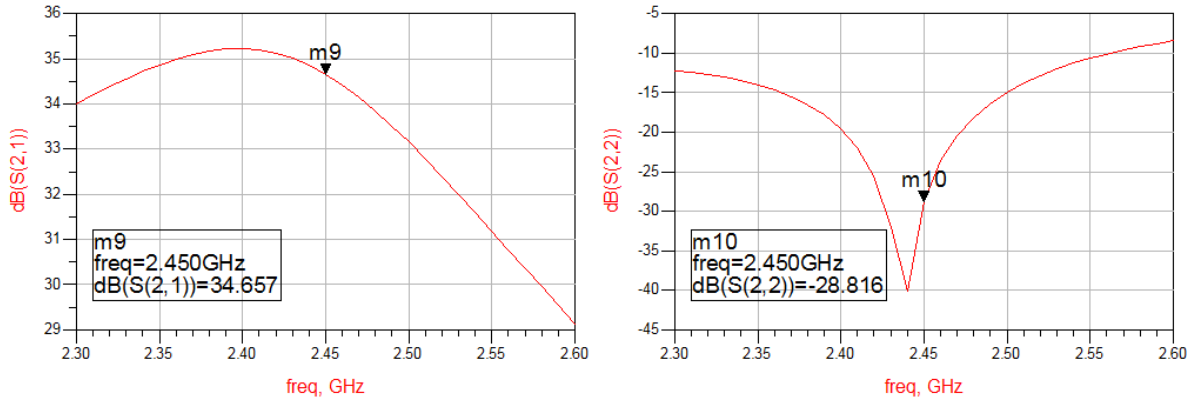


Figure 6.4(b) S_{21} & S_{22} VS frequency of Co-simulated two stages Power amplifier

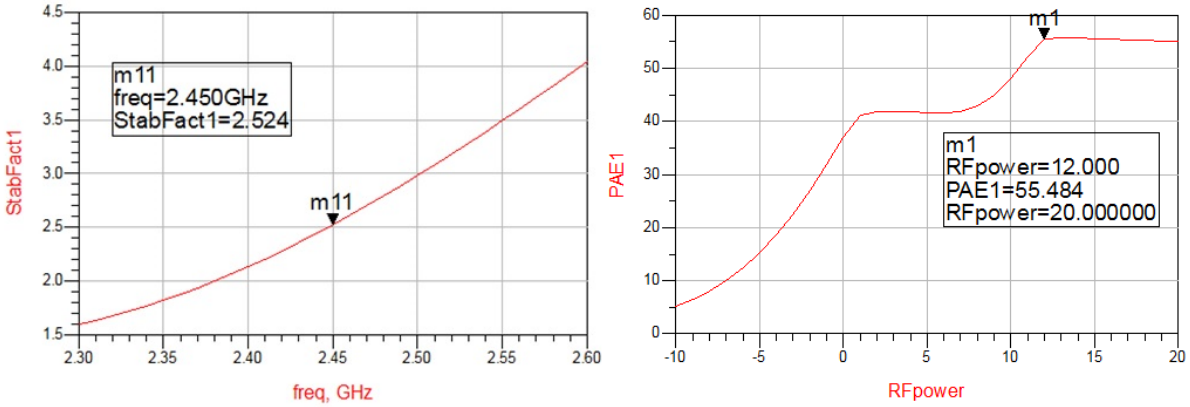


Figure 6.4(c) Power Added Efficiency & Stability of Co-simulated two stages Power amplifier

6.1.5 Results of CMOS Power Amplifier

Figure 6.5 show the results of the CMOS Power Amplifier. The final design is optimized and simulated in ADS software where the S-Parameters are as follows: S_{11} is -25.4 dB, S_{12} is -23.3 dB, S_{21} is 17.1 dB and S_{22} is -11.3 dB. The power amplifier is stable from 2.3 GHz up to 2.6 GHz and the Power Added Efficiency came out to be 42.6%. These Results show that the designed CMOS Power Amplifier is stable, providing the desired efficiency and high output Gain for our WIFI and Bluetooth applications.

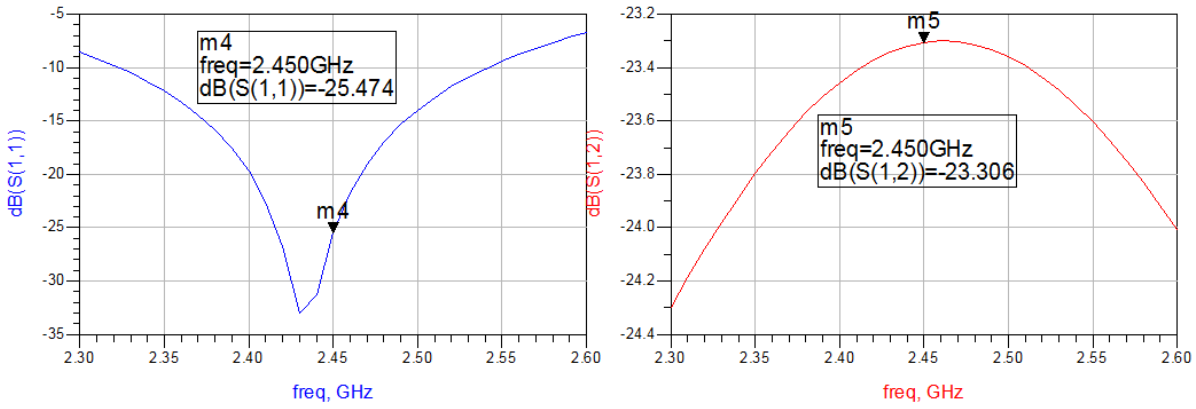


Figure 6.5(a) S_{11} & S_{12} VS frequency of CMOS Power amplifier

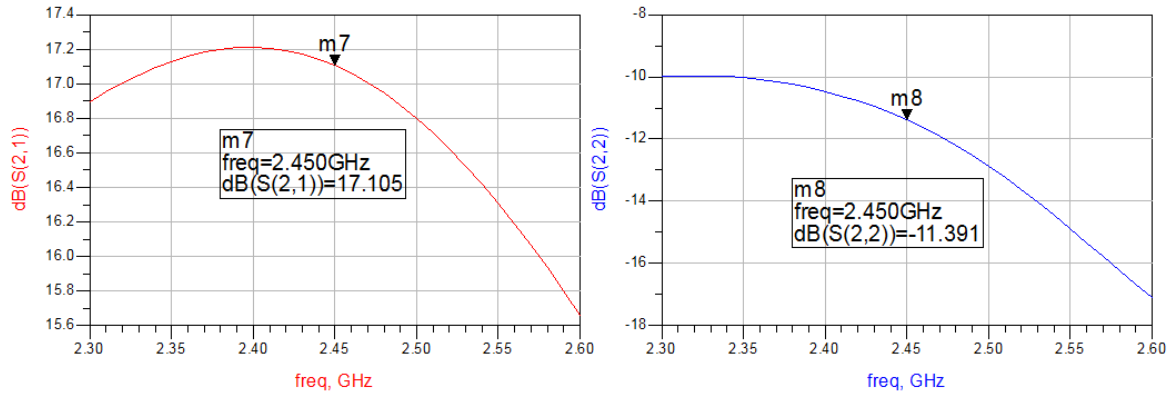


Figure 6.5(b) S_{21} & S_{22} VS frequency of CMOS Power amplifier

Figure 6.5 (c) depicts that the Power added efficiency in case of CMOS Power amplifier has the maximum value of 42.6% which is achieved at 14 dB input RF power and this value is maintained at ±2 dB signal. Also the stability graph show the value of K = 1.18 which is a stable value and the designed Power amplifier is stable between the frequencies 2.3 GHz up to 2.6 GHz.

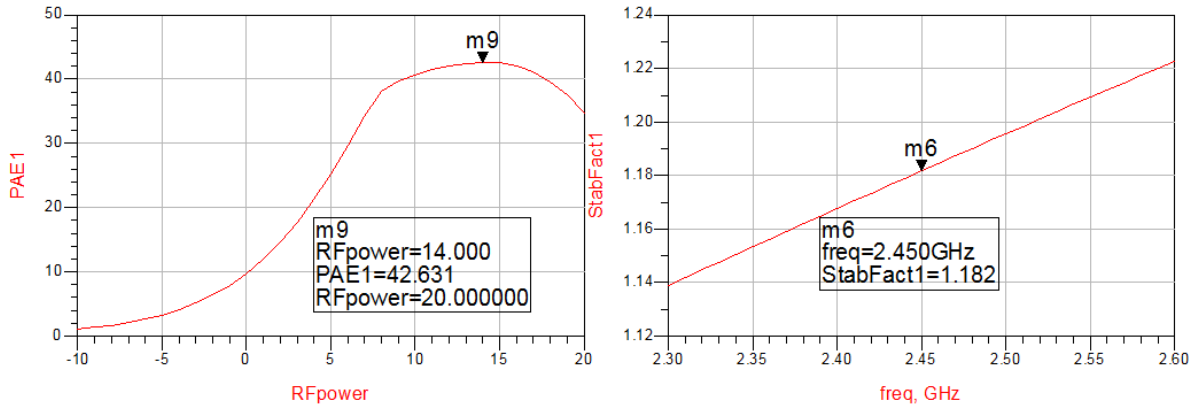


Figure 6.5(c) Power Added Efficiency and Stability of CMOS Power amplifier

6.2 Measured Results:

6.2.1 Test Setup

In measurement process the main elements which need to be measured are the Output power, Gain, input-output impedance matching and linearity.

First the S-parameters of the fabricated Power amplifier are tested using E5071C Vector Network Analyzer which is capable of covering the frequency range 9 kHz to 8.5 GHz. In the first step the VNA is calibrated which involves the use of open and short circuit loads of standard 50 Ω. Figure 6.6 below shows the setup for measuring the S-parameters.

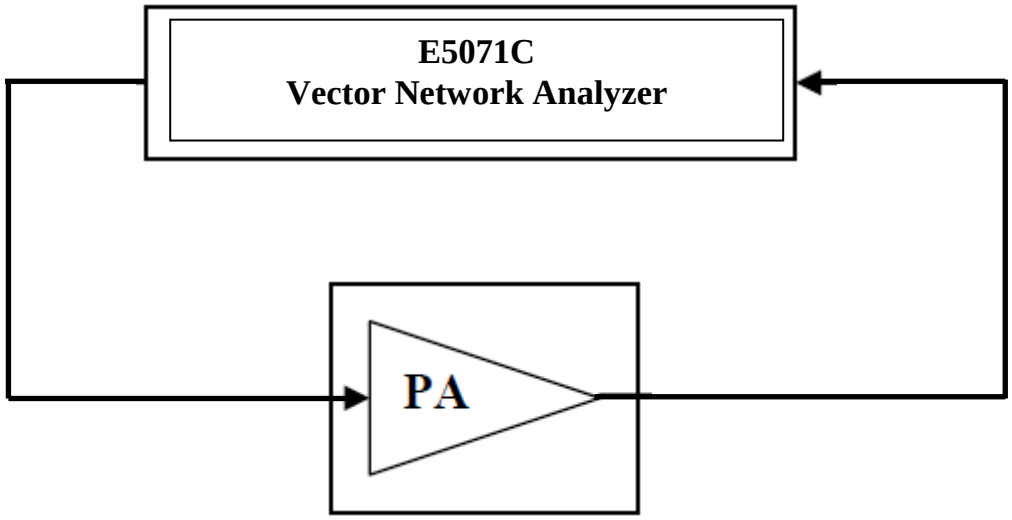


Figure 6.6 Test setup for measuring the S-Parameters

After testing the fabricated design on VNA, the results are shown below. Figure 6.7 and 6.8 show the results of output power for single stage and 2-stage Power amplifiers respectively. The Single stage Power Amplifier delivers output power of 16.7dB in case of single stage while in 2-stage Amplifier its output Power is 30.5dB. The measured results in both the cases are almost similar to the simulation results.

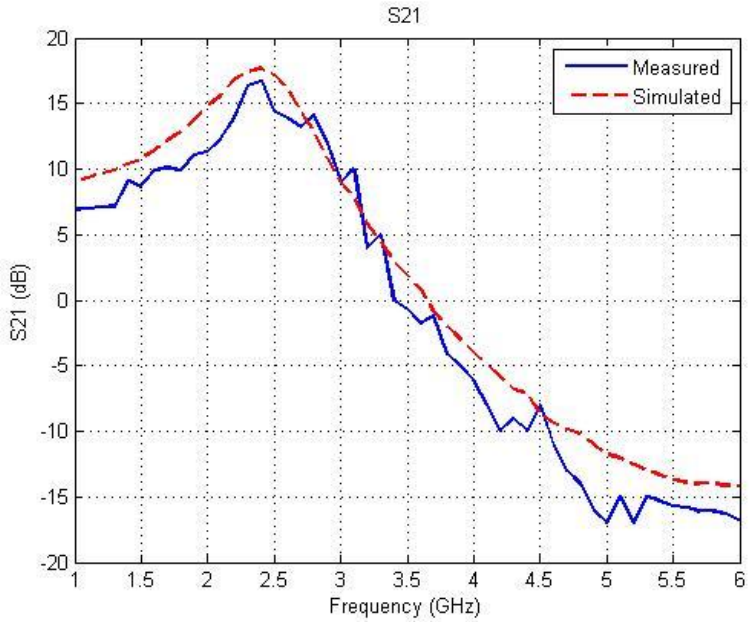


Figure 6.7 Measured Output Power VS frequency plot of single stage Power Amplifier

In Figure 6.7 the X-axis defines the frequency and the Y-axis defines the output power gain. As the frequency increases from 1 GHz to 6 GHz the gain initially starts to increase and at 2.4 GHz its value is 16.7 dB which is the maximum gain seen in this plot. From 2.4 GHz onwards the gain begin to decrease and it soon falls below 0 dB at 3.6 GHz.

Looking towards Figure 6.5 for the measured results of two stage Power amplifier the gain can be seen to increase from 10 dB at 1 GHz and it soon reaches to 30.5 dB at 2.4 GHz where it becomes stable and the Power amplifier maintains this gain up to 2.5 GHz then it begins to fall and at 4 GHz the gain becomes 0 dB.

For both single stage and two stages Power amplifier the output gain has a bandwidth of nearly 200 MHz which assures that the proposed Power amplifier will maintain its gain of 16.7 dB in single stage and 30.5 dB in two stages power amplifier for its applications in WIFI and Bluetooth.

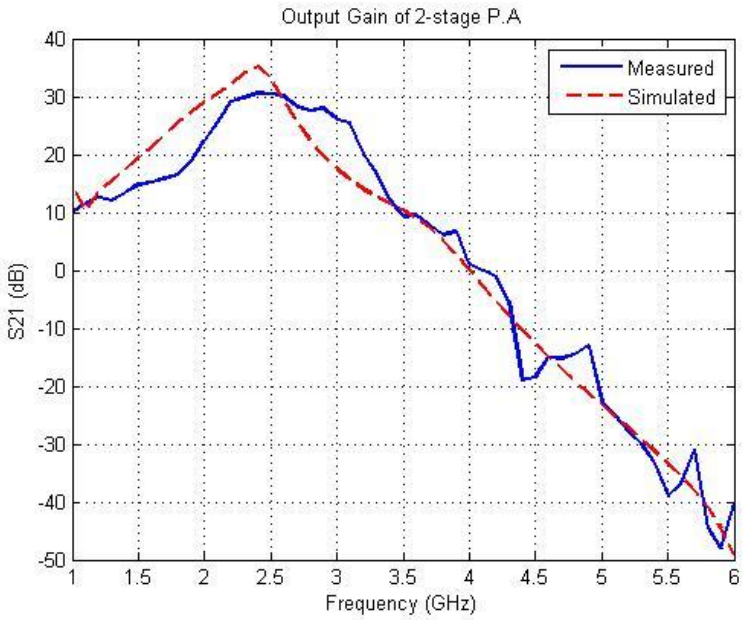


Figure 6.8 Measured Output Power VS frequency plot of two stage Power amplifier

The Power Added Efficiency is also measured and its plot is shown in Figure 6.9. In this figure the input RF power is plotted on X-axis and the Power Added Efficiency is plotted on Y-axis. At around 0 dB input power, the Power Added Efficiency is nearly 8% which begins to incline and just after 5 dB increase in input RF power the efficiency of the proposed Power amplifier reaches to 24%. The peak of Power Added Efficiency is 49.5% which can be seen at an input signal power of 15 dB and these results are quite similar to the simulated one.

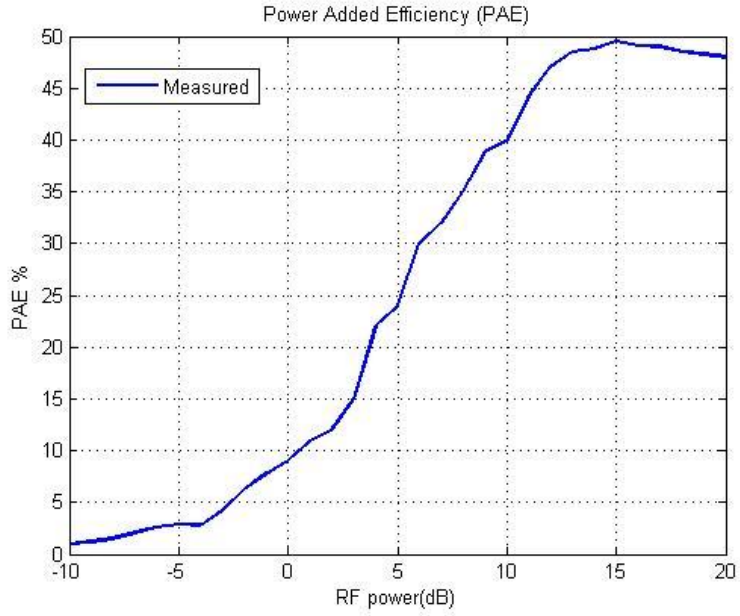


Figure 6.9 Measured Power Added Efficiency VS input RF power

Finally the plot for S_{11} is shown in Figure 6.10 and 6.11 for both single stage and 2-stage Power amplifiers respectively. In both the results the return losses are low enough which ensures that most of the input RF signal will reach the Transistor for amplification process.

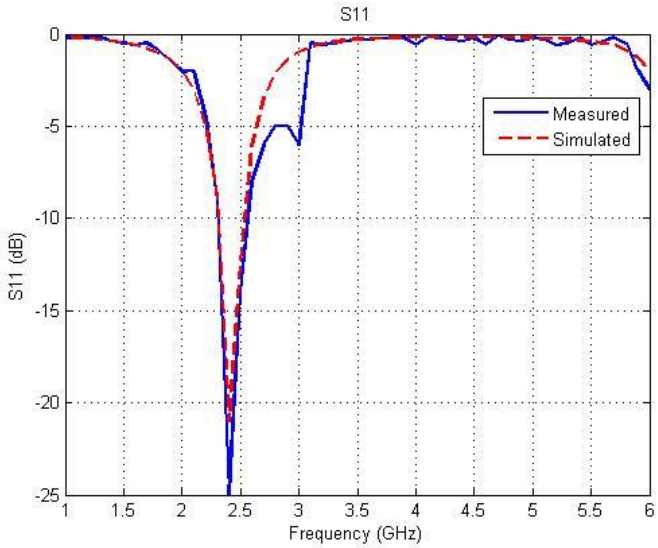


Figure 6.10 Measured S_{11} VS frequency of Single Stage Power Amplifier

In case of single stage Power amplifier the S_{11} in Figure 6.10 shows compromising results. At 2.4 GHz frequency the return losses are nearly -26 dB which is quite enough for the low power input single to reach the input port of transistor for amplification.

The S_{11} in Figure 6.11 for two stage Power amplifier show that at 2.4 GHz the S_{11} is -14 dB. In both the single stage and two stages Power amplifier the input return losses are below -10 dB which is the threshold value.

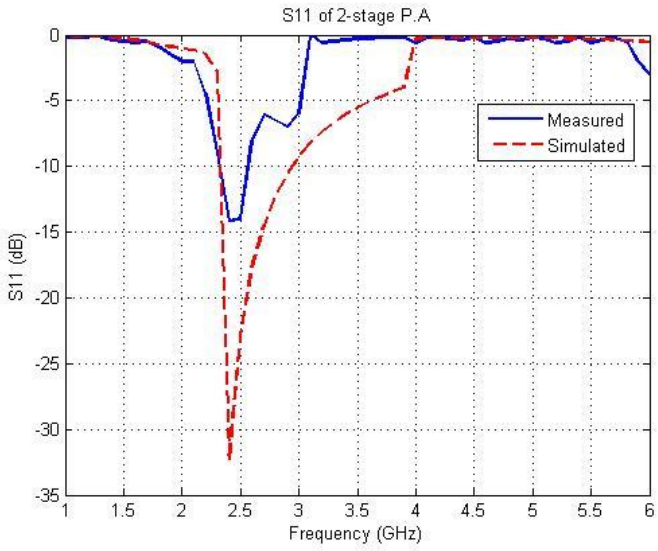


Figure 6.11 Measured S_{11} VS frequency of two stages Power Amplifier

Chapter 7

Conclusion and Future Work

7.1 **Conclusion**

In this work the design of an Efficient Power Amplifier for 2.4 GHz frequency is presented with a high output Power. First different design techniques of amplifiers are discussed which show many classes of amplifiers and their pros and cons. Then a class of amplifier is selected which delivers the desired efficiency and output gain.

After the selection of a suitable Class of amplifier, a simple simulation for our desired frequency power amplifier is carried out on ADS software and the test results are checked for its efficiency and output gain. Then optimized input and output impedance matching circuits are designed which enhances the output gain for our Amplifier.

For the improvement in efficiency, the harmonic suppression techniques are implemented on the designed Power amplifier to achieve the improved Power Added Efficiency while maintaining the high output Gain.

It was noted that using two harmonic suppression circuits at the input of our proposed Power amplifier, its efficiency can improved. DC supply voltage V_{CC} was chosen to be 4.2 v and the DC biasing circuit was tuned in such a way in order to deliver 4 v and 135 mA to the drain source loop of the transistor.

In case of two stage power amplifier, a well designed impedance matching circuit was used to match the output impedance of 1^{st} stage with the input impedance of 2^{nd} stage. In this 2-stage power amplifier, the output gain was targeted to be above 30 dB while compromising for little loss of efficiency.

Presented simulated and measured results for both single stage and two stage Power amplifier are in good agreement. In case of single stage power amplifier 49.5% Power Added Efficiency was achieved where as in case of two stage Power amplifier it was 45%. Output

gain of 16.7 dB in case of single stage and 30.5 dB in case of two stage Power amplifier was achieved.

7.2 **Future Work**

- Since the proposed Power amplifier is very useful in many applications like WIFI, Bluetooth and other devices which uses 2.4 GHz frequency the improvements in designed Power amplifier is inevitable.
- Design and simulation of CMOS Power amplifier has been presented in thesis. The design can be fabricated and techniques can be implemented to reduce the size of the CMOS Power amplifier for its applications in WIFI and Bluetooth.

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